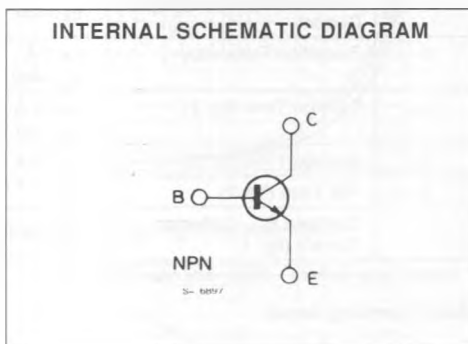
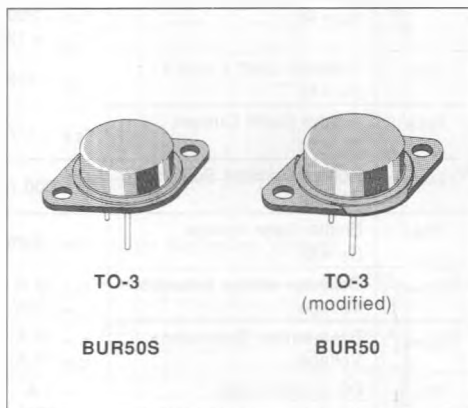


HIGH CURRENT, HIGH SPEED, HIGH POWER TRANSISTOR

DESCRIPTION

The BUR50 is a silicon multiepitaxial planar NPN transistor in modified Jedec TO-3 metal case, the BUR50S is the same type in Jedec TO-3 metal case, intended for use, in switching and linear applications in military and industrial equipment.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base Voltage ($I_E = 0$)	200	V
V_{CEO}	Collector-emitter Voltage ($I_B = 0$)	125	V
V_{EBO}	Emitter-base Voltage ($I_C = 0$)	10	V
I_C	Collector Current	70	A
I_{CM}	Collector Peak Current ($t_p = 10$ ms)	100	A
I_B	Base Current	20	A
P_{Tot}	Total Power Dissipation at $T_{case} \leq 25$ °C	350	W
T_{stg}	Storage Temperature	- 65 to 200	°C
T_j	Junction Temperature	200	°C

THERMAL DATA

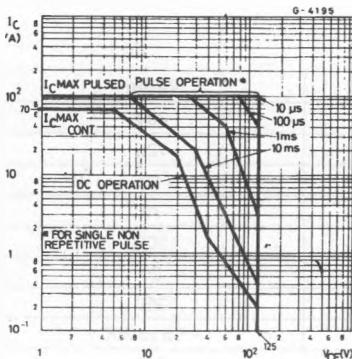
$R_{th\ j-case}$	Thermal Resistance Junction-case	Max	0.5	°C/W
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ELECTRICAL CHARACTERISTICS ($T_{case} = 25\text{ °C}$ unless otherwise specified)

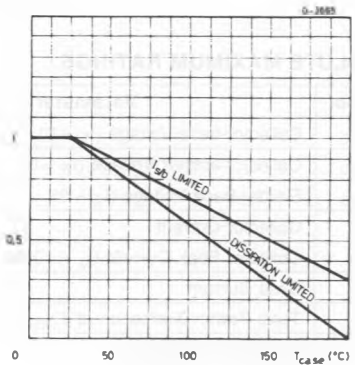
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cutoff Current ($I_E = 0$)	$V_{CB} = 200\text{ V}$ $V_{CB} = 200\text{ V}$ $T_{case} = 125\text{ °C}$			0.2 2	mA mA
I_{CEO}	Collector cutoff Current ($I_B = 0$)	$V_{CE} = 125\text{ V}$			1	mA
I_{EBO}	Emitter Cutoff Current ($I_C = 0$)	$V_{EB} = 7\text{ V}$			0.2	mA
$V_{CEO(sus)}^*$	Collector-emitter Sustaining Voltage	$I_C = 200\text{ mA}$	125			V
V_{EBO}	Emitter-base Voltage ($I_C = 0$)	$I_E = 10\text{ mA}$	10			V
$V_{CE(sat)}^*$	Collector-emitter Saturation Voltage	$I_C = 35\text{ A}$ $I_C = 70\text{ A}$		0.8	1 1.5	V V
$V_{BE(sat)}^*$	Base-emitter Saturation Voltage	$I_C = 35\text{ A}$ $I_C = 70\text{ A}$		1.6	1.8 2	V V
h_{FE}^*	DC Current Gain	$I_C = 5\text{ A}$ $I_C = 50\text{ A}$	20 15		100	
$I_{s/b}$	Second Breakdown Collector Current	$V_{CE} = 20\text{ V}$	17.5			A
f_T	Transition Frequency	$I_C = 1\text{ A}$ $f = 1\text{ MHz}$	10	16		MHz
t_{on}	Turn-on Time (fig. 2)	$I_C = 70\text{ A}$ $V_{CC} = 60\text{ V}$		0.5	1.2	μs
t_s	Storage Time (fig. 2)	$I_C = 70\text{ A}$		0.82	2	μs
t_f	Fall Time (fig. 2)	$I_{B2} = -7\text{ A}$ $V_{CC} = 60\text{ V}$		0.1	0.5	μs
	Clamped $E_{s/b}$ Collector Current (fig. 1)	$V_{clamp} = 125\text{ V}$ $L = 500\text{ μH}$	70			A

* Pulsed : pulse duration = 300μs, duty cycle ≤ 2%.

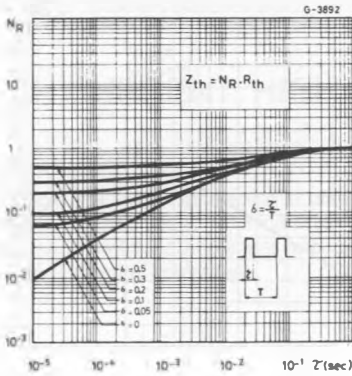
Safe Operating Areas.



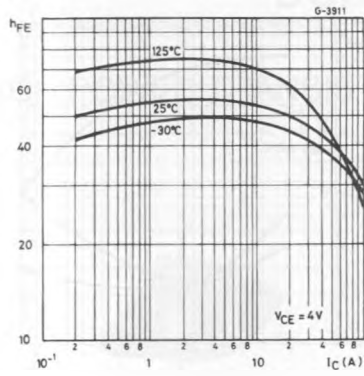
Derating Curves.



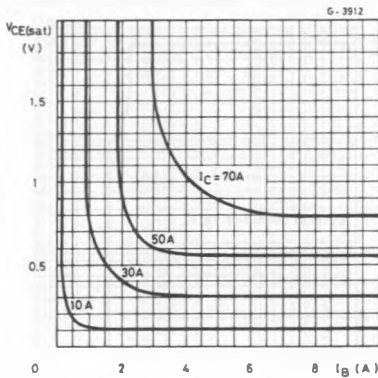
Thermal Transient Response.



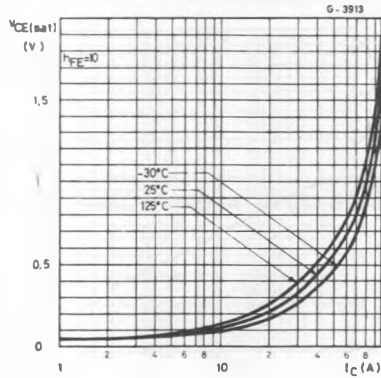
DC Current Gain.



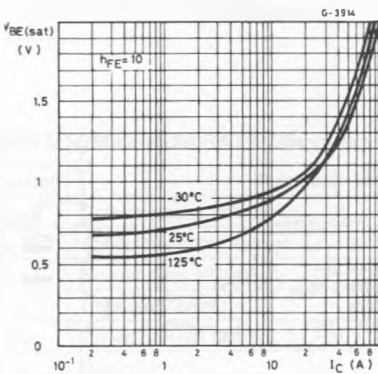
Collector-emitter Saturation Voltage.



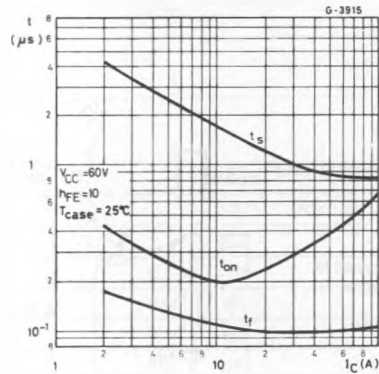
Collector-emitter Saturation Voltage.



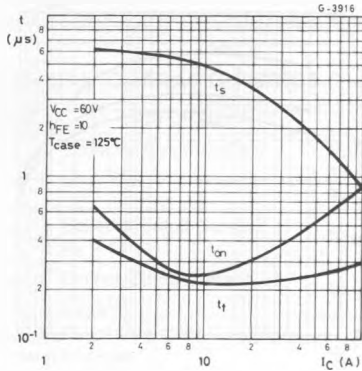
Base-emitter Saturation Voltage.



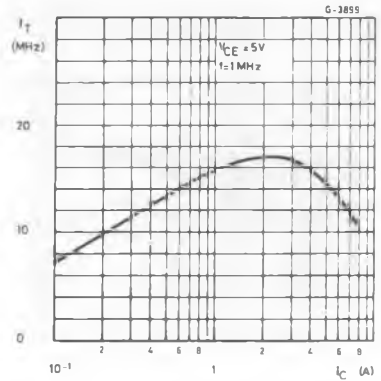
Saturated Switching Characteristics.



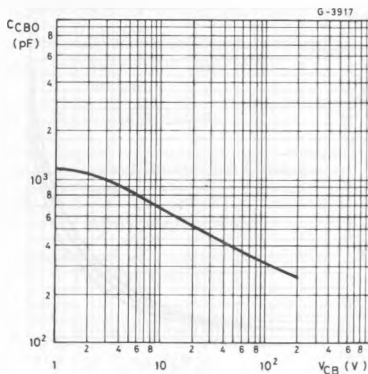
Saturated Switching Characteristics.



Transition Frequency.



Collector-base Capacitance.



Clamped Reverse Bias Safe Operating Areas.

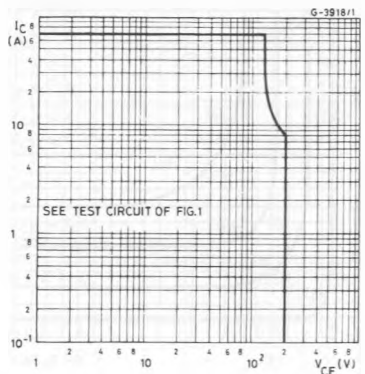


Figure 1 : Clamped $E_{s,b}$ Test Circuit.

Figure 2 : Switching Times Test Circuit (resistive load).

