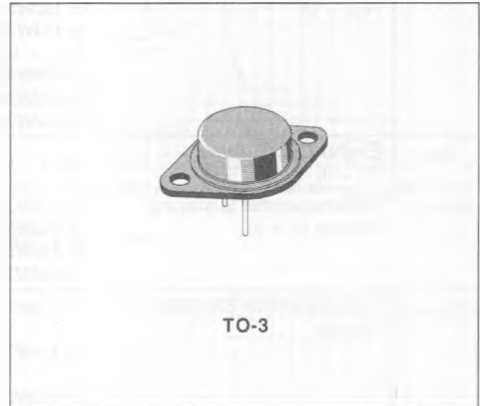


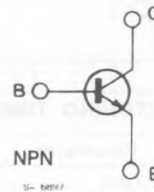
## HIGH VOLTAGE POWER SWITCH

### DESCRIPTION

The BUW34, BUW35 and BUW36 are silicon multi-epitaxial mesa NPN transistors in Jedec TO-3 metal case. They are intended for high voltage, fast switching applications.



### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		BUW34	BUW35	BUW36	
$V_{CES}$	Collector-emitter Voltage ( $V_{BE} = 0$ )	500	800	900	V
$V_{CEO}$	Collector-emitter Voltage ( $I_B = 0$ )	400	400	450	V
$V_{EBO}$	Emitter-base Voltage ( $I_C = 0$ )	7			V
$I_C$	Collector Current	10			A
$I_{CM}$	Collector Peak Current	15			A
$I_B$	Base Current	5			A
$P_{tot}$	Total Power Dissipation at $T_{case} \leq 25^\circ\text{C}$	125			W
$T_{stg}$	Storage Temperature	- 65 to 200			$^\circ\text{C}$
$T_j$	Junction Temperature	200			$^\circ\text{C}$

**THERMAL DATA**

$R_{th(j-case)}$	Thermal Resistance Junction-case	max	1.4	°C/W
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**ELECTRICAL CHARACTERISTICS** ( $T_{case} = 25\text{ °C}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{CES}$	Collector Cutoff Current ( $V_{BE} = 0$ )	for <b>BUW34</b> $V_{CE} = 500\text{ V}$ for <b>BUW35</b> $V_{CE} = 800\text{ V}$ for <b>BUW36</b> $V_{CE} = 900\text{ V}$ $T_{case} = 125\text{ °C}$ for <b>BUW34</b> $V_{CE} = 500\text{ V}$ for <b>BUW35</b> $V_{CE} = 800\text{ V}$ for <b>BUW36</b> $V_{CE} = 900\text{ V}$			500 500 500	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$
$I_{EBO}$	Emitter Cutoff Current ( $I_C = 0$ )	$V_{EB} = 7\text{ V}$			1	mA
$V_{CEO(sus)}$ *	Collector-emitter Sustaining Voltage ( $I_C = 0$ )	$I_C = 100\text{ mA}$ for <b>BUW34</b> for <b>BUW35</b> for <b>BUW36</b>	400 400 450			V V V
$V_{CE(sat)}$ *	Collector-emitter Saturation Voltage	All Types $I_C = 5\text{ A}$ $I_B = 1\text{ A}$ for <b>BUW35</b> $I_C = 8\text{ A}$ $I_B = 2.5\text{ A}$ for <b>BUW36</b> $I_C = 8\text{ A}$ $I_B = 2.5\text{ A}$			1.5 1.5 3	V V V
$V_{BE(sat)}$ *	Base-emitter Saturation Voltage	All Types $I_C = 5\text{ A}$ $I_B = 1\text{ A}$ for <b>BUW35</b> $I_C = 8\text{ A}$ $I_B = 2.5\text{ A}$ for <b>BUW36</b> $I_C = 8\text{ A}$ $I_B = 2.5\text{ A}$			1.5 1.8 1.8	V V V

**RESISTIVE SWITCHING TIMES** (see fig. 1)

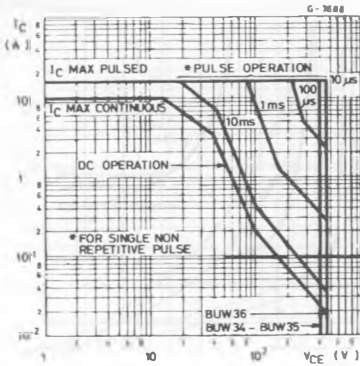
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on Time	$I_C = 5\text{ A}$ , $I_{B1} = 1\text{ A}$ , $V_{CC} = 250\text{ V}$			0.70	$\mu\text{s}$
$t_s$	Storage Time	$I_C = 5\text{ A}$ , $I_{B1} = 1\text{ A}$ , $V_{CC} = 250\text{ V}$			3	$\mu\text{s}$
$t_f$	Fall Time	$I_{B2} = -1\text{ A}$			0.8	$\mu\text{s}$

**INDUCTIVE SWITCHING TIMES** (see fig. 2)

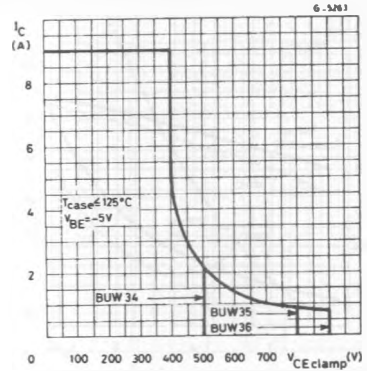
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_f$	Fall Time	$I_C = 5\text{ A}$ $I_{B1} = 1\text{ A}$ $V_{BE} = -5\text{ V}$ $V_{CC} = 300\text{ V}$ $T_{case} = 100\text{ °C}$ $I_C = 5\text{ A}$ $I_{B1} = 1\text{ A}$ $V_{BE} = -5\text{ V}$ $V_{CC} = 300\text{ V}$			0.3 0.6	$\mu\text{s}$ $\mu\text{s}$

\* Pulsed : pulse duration  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 1.5\%$ .

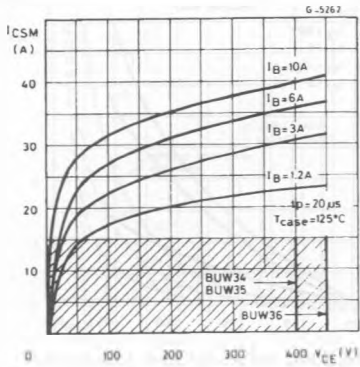
Safe Operating Areas.



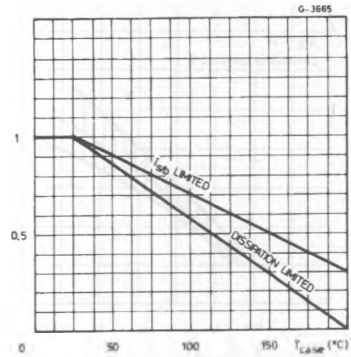
Clamped Reverse Bias Safe Operating Areas.



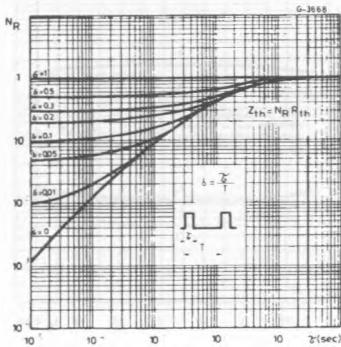
Forward Biased Accidental Overload Area (see fig. 3).



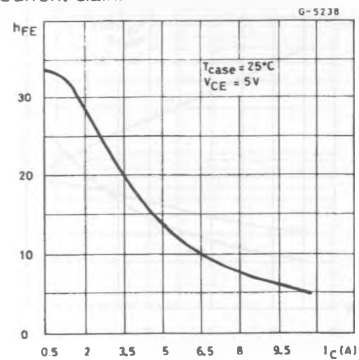
Derating Curves.



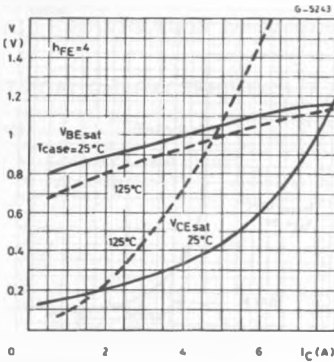
Transient Thermal Response.



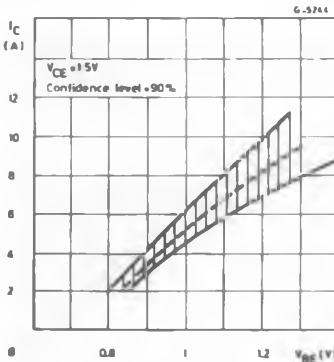
DC Current Gain.



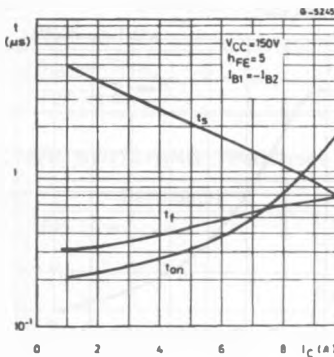
Saturation Voltages.



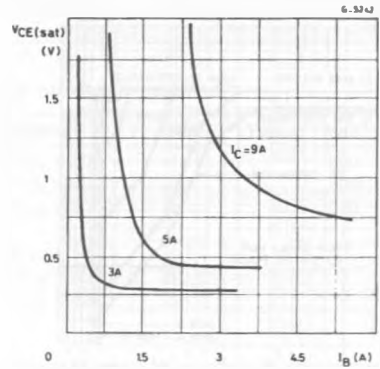
Collector Current Spread vs. Base Emitter Voltage.



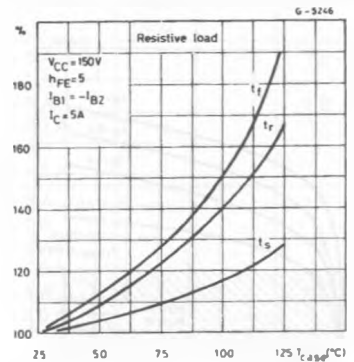
Switching Times Resistive Load (see fig. 1).



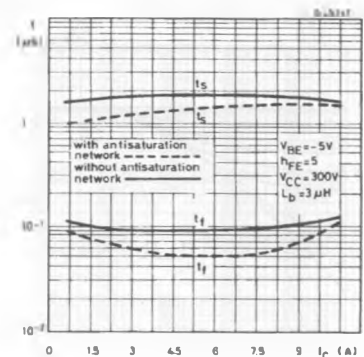
Collector-emitter Saturation Voltage.



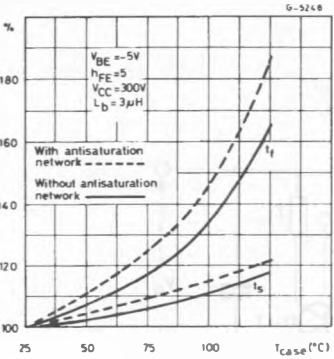
Switching Time Percentage Variation vs. case Temperature.



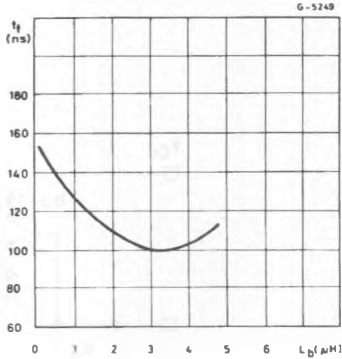
Switching Time Inductive Load (see fig. 2).



Switching Time Inductive Load vs. Case Temperature.



Fall Times vs.  $L_B$  (see fig. 2).



Dynamic Collector-emitter Saturation Voltage (see fig. 4).

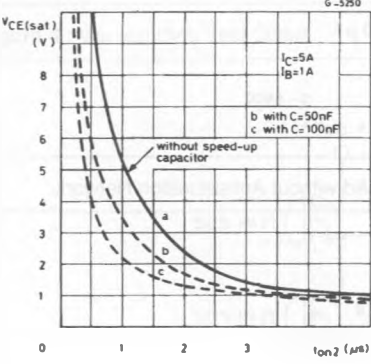


Figure 1 : Switching Times Test Circuit on resistive Load.

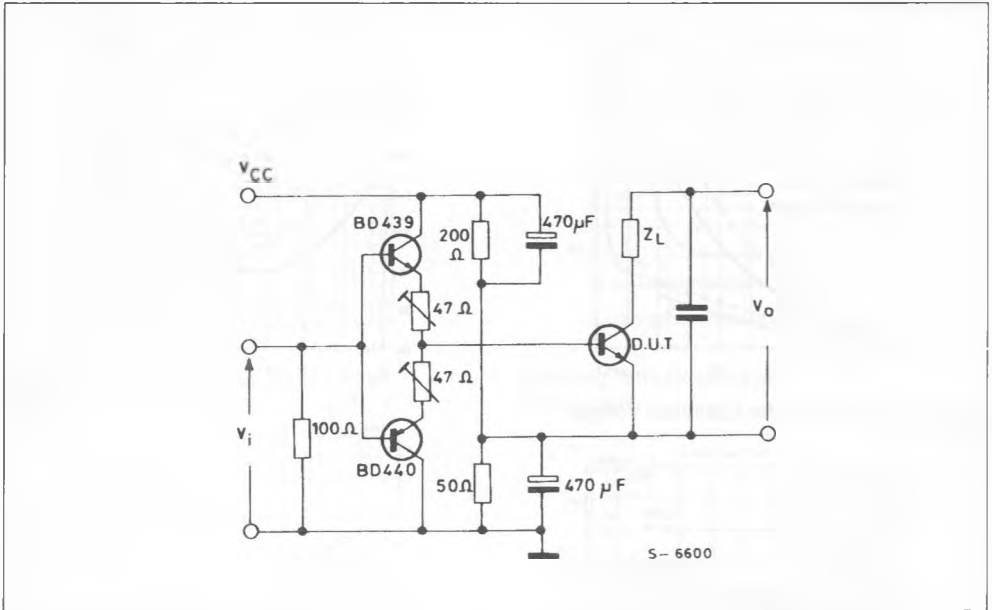


Figure 2 : Switching Times Test Circuit on Inductive Load with Ad without Antisaturation Network.

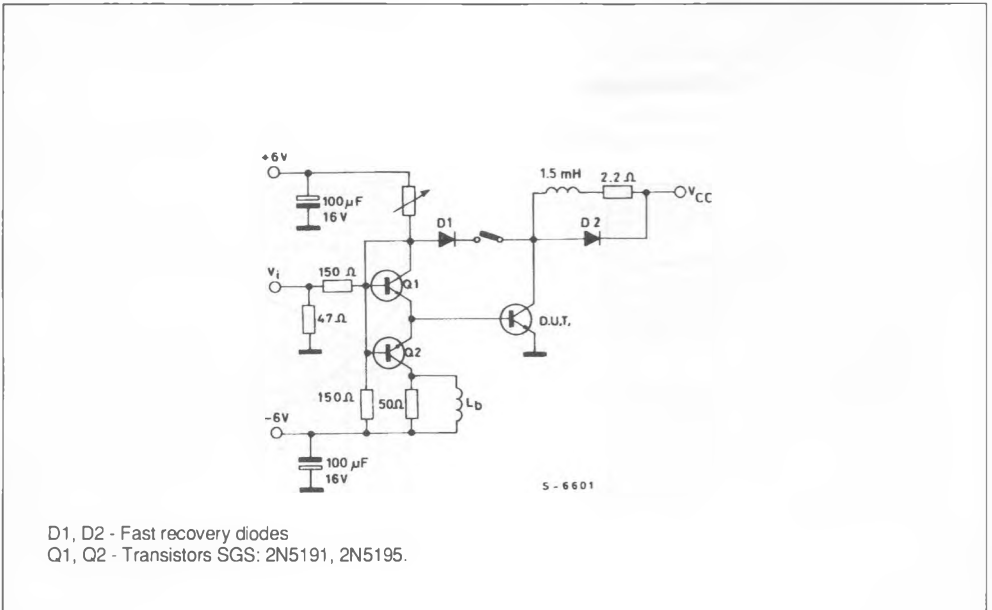


Figure 3 : Forward Biased Accidental Over Load Area Test Circuit.

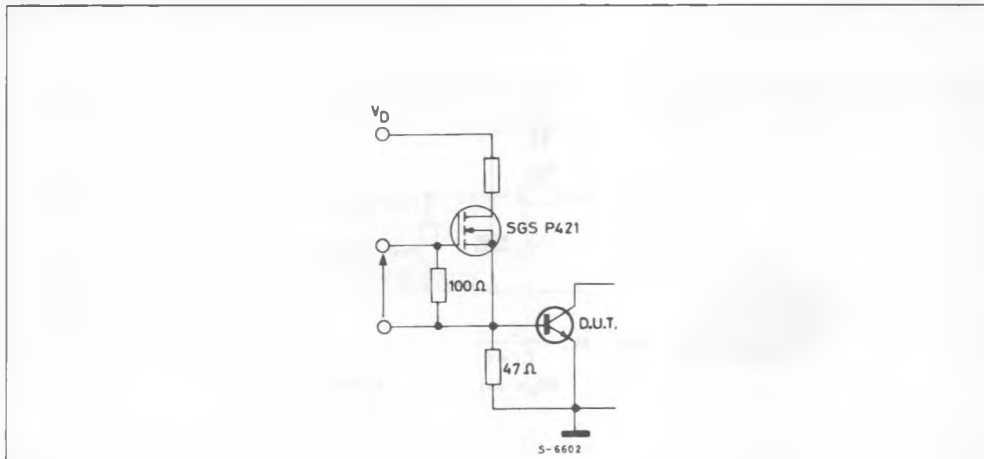


Figure 4 :  $V_{CE(sat)}$  Dyn. Test Circuit.

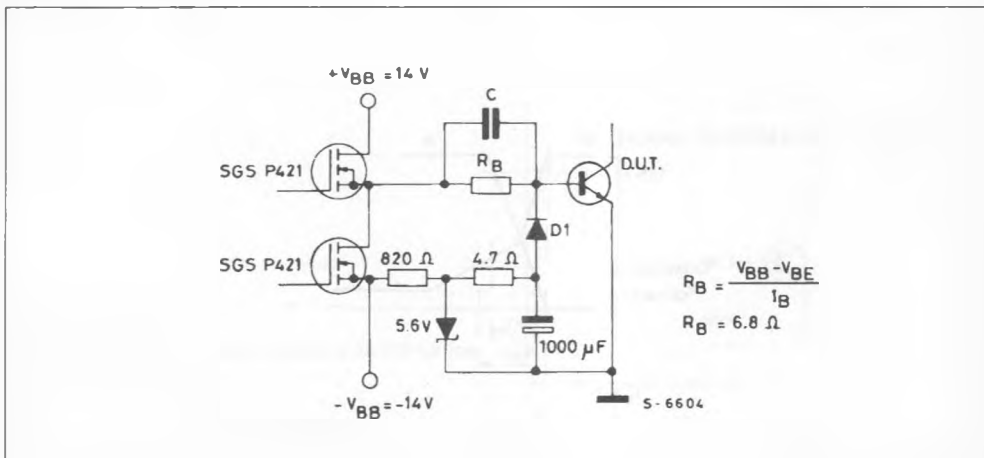


Figure 5 : Equivalent Input Schematic at Turn-on.

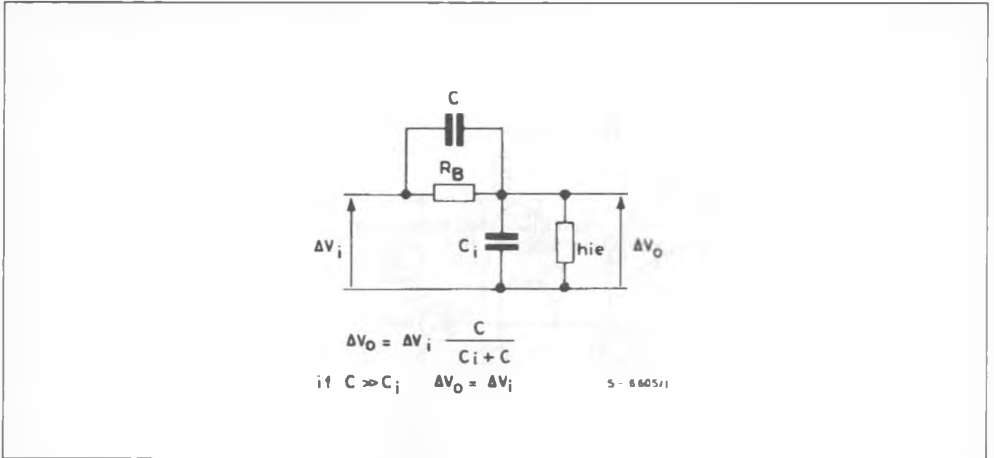
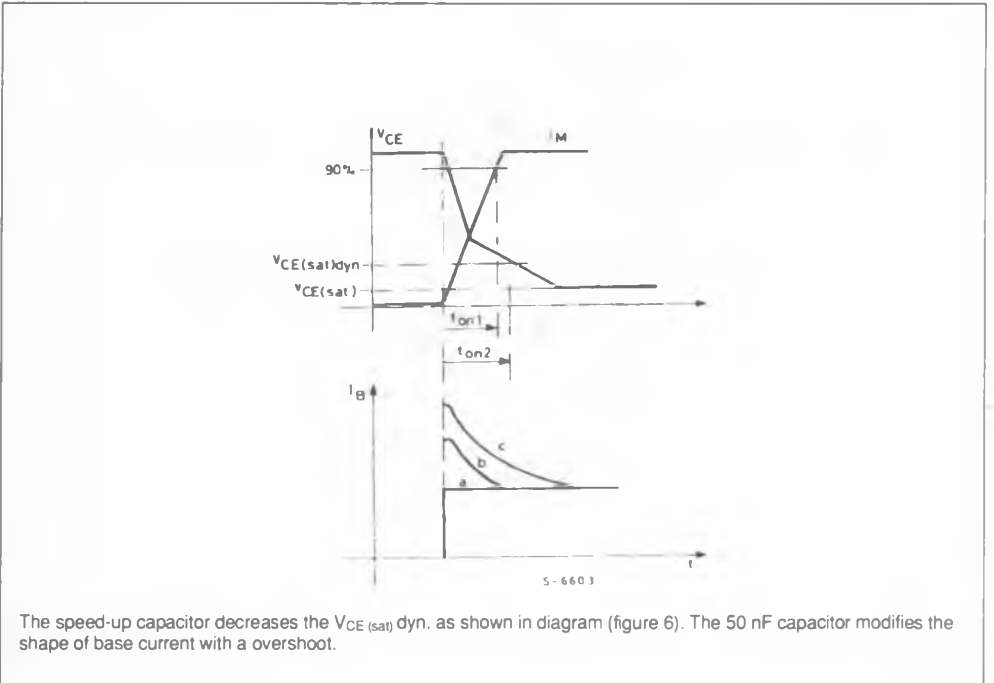


Figure 6 : Remarks to  $V_{CE(sat)}$  Dyn. Test Circuit (fig. 4).



The speed-up capacitor decreases the  $V_{CE(sat)}$  dyn. as shown in diagram (figure 6). The 50 nF capacitor modifies the shape of base current with an overshoot.