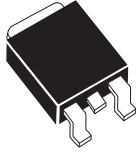


**CJD13003**  
**NPN SILICON**  
**POWER TRANSISTOR**

**DPAK**  
**POWER!**



**DPAK TRANSISTOR CASE**

# Central<sup>TM</sup>

**Semiconductor Corp.**

**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CJD13003 type is an NPN Silicon Power Transistor manufactured in a surface mount package designed for high voltage, high speed power switching inductive applications.

**MARKING CODE: FULL PART NUMBER**

**MAXIMUM RATINGS:** ( $T_C=25^\circ\text{C}$  unless otherwise noted)

	<b>SYMBOL</b>		<b>UNITS</b>
Collector-Emitter Voltage	$V_{CEV}$	700	V
Collector-Emitter Voltage	$V_{CEO}$	400	V
Emitter-Base Voltage	$V_{EBO}$	9.0	V
Continuous Collector Current	$I_C$	1.5	A
Peak Collector Current	$I_{CM}$	3.0	A
Continuous Base Current	$I_B$	750	mA
Peak Base Current	$I_{BM}$	1.5	A
Continuous Emitter Current	$I_E$	2.25	A
Peak Emitter Current	$I_{EM}$	4.5	A
Power Dissipation	$P_D$	15	W
Power Dissipation ( $T_A=25^\circ\text{C}$ )	$P_D$	1.56	W
Operating and Storage			
Junction Temperature	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$
Thermal Resistance	$\theta_{JC}$	8.33	$^\circ\text{C/W}$
Thermal Resistance	$\theta_{JA}$	80.1	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS:** ( $T_C=25^\circ\text{C}$  unless otherwise noted)

<b>SYMBOL</b>	<b>TEST CONDITIONS</b>	<b>MIN</b>	<b>TYP</b>	<b>MAX</b>	<b>UNITS</b>
$I_{CEV}$	$V_{CE}=700\text{V}, V_{BE(\text{off})}=1.5\text{V}$			100	$\mu\text{A}$
$I_{CEV}$	$V_{CE}=700\text{V}, V_{BE(\text{off})}=1.5\text{V}, T_C=100^\circ\text{C}$			2.0	mA
$I_{EBO}$	$V_{EB}=9.0\text{V}$			1.0	mA
$BV_{CEO}$	$I_C=10\text{mA}$	400			V
$V_{CE(\text{SAT})}$	$I_C=500\text{mA}, I_B=100\text{mA}$			0.5	V
$V_{CE(\text{SAT})}$	$I_C=1.0\text{A}, I_B=250\text{mA}$			1.0	V
$V_{CE(\text{SAT})}$	$I_C=1.5\text{A}, I_B=500\text{mA}$			3.0	V
$V_{CE(\text{SAT})}$	$I_C=1.0\text{A}, I_B=250\text{mA}, T_C=100^\circ\text{C}$			1.0	V
$V_{BE(\text{SAT})}$	$I_C=500\text{mA}, I_B=100\text{mA}$			1.0	V
$V_{BE(\text{SAT})}$	$I_C=1.0\text{A}, I_B=250\text{mA}$			1.2	V
$V_{BE(\text{SAT})}$	$I_C=1.0\text{A}, I_B=250\text{mA}, T_C=100^\circ\text{C}$			1.1	V
$h_{FE}$	$V_{CE}=2.0\text{V}, I_C=500\text{mA}$	8.0		40	
$h_{FE}$	$V_{CE}=2.0\text{V}, I_C=1.0\text{A}$	5.0		25	
$f_T$	$V_{CE}=10\text{V}, I_C=100\text{mA}, f=1.0\text{MHz}$	4.0			MHz
$C_{ob}$	$V_{CB}=10\text{V}, I_E=0, f=0.1\text{MHz}$		20		pF

(1)  $t_p=25\mu\text{s}$ , Duty Cycle $\leq$ 1%

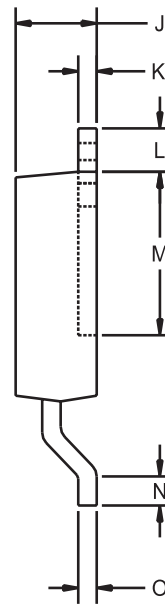
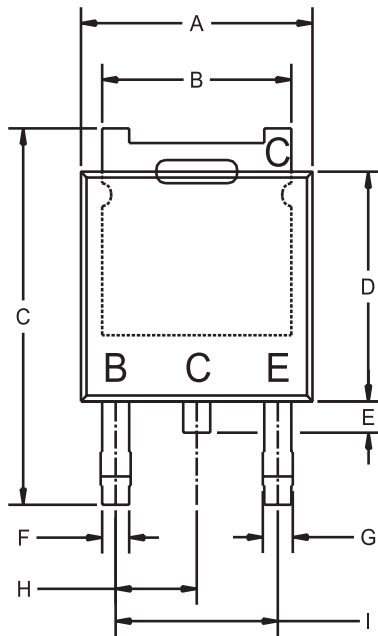
**NPN SILICON  
POWER TRANSISTOR**

**ELECTRICAL CHARACTERISTICS:** ( $T_C=25^\circ\text{C}$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_d$	$V_{CC}=125\text{V}, I_C=1.0\text{A}, I_{B1}=I_{B2}=200\text{mA}$ (1)			0.1	$\mu\text{s}$
$t_r$	$V_{CC}=125\text{V}, I_C=1.0\text{A}, I_{B1}=I_{B2}=200\text{mA}$ (1)			1.0	$\mu\text{s}$
$t_s$	$V_{CC}=125\text{V}, I_C=1.0\text{A}, I_{B1}=I_{B2}=200\text{mA}$ (1)			4.0	$\mu\text{s}$
$t_f$	$V_{CC}=125\text{V}, I_C=1.0\text{A}, I_{B1}=I_{B2}=200\text{mA}$ (1)			0.7	$\mu\text{s}$

(1)  $t_p=25\mu\text{s}$ , Duty Cycles $\leq$ 1%

**DPAK TRANSISTOR CASE - MECHANICAL OUTLINE**



R1

**LEAD CODE:**

- B) BASE
- C) COLLECTOR
- E) EMITTER
- C) COLLECTOR

**MARKING CODE:**

**FULL PART NUMBER**

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.250	0.265	6.35	6.73
B	0.205	0.215	5.21	5.46
C	0.374	0.409	9.50	10.40
D	0.235	0.245	5.97	6.22
E	0.025	0.040	0.64	1.02
F	0.025	0.035	0.64	0.88
G	0.030	0.045	0.76	1.14
H	0.090		2.28	
I	0.180		4.57	
J	0.086	0.094	2.19	2.38
K	0.018	0.023	0.46	0.58
L	0.040	0.050	1.02	1.27
M	0.170	-	4.32	-
N	0.020	-	0.51	-
O	0.018	0.023	0.46	0.58

DPAK TRANSISTOR (REV: R1)

R1 (26-August 2002)