

N-Channel NexFET™ Power MOSFETs

 Check for Samples: [CSD16325Q5](#)

FEATURES

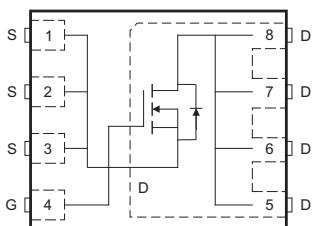
- Optimized for 5V Gate Drive
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm x 6-mm Plastic Package

APPLICATIONS

- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications and optimized for 5V gate drive applications.

Top View


P0094-01

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25	V
Q_g	Gate Charge Total (4.5V)	18	nC
Q_{gd}	Gate Charge Gate to Drain	3.5	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	2.1 mΩ
		$V_{GS} = 4.5V$	1.7 mΩ
		$V_{GS} = 8V$	1.5 mΩ
$V_{GS(th)}$	Threshold Voltage	1.1	V

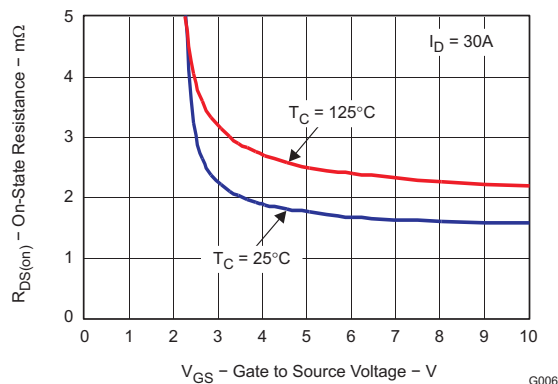
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16325Q5	SON 5-mm x 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

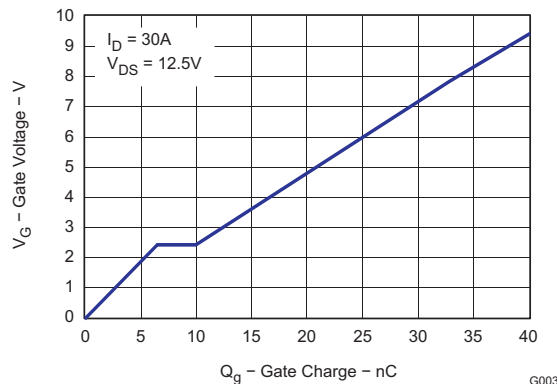
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / -8	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current ⁽¹⁾	33	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	200	A
P_D	Power Dissipation ⁽¹⁾	3.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 100A, L = 0.1mH, R_G = 25\Omega$	500	mJ

- (1) Typical $R_{\theta JA} = 38^\circ\text{C/W}$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.
 (2) Pulse duration $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

 $R_{DS(on)}$ vs V_{GS}


G006

Gate Charge


G003



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25			V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 20V$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10/-8V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V, I_D = 30A$		2.1	2.9	m Ω
		$V_{GS} = 4.5V, I_D = 30A$		1.7	2.2	m Ω
		$V_{GS} = 8V, I_D = 30A$		1.5	2	m Ω
g_{fs}	Transconductance	$V_{DS} = 15V, I_D = 30A$		159		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V,$ $f = 1MHz$		3070	4000	pF
C_{oss}	Output Capacitance			2190	2850	pF
C_{rss}	Reverse Transfer Capacitance			120	150	pF
R_G	Series Gate Resistance			1.6	3.2	Ω
Q_g	Gate Charge Total (4.5V)	$V_{DS} = 12.5V,$ $I_{DS} = 30A$		18	25	nC
Q_{gd}	Gate Charge – Gate to Drain			3.5		nC
Q_{gs}	Gate Charge – Gate to Source			6.6		nC
$Q_{g(th)}$	Gate Charge at V_{th}			3.3		nC
Q_{oss}	Output Charge	$V_{DS} = 13V, V_{GS} = 0V$		43		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 12.5V, V_{GS} = 4.5V,$ $I_{DS} = 30A, R_G = 2\Omega$		10.5		ns
t_r	Rise Time			16		ns
$t_{d(off)}$	Turn Off Delay Time			32		ns
t_f	Fall Time			12		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{DS} = 30A, V_{GS} = 0V$		0.8	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 10V, I_F = 30A, di/dt = 300A/\mu s$		63		nC
t_{rr}	Reverse Recovery Time	$V_{DD} = 10V, I_F = 30A, di/dt = 300A/\mu s$		47		ns

THERMAL CHARACTERISTICS

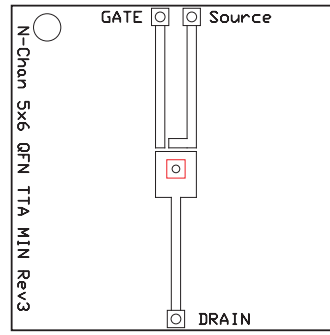
($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^{(1) (2)}			50	$^\circ\text{C/W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.



Max $R_{\theta JA} = 126^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

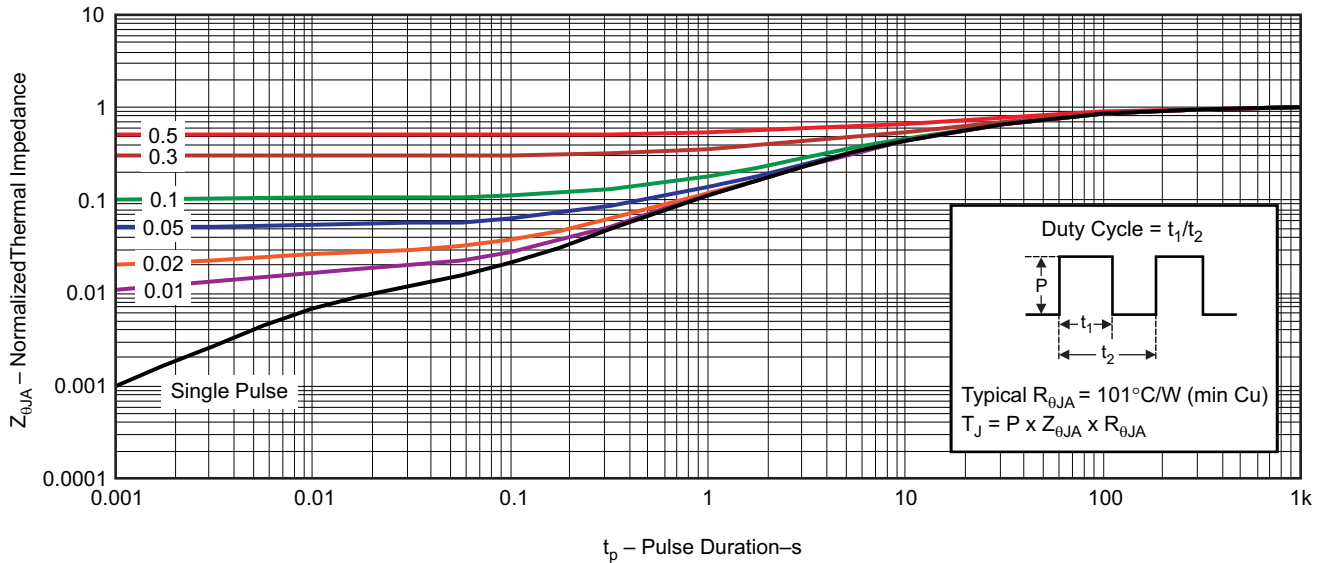


Figure 1. Transient Thermal Impedance

G012

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

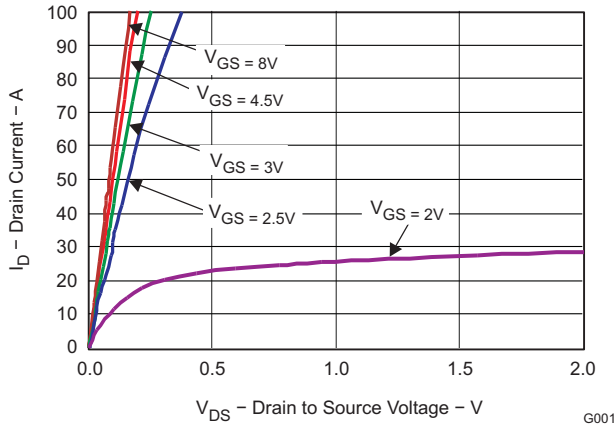


Figure 2. Saturation Characteristics

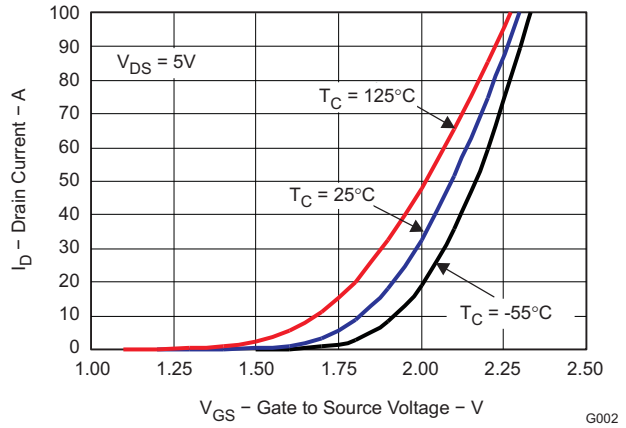


Figure 3. Transfer Characteristics

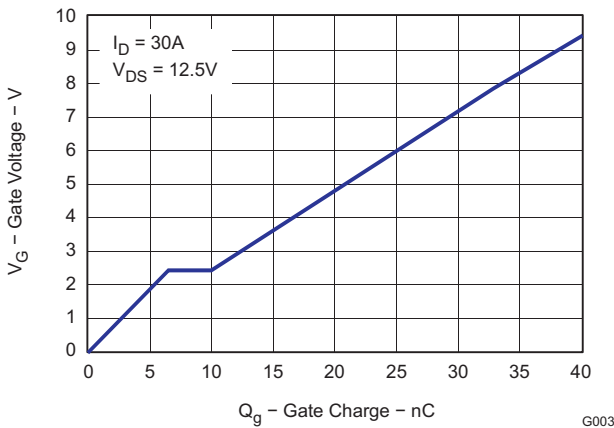


Figure 4. Gate Charge

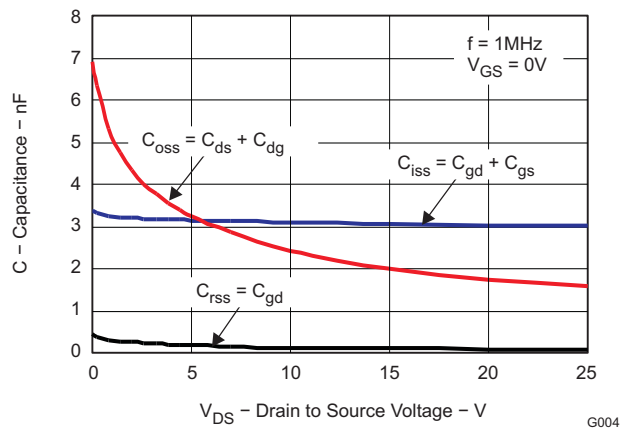


Figure 5. Capacitance

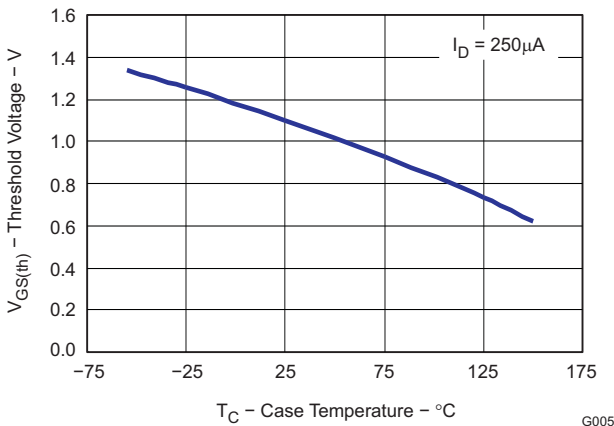


Figure 6. Threshold Voltage vs. Temperature

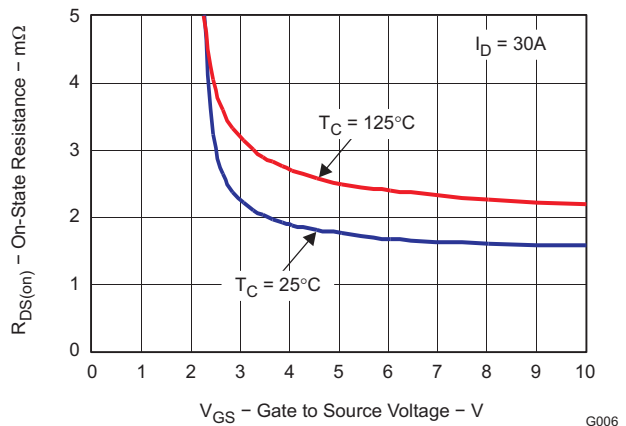


Figure 7. On-State Resistance vs. Gate to Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

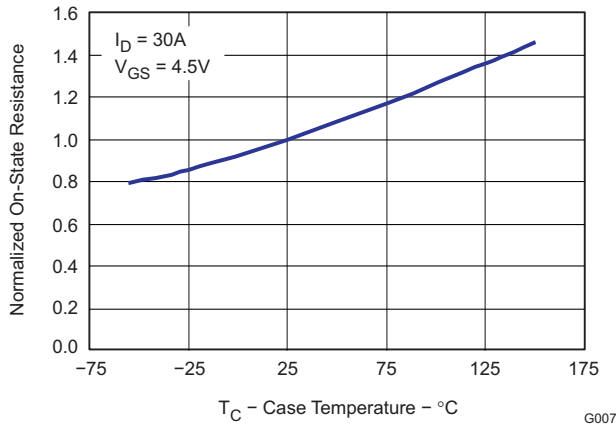


Figure 8. Normalized On-State Resistance vs. Temperature

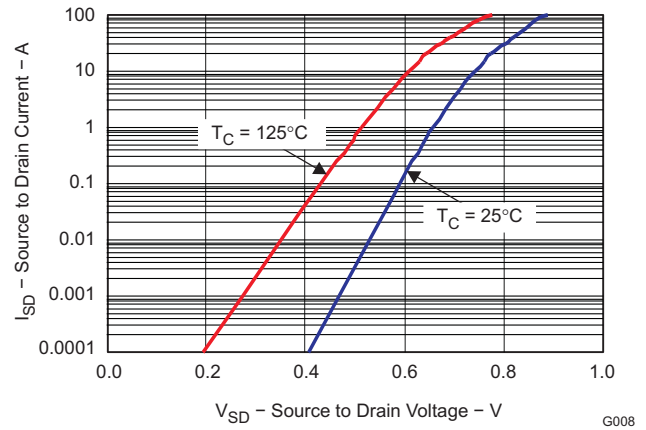


Figure 9. Typical Diode Forward Voltage

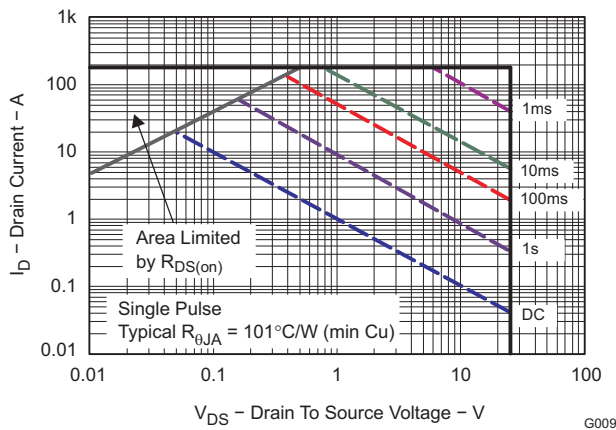


Figure 10. Maximum Safe Operating Area

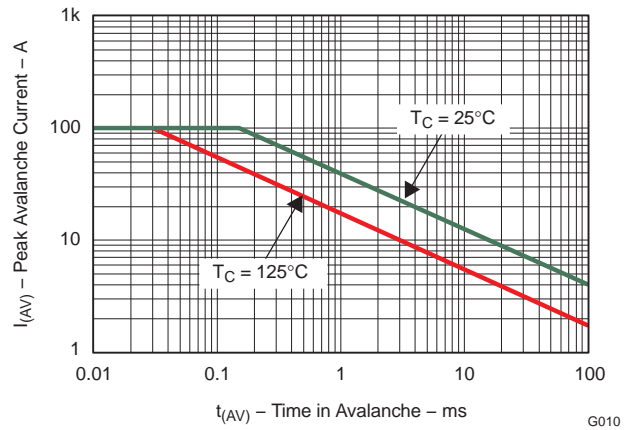


Figure 11. Single Pulse Unclamped Inductive Switching

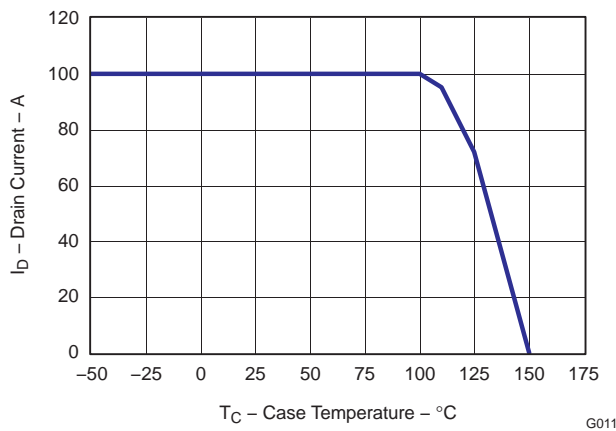
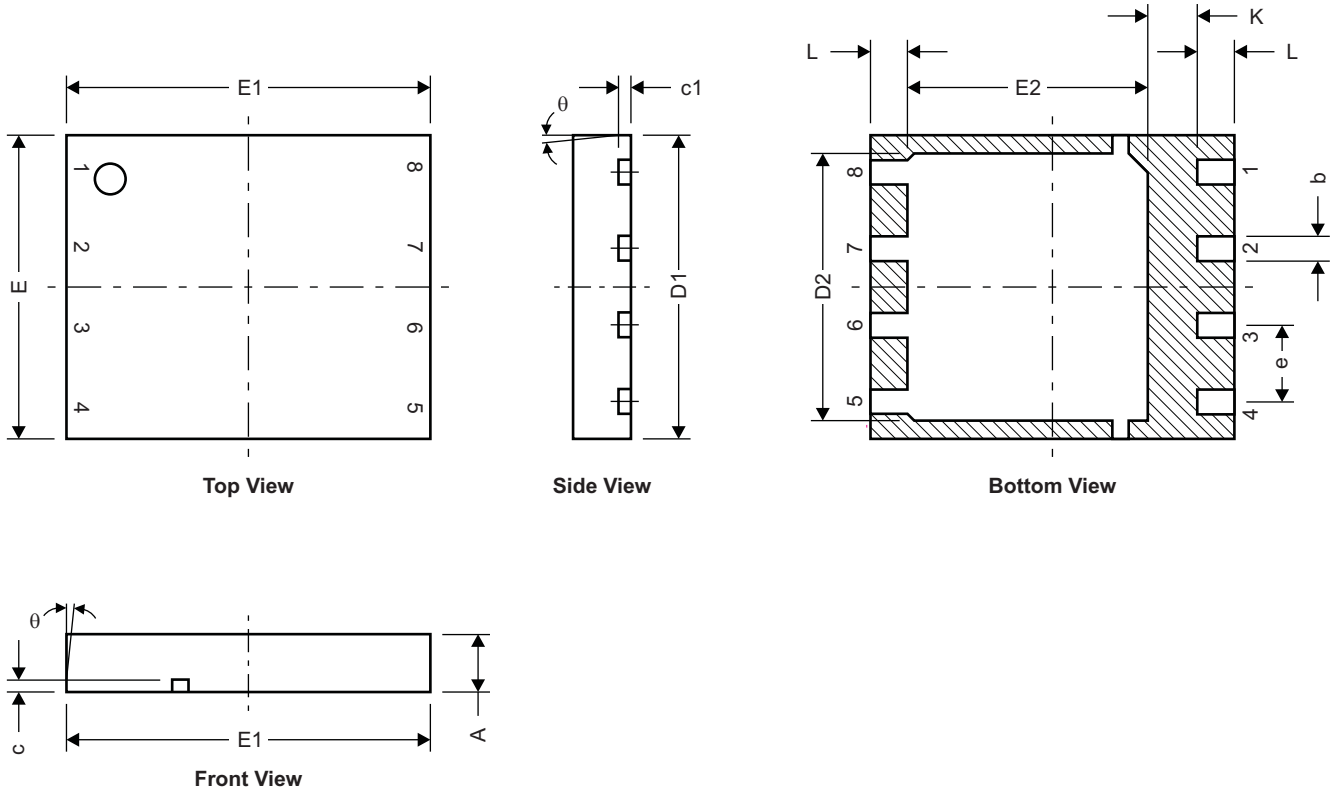


Figure 12. Maximum Drain Current vs. Temperature

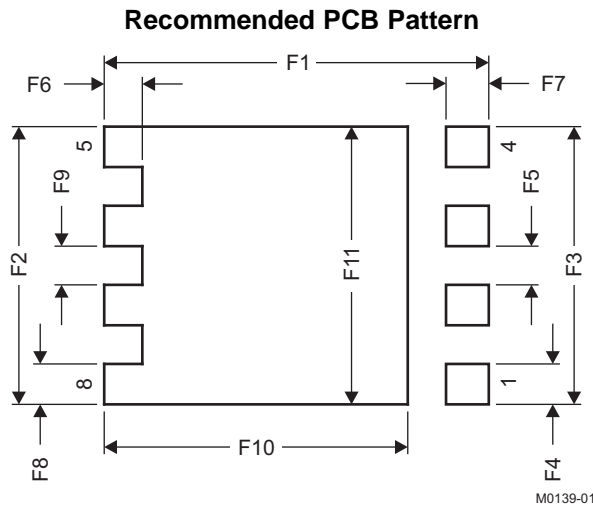
MECHANICAL DATA

Q5 Package Dimensions



M0140-01

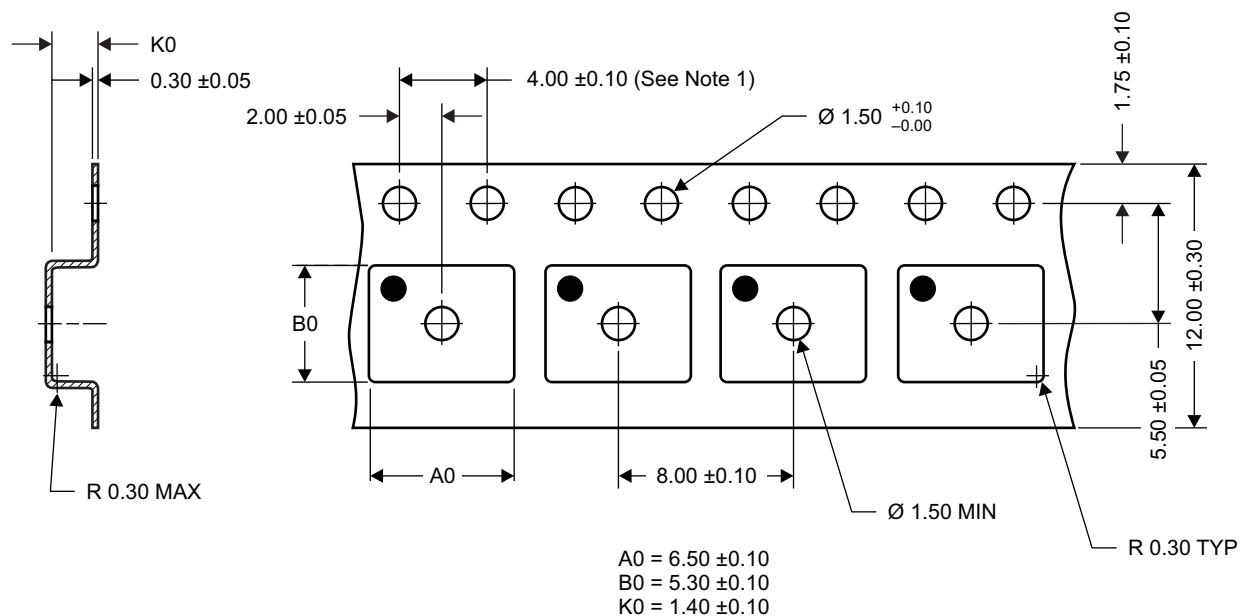
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
L	0.510	0.710	0.020	0.028
θ	0.00			



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q5 Tape and Reel Information



M0138-01

Notes:

- 10-sprocket hole-pitch cumulative tolerance ±0.2
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm, unless otherwise specified.
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
- MSL1 260°C (IR and convection) PbF reflow compatible

REVISION HISTORY

Changes from Original (August 2009) to Revision A Page

- Changed Q_{rr} Reverse Recovery Charge typical value From: 102nC To: 63nC **2**
-

Changes from Revision A (September 2009) to Revision B Page

- Changed Note 1 of the ABSOLUTE MAXIMUM RATINGS From: $R_{\theta JA} = 38^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 38^{\circ}\text{C/W}$ **1**
 - Changed I_{DM} Pulsed Drain Current in the ABSOLUTE MAXIMUM RATINGS From: 210A To: 200A **1**
 - Changed From: Max $R_{\theta JA} = 48^{\circ}\text{C/W}$ To: Max $R_{\theta JA} = 50^{\circ}\text{C/W}$ **3**
 - Changed From: Max $R_{\theta JA} = 113^{\circ}\text{C/W}$ To: Max $R_{\theta JA} = 126^{\circ}\text{C/W}$ **3**
 - Changed [Figure 1](#) text - From: $R_{\theta JA} = 101^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 101^{\circ}\text{C/W}$ **3**
 - Changed [Figure 10](#) text - From: $R_{\theta JA} = 101^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 101^{\circ}\text{C/W}$ **5**
-

Changes from Revision B (April 2010) to Revision C Page

- Changed $R_{DS(on)}$ - $V_{GS} = 3\text{V}$ in the Electrical Characteristics table From: 2.7 to 2.9 in the max column **2**
 - Deleted the Package Marking Information section **7**
-

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16325Q5	SON	DQH	8	2500	330.0	12.8	6.5	5.3	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

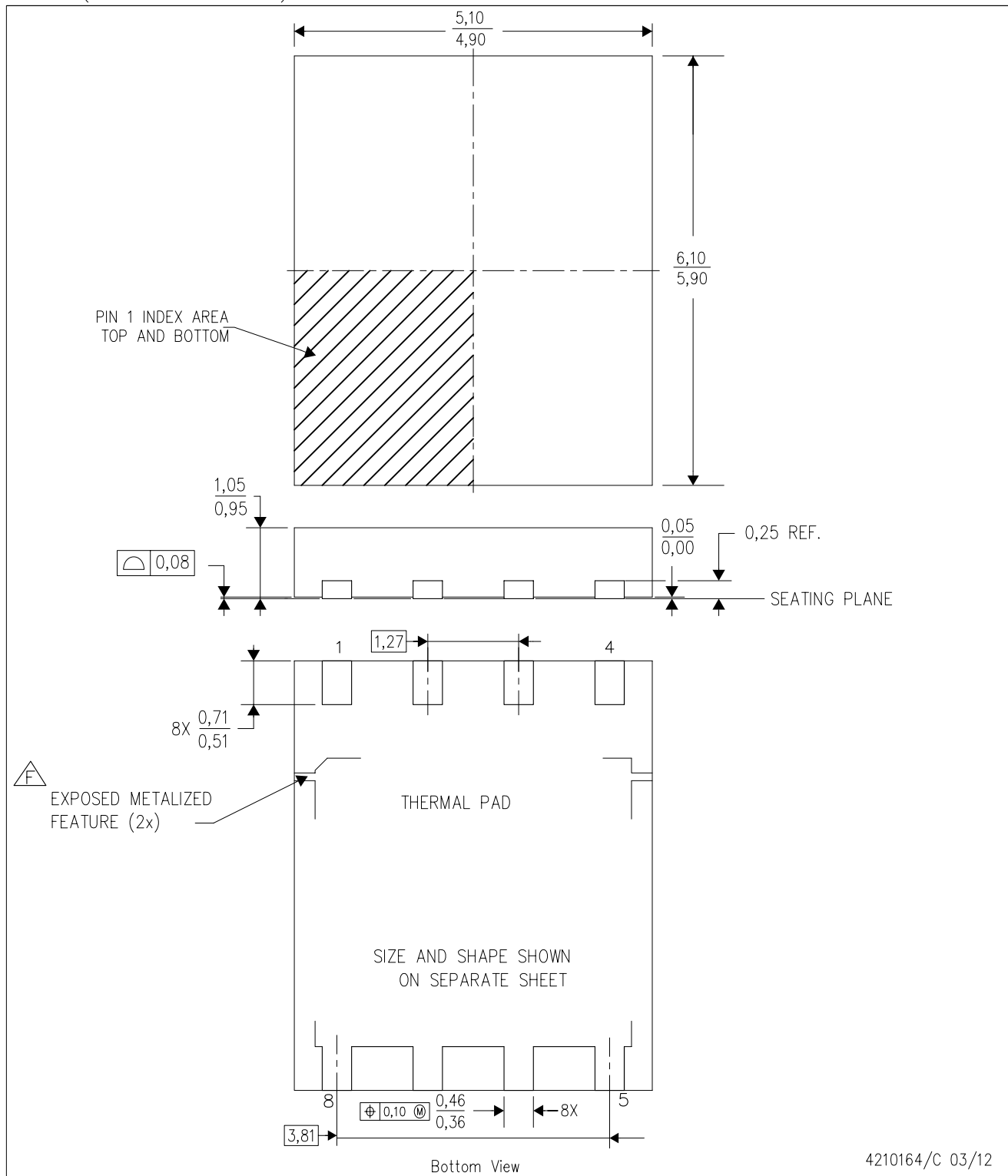


*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16325Q5	SON	DQH	8	2500	335.0	335.0	32.0

DQH (R-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4210164/C 03/12

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
-  Metalized features are supplier options and may not be on the package.

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