

# N-Channel NexFET™ Power MOSFETs

 Check for Samples: [CSD16410Q5A](#)

## FEATURES

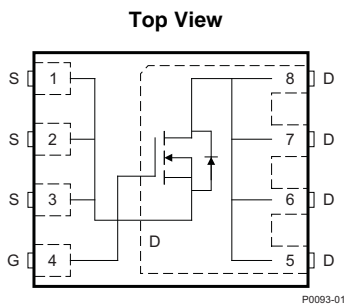
- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5mm x 6mm Plastic Package

## APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

## DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.



## PRODUCT SUMMARY

$V_{DS}$	Drain to Source Voltage	25	V
$Q_g$	Gate Charge Total (4.5V)	3.9	nC
$Q_{gd}$	Gate Charge Gate to Drain	1.1	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V$	9.6 mΩ
		$V_{GS} = 10V$	6.8 mΩ
$V_{GS(th)}$	Threshold Voltage	1.9	V

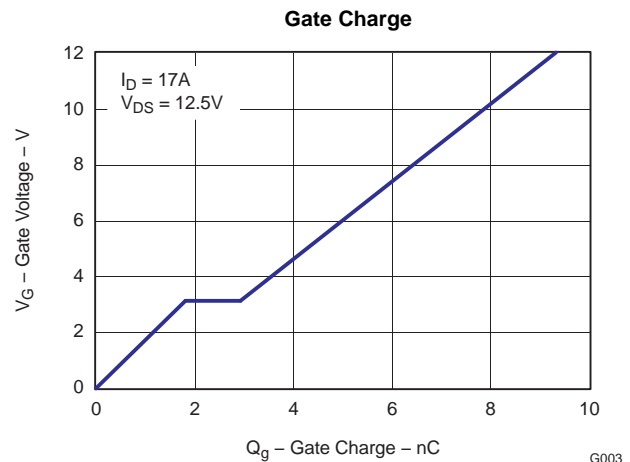
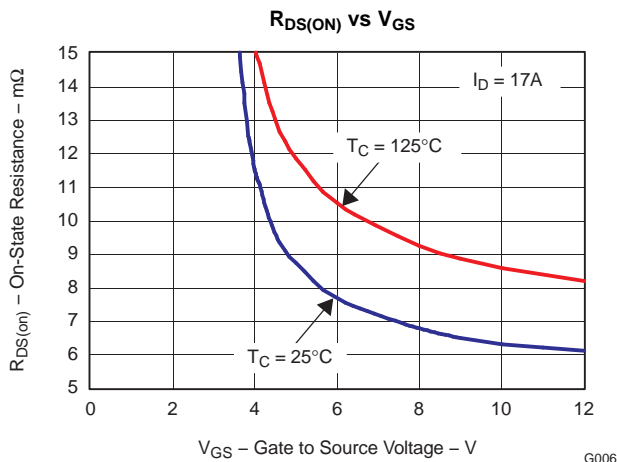
## ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16410Q5A	SON 5X6 Plastic Package	13-inch reel	2500	Tape and Reel

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	+16 / -12	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	59	A
	Continuous Drain Current <sup>(1)</sup>	16	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	158	A
$P_D$	Power Dissipation <sup>(1)</sup>	3	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 32A, L = 0.1mH, R_G = 25\Omega$	51	mJ

- (1)  $R_{\theta JA} = 42^\circ\text{C/W}$  on  $1\text{in}^2$  Cu (2 oz.) on 0.060" thick FR4 PCB.  
 (2) Pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

(T<sub>A</sub> = 25°C unless otherwise stated)

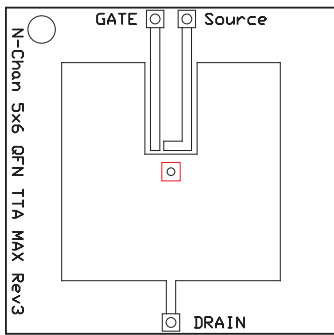
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
B <sub>V</sub> DSS	Drain to Source Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	25			V
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 20V			1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = +16/-12V			100	nA
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.6	1.9	2.3	V
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 17A		9.6	12	mΩ
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 17A		6.8	8.5	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 15V, I <sub>D</sub> = 17A		38		S
<b>Dynamic Characteristics</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 12.5V, f = 1MHz		570	740	pF
C <sub>OSS</sub>	Output Capacitance			460	600	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			40	52	pF
R <sub>g</sub>	Series Gate Resistance	V <sub>DS</sub> = 12.5V, I <sub>D</sub> = 17A		0.7	1.4	Ω
Q <sub>g</sub>	Gate Charge Total (4.5V)			3.9	5	nC
Q <sub>gd</sub>	Gate Charge Gate to Drain			1.1		nC
Q <sub>gs</sub>	Gate Charge Gate to Source			1.8		nC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>			1.1		nC
Q <sub>OSS</sub>	Output Charge	V <sub>DS</sub> = 13V, V <sub>GS</sub> = 0V		10		nC
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = 12.5V, V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 17A R <sub>G</sub> = 2Ω		6.2		ns
t <sub>r</sub>	Rise Time			10.7		ns
t <sub>d(off)</sub>	Turn Off Delay Time			6.5		ns
t <sub>f</sub>	Fall Time			3.6		ns
<b>Diode Characteristics</b>						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> = 17A, V <sub>GS</sub> = 0V		0.85	1	V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DD</sub> = 13V, I <sub>F</sub> = 17A, di/dt = 300A/μs		14		nC
t <sub>rr</sub>	Reverse Recovery Time	V <sub>DD</sub> = 13V, I <sub>F</sub> = 17A, di/dt = 300A/μs		18.2		ns

## THERMAL CHARACTERISTICS

(T<sub>A</sub> = 25°C unless otherwise stated)

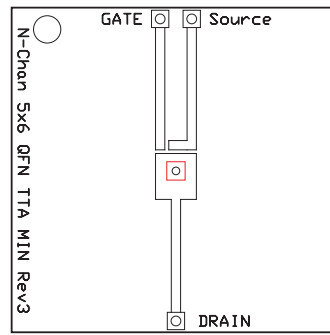
PARAMETER		MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Thermal Resistance Junction to Case <sup>(1)</sup>			3.8	°C/W
R <sub>θJA</sub>	Thermal Resistance Junction to Ambient <sup>(1) (2)</sup>			52	°C/W

- (1) R<sub>θJC</sub> is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 × 1.5 in 0.060 inch thick FR4 board. R<sub>θJC</sub> is specified by design while R<sub>θJA</sub> is determined by the user's board design.  
(2) Device mounted on FR4 Material with 1 inch<sup>2</sup> of 2 oz. Cu.



Max  $R_{\theta JA} = 52^{\circ}\text{C/W}$   
when mounted on 1  
 $\text{inch}^2$  of 2 oz. Cu.

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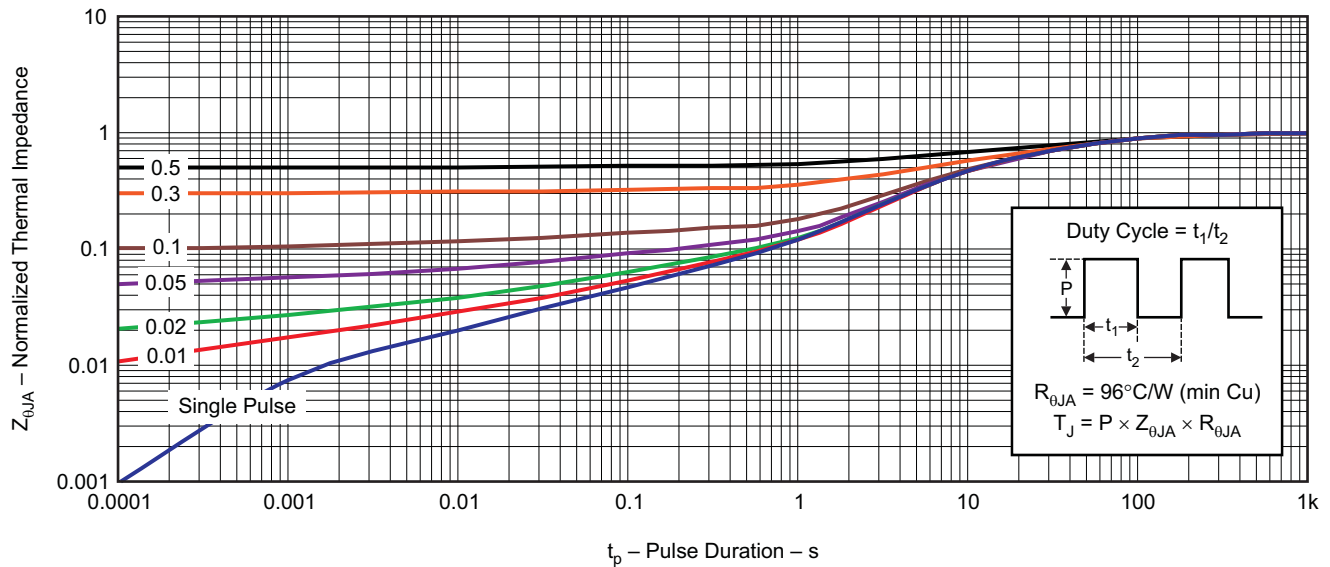


Max  $R_{\theta JA} = 121^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of 2  
oz. Cu.

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### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

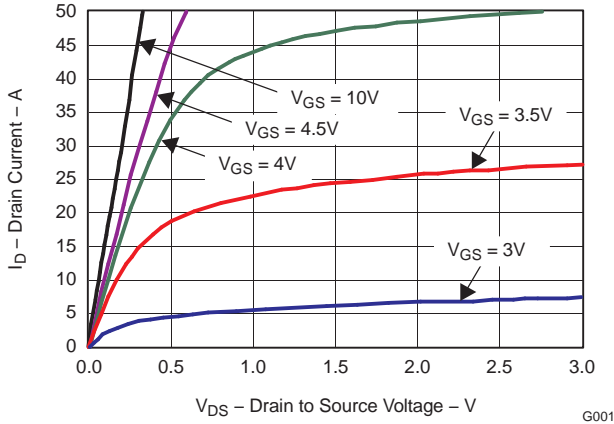


G012

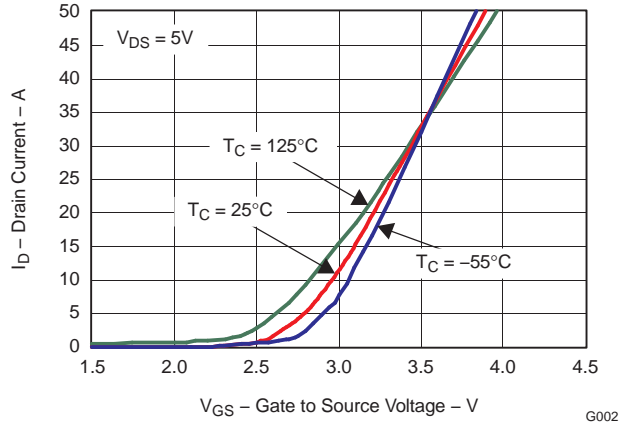
Figure 1. Transient Thermal Impedance

**TYPICAL MOSFET CHARACTERISTICS (continued)**

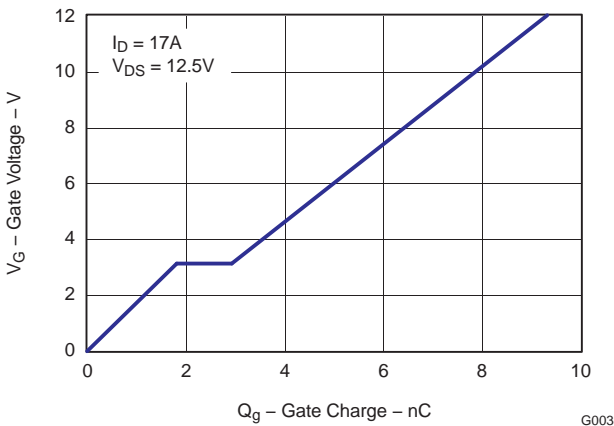
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



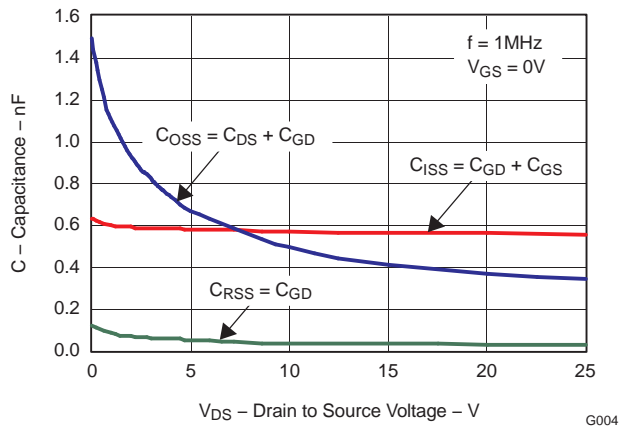
**Figure 2. Saturation Characteristics**



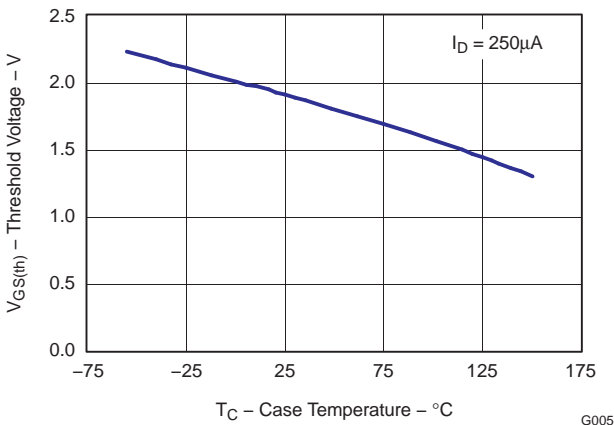
**Figure 3. Transfer Characteristics**



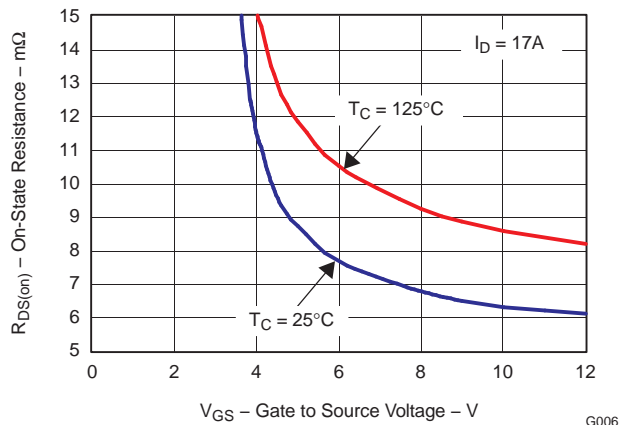
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On Resistance vs. Gate Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

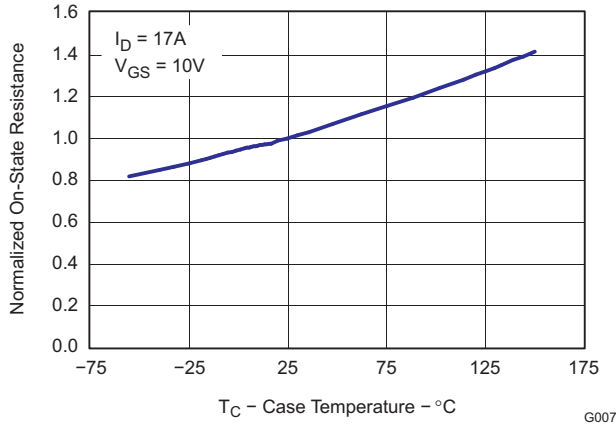


Figure 8. On Resistance vs. Temperature

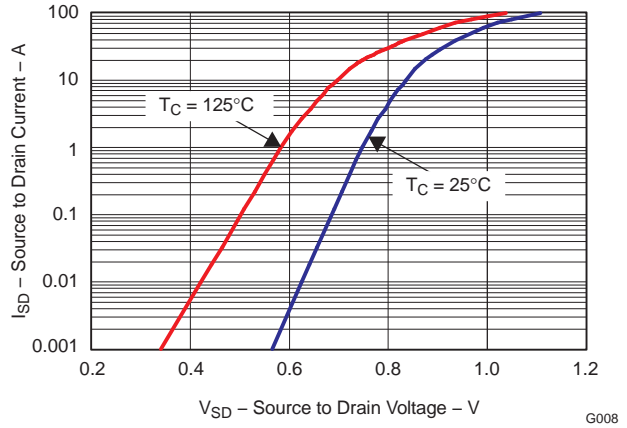


Figure 9. Typical Diode Forward Voltage

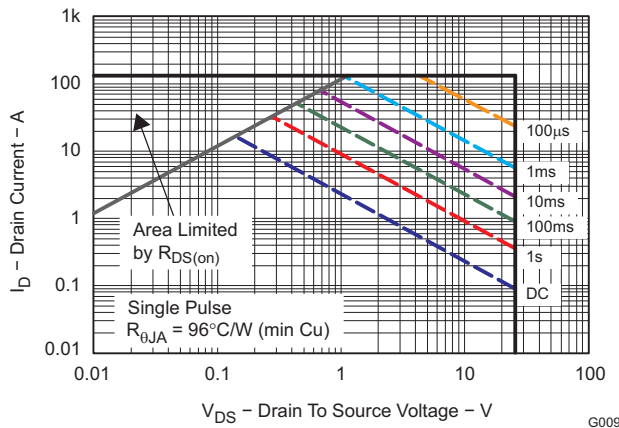


Figure 10. Maximum Safe Operating Area

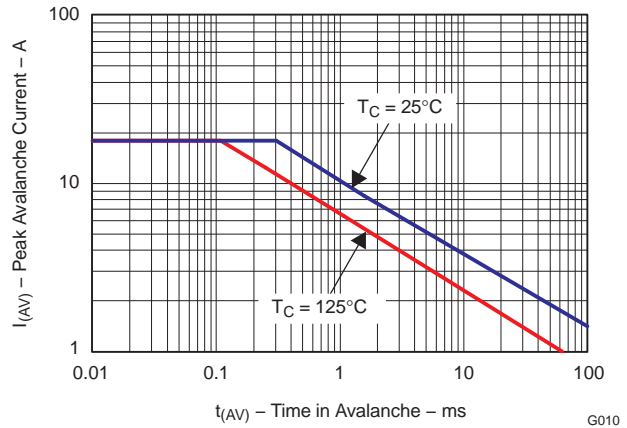


Figure 11. Single Pulse Unclamped Inductive Switching

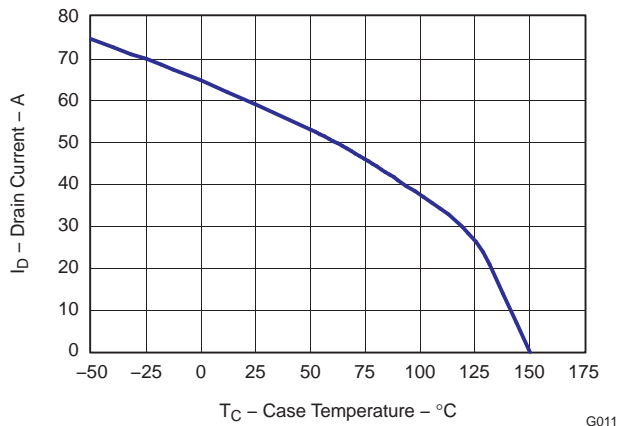
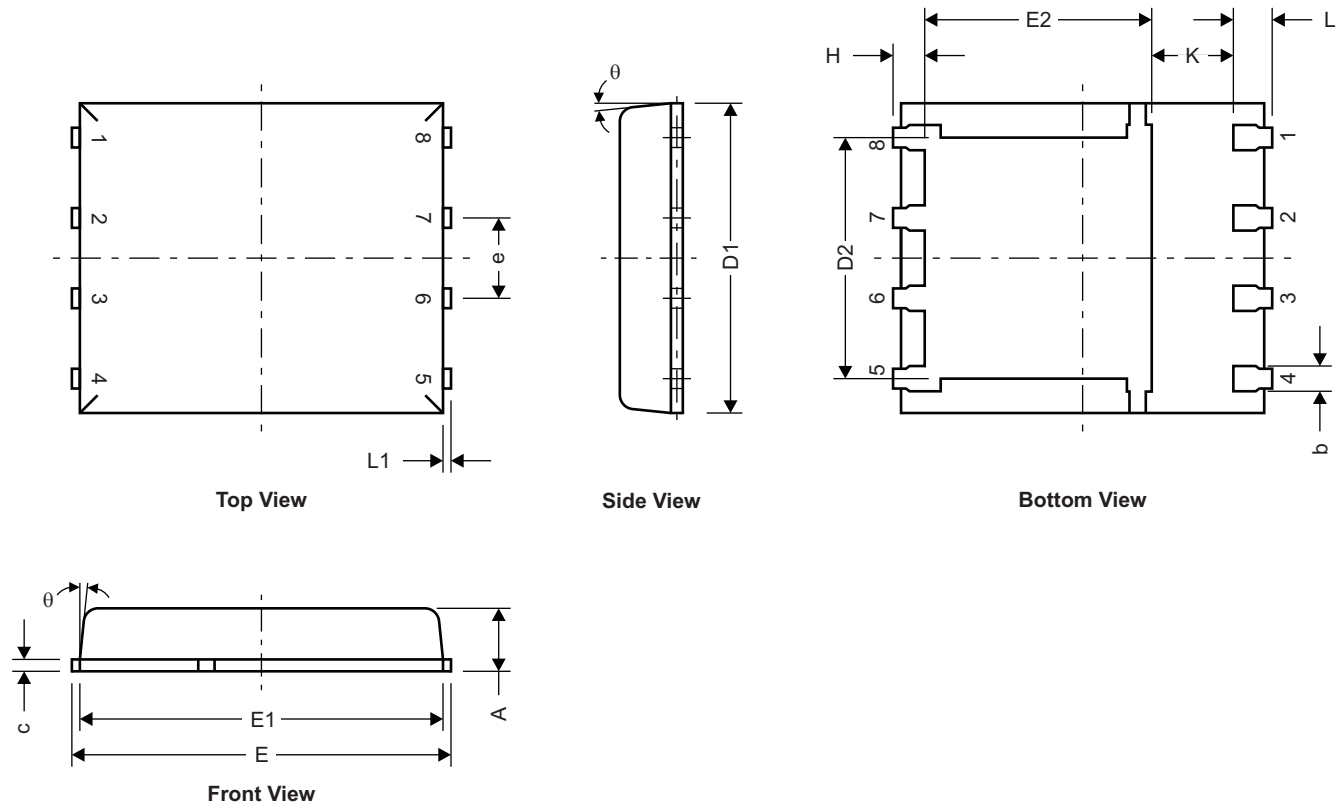


Figure 12. Maximum Drain Current vs. Temperature

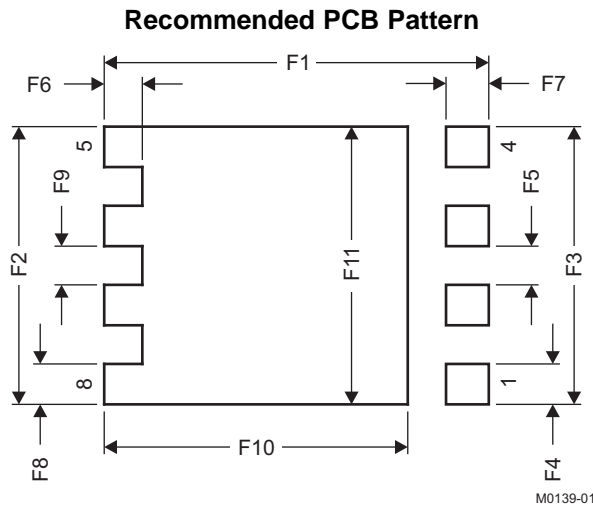
**MECHANICAL DATA**

**Q5A Package Dimensions**



M0135-01

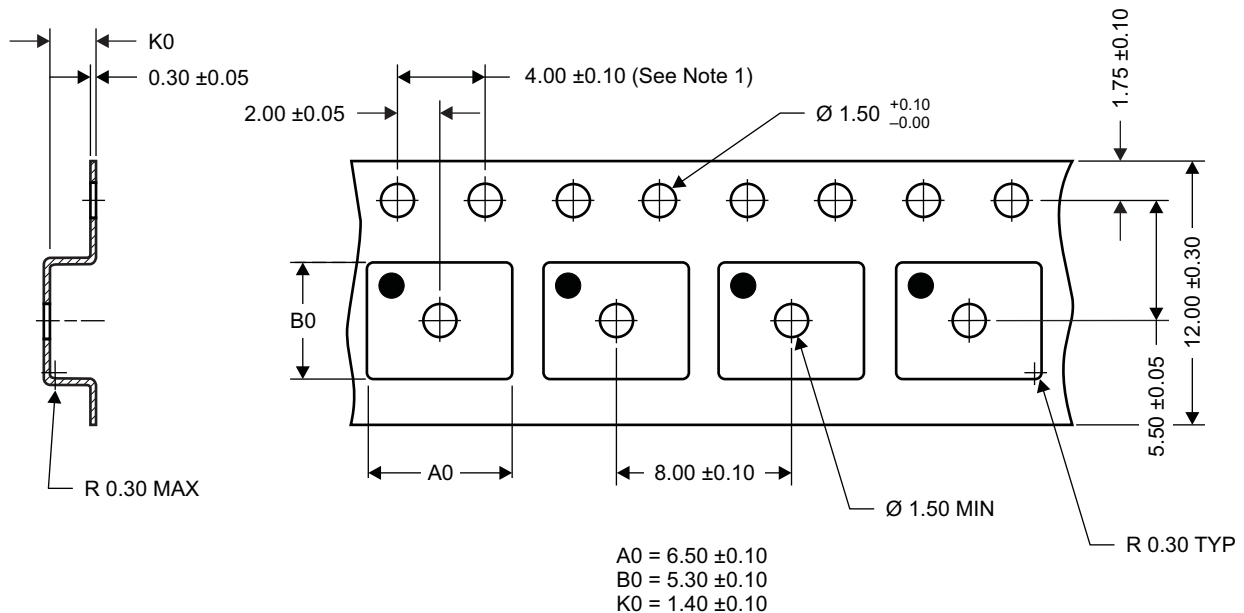
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
$\theta$	0°		12°



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

### Q5A Tape and Reel Information



### Notes:

- 10 sprocket hole pitch cumulative tolerance ±0.2
- Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
- Material: black static dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
- MSL1 260°C (IR and Convection) PbF Reflow Compatible

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## REVISION HISTORY

Changes from Original (August 2009) to Revision A	Page
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- Deleted the Package Marking Information section ..... [7](#)
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### Applications

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