

P-Channel NexFET™ Power MOSFET

 Check for Samples: [CSD25211W1015](#)

FEATURES

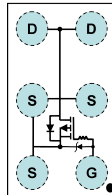
- Ultra Low On Resistance
- Ultra Low Qg and Qgd
- Small Footprint 1.0mm x 1.5mm
- Low Profile 0.62mm Height
- Pb Free
- Gate-Source Voltage Clamp
- Gate ESD Protection - 3KV
- RoHS Compliant
- Halogen Free

APPLICATIONS

- Battery Management
- Load Switch
- Battery Protection

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

Top View


PRODUCT SUMMARY

T _A = 25°C unless otherwise stated		TYPICAL VALUE		UNIT
V _{DS}	Drain to Source Voltage	-20		V
Q _g	Gate Charge Total (-4.5V)	3.4		nC
Q _{gd}	Gate Charge Gate to Drain	0.2		nC
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = -2.5V	36	mΩ
		V _{GS} = -4.5V	27	mΩ
V _{GS(th)}	Voltage Threshold	-0.8		V

ORDERING INFORMATION

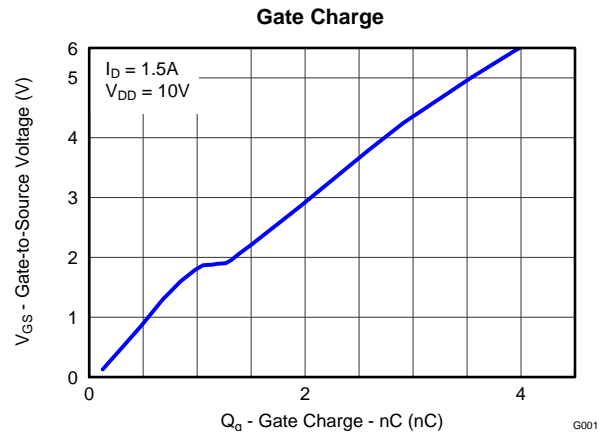
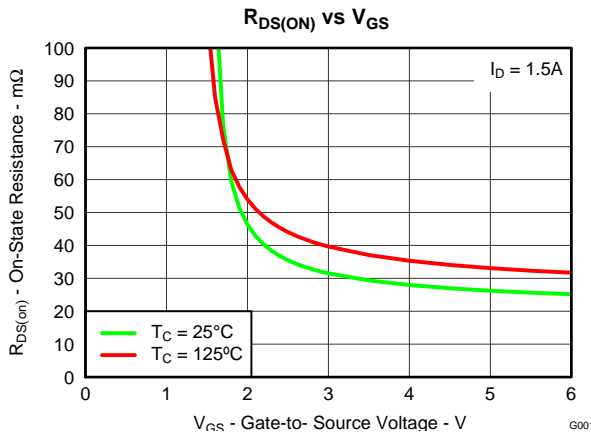
Device	Package	Media	Qty	Ship
CSD25211W1015	1 × 1.5 Wafer Level Package	7-inch reel	3000	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

T _A = 25°C unless otherwise stated		VALUE	UNIT
V _{DS}	Drain to Source Voltage	-20	V
V _{GS}	Gate to Source Voltage	-6	V
I _D	Continuous Drain Current, T _A = 25°C ⁽¹⁾	-3.2	A
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	-9.5	A
I _G	Continuous Drain Current, T _A = 25°C	-0.5	A
	Pulsed Drain Current	-7	A
P _D	Power Dissipation ⁽¹⁾	1	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range		

(1) Typical R_{θJA} = 119°C/W on 1 inch² of 2 oz. Cu on 0.06" thick FR4 PCB.

(2) Pulse width ≤10μs, duty cycle ≤2%



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

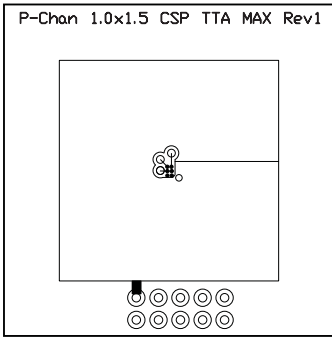
($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
V_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
V_{GSS}	Gate to Source Voltage	$V_{DS} = 0V, I_G = -250\mu A$	-6.1		-7.2	V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = -16V$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = -6V$			-100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.5	-0.8	-1.1	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -2.5V, I_D = -1.5A$		36	44	$m\Omega$
		$V_{GS} = -4.5V, I_D = -1.5A$		27	33	$m\Omega$
g_{fs}	Transconductance	$V_{DS} = -10V, I_D = -1.5A$		12		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = -10V, f = 1MHz$		475	570	pF
C_{OSS}	Output Capacitance			234	281	pF
C_{RSS}	Reverse Transfer Capacitance			10.5	13.1	pF
Q_g	Gate Charge Total (-4.5V)	$V_{DS} = -10V, I_D = -1.5A$		3.4	4.1	nC
Q_{gd}	Gate Charge Gate to Drain			0.2		nC
Q_{gs}	Gate Charge Gate to Source			1.1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.6		nC
Q_{OSS}	Output Charge	$V_{DS} = -10V, V_{GS} = 0V$		3.8		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = -10V, V_{GS} = -4.5V, I_D = -1.5A$ $R_G = 4\Omega$		13.6		ns
t_r	Rise Time			8.8		ns
$t_{d(off)}$	Turn Off Delay Time			36.9		ns
t_f	Fall Time			14.2		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_S = -1.5A, V_{GS} = 0V$		-0.8	-1	V
Q_{rr}	Reverse Recovery Charge	$V_{dd} = -10V, I_F = -1.5A, di/dt = 200A/\mu s$		6.9		nC
t_{rr}	Reverse Recovery Time			11.6		ns

THERMAL CHARACTERISTICS

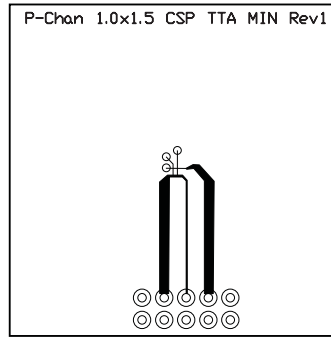
($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Minimum Cu area)			230	$^\circ\text{C/W}$
	Thermal Resistance Junction to Ambient (1 in ² Cu area)			149	$^\circ\text{C/W}$



Max $R_{\theta JA} = 149^{\circ}\text{C/W}$
when mounted on 1
 inch^2 of 2 oz. Cu.

M0155-01



Max $R_{\theta JA} = 230^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

M0156-01

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

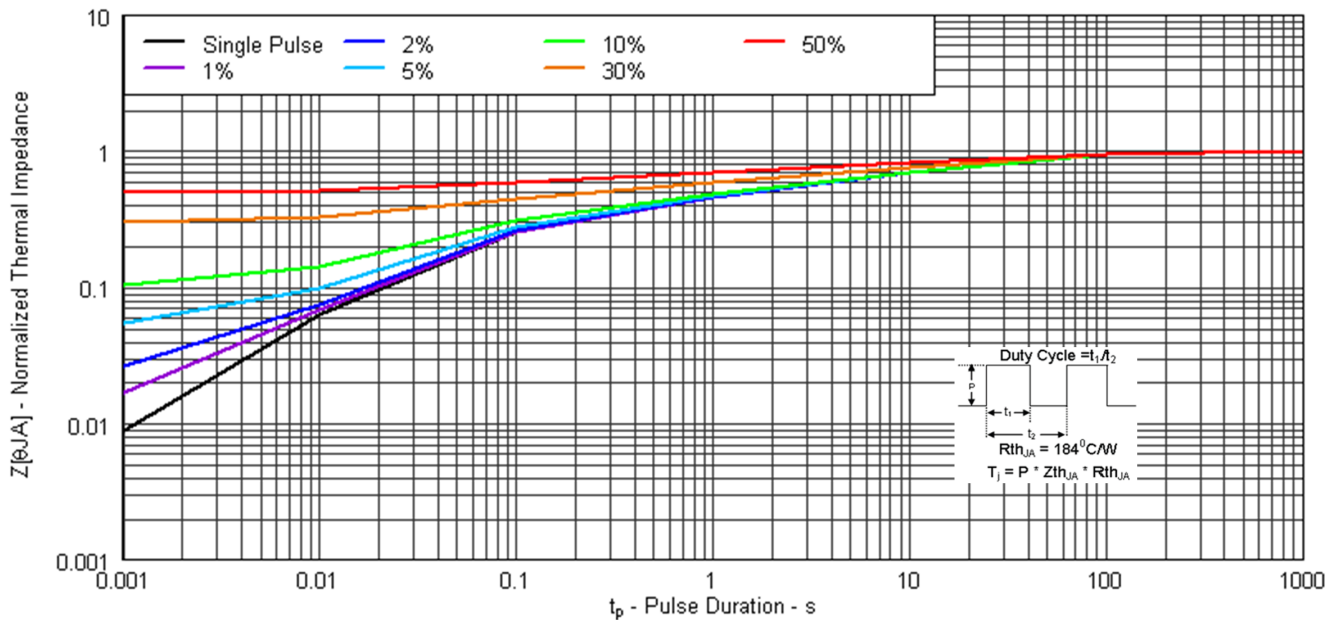


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

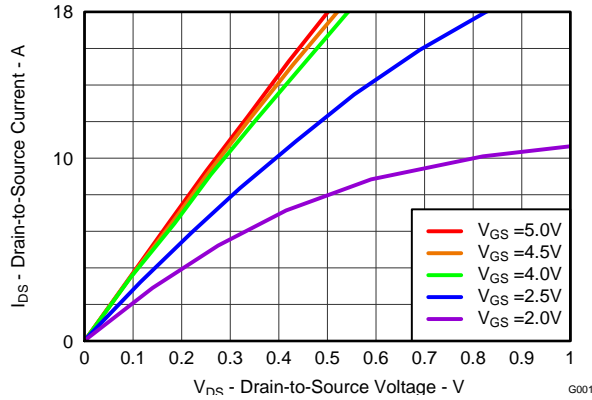


Figure 2. Saturation Characteristics

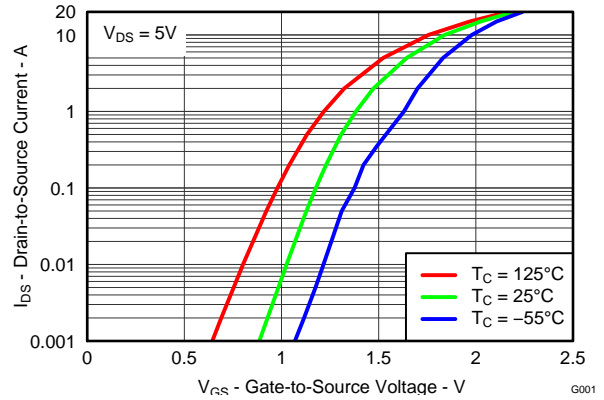


Figure 3. Transfer Characteristics

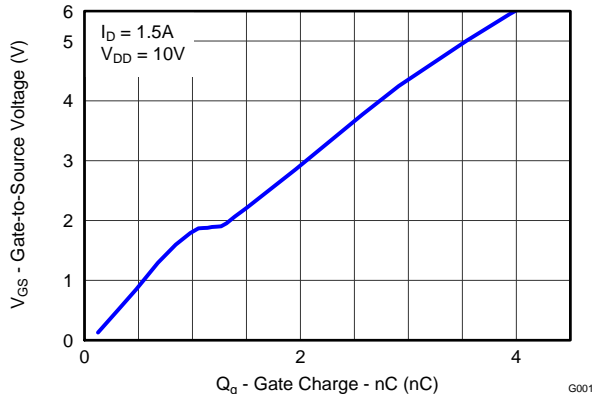


Figure 4. Gate Charge

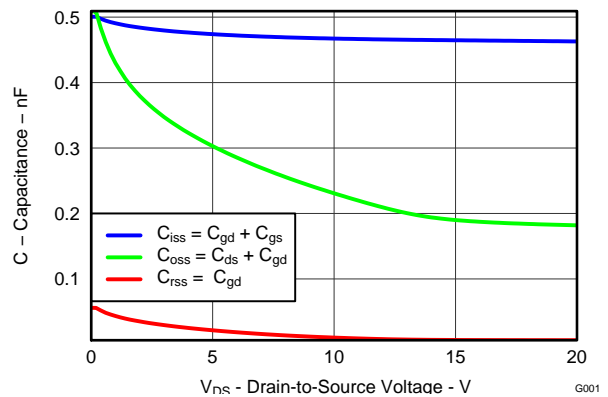


Figure 5. Capacitance

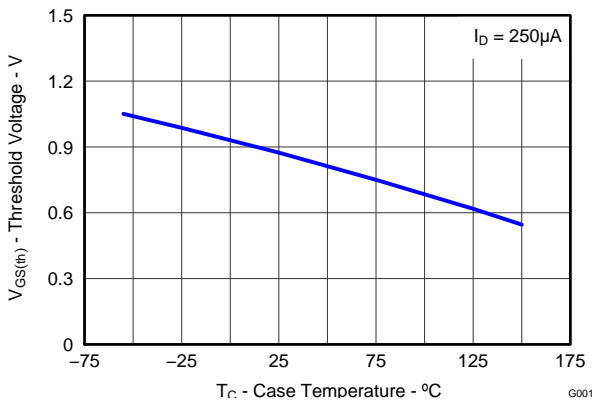


Figure 6. Threshold Voltage vs. Temperature

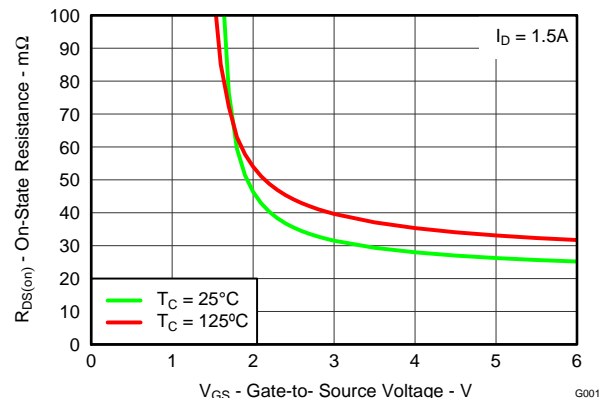


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

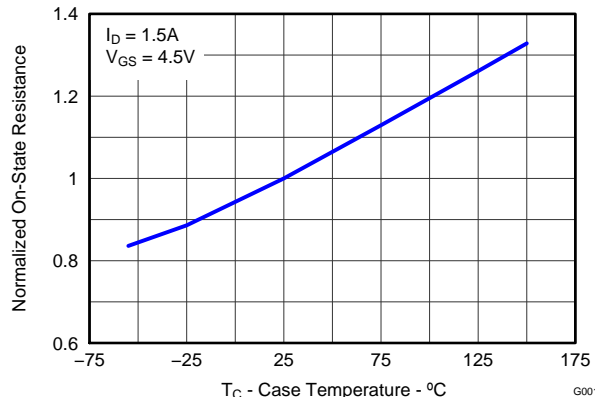


Figure 8. Normalized On Resistance vs. Temperature

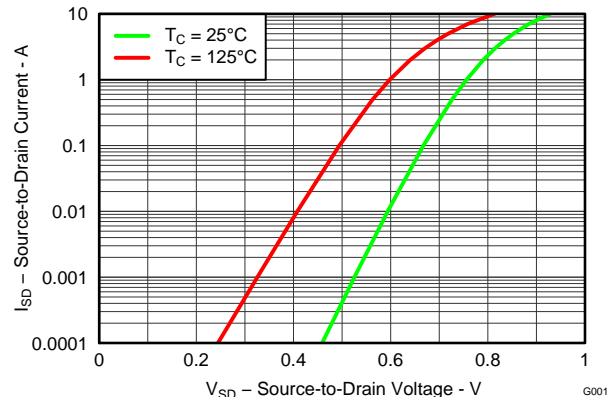


Figure 9. Typical Diode Forward Voltage

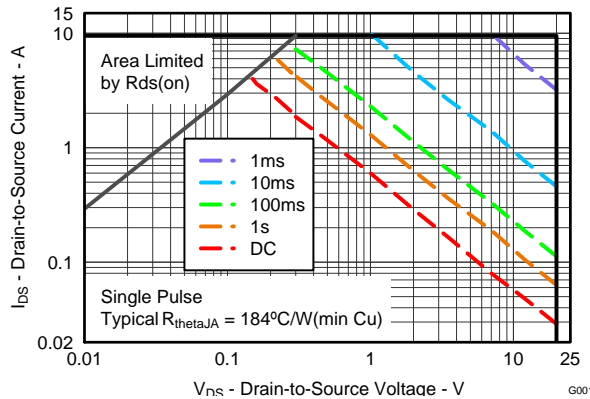


Figure 10. Maximum Safe Operating Area

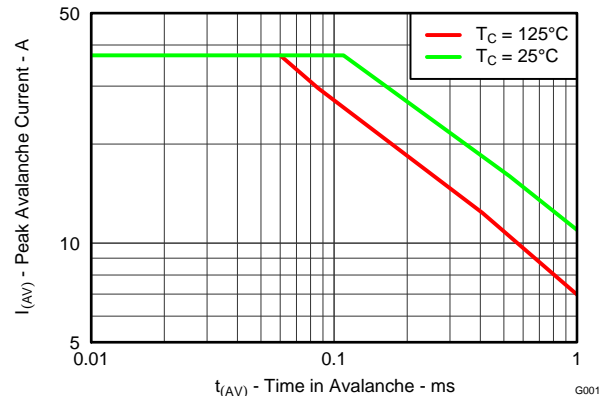


Figure 11. Single Pulse Unclamped Inductive Switching

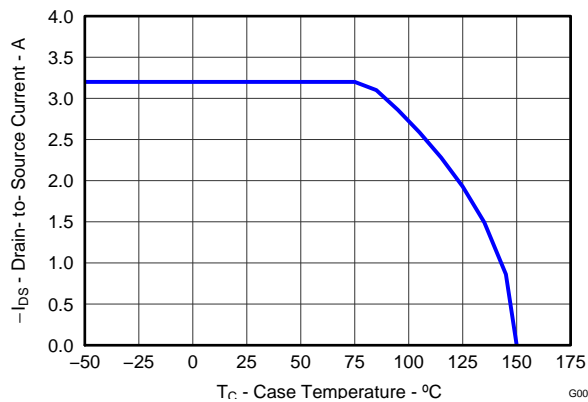
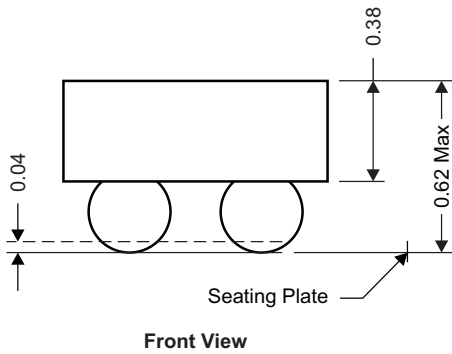
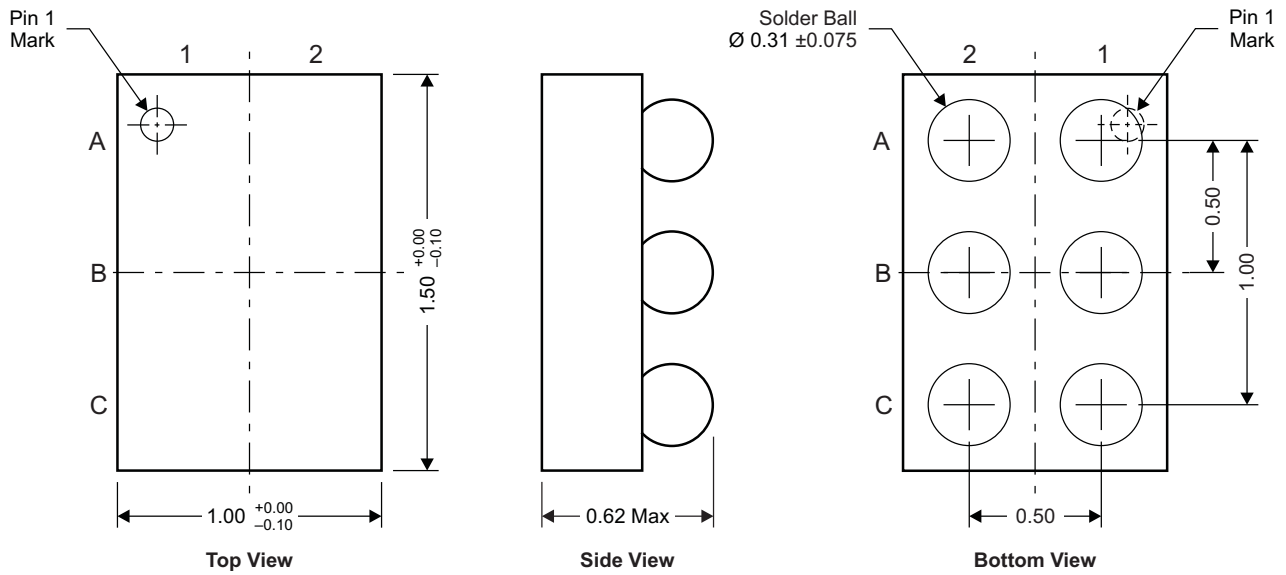


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD25211W1015 Package Dimensions



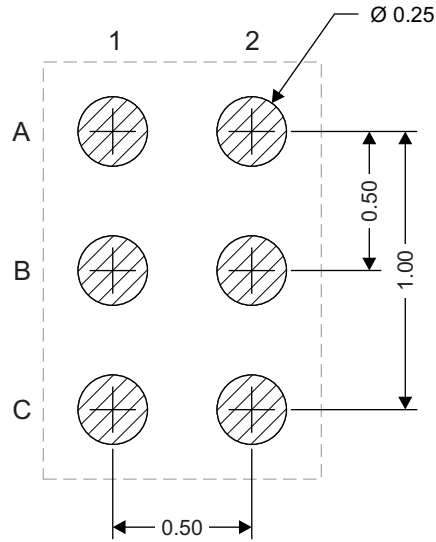
NOTE: All dimensions are in mm (unless otherwise specified)

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Pinout

POSITION	DESIGNATION
C1, C2	Drain
A1	Gate
A2, B1, B2	Source

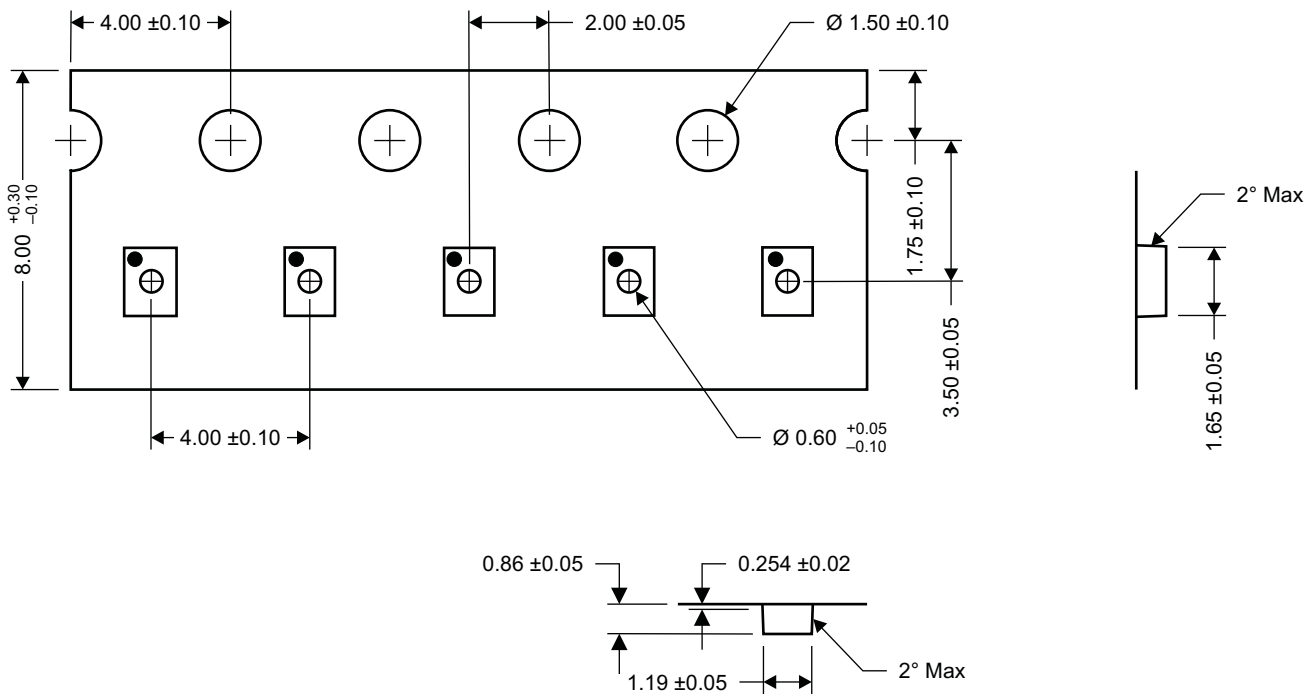
Land Pattern Recommendation



M0158-01

NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



M0159-01

NOTE: All dimensions are in mm (unless otherwise specified)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
CSD25211W1015	ACTIVE	DSBGA	YZC	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

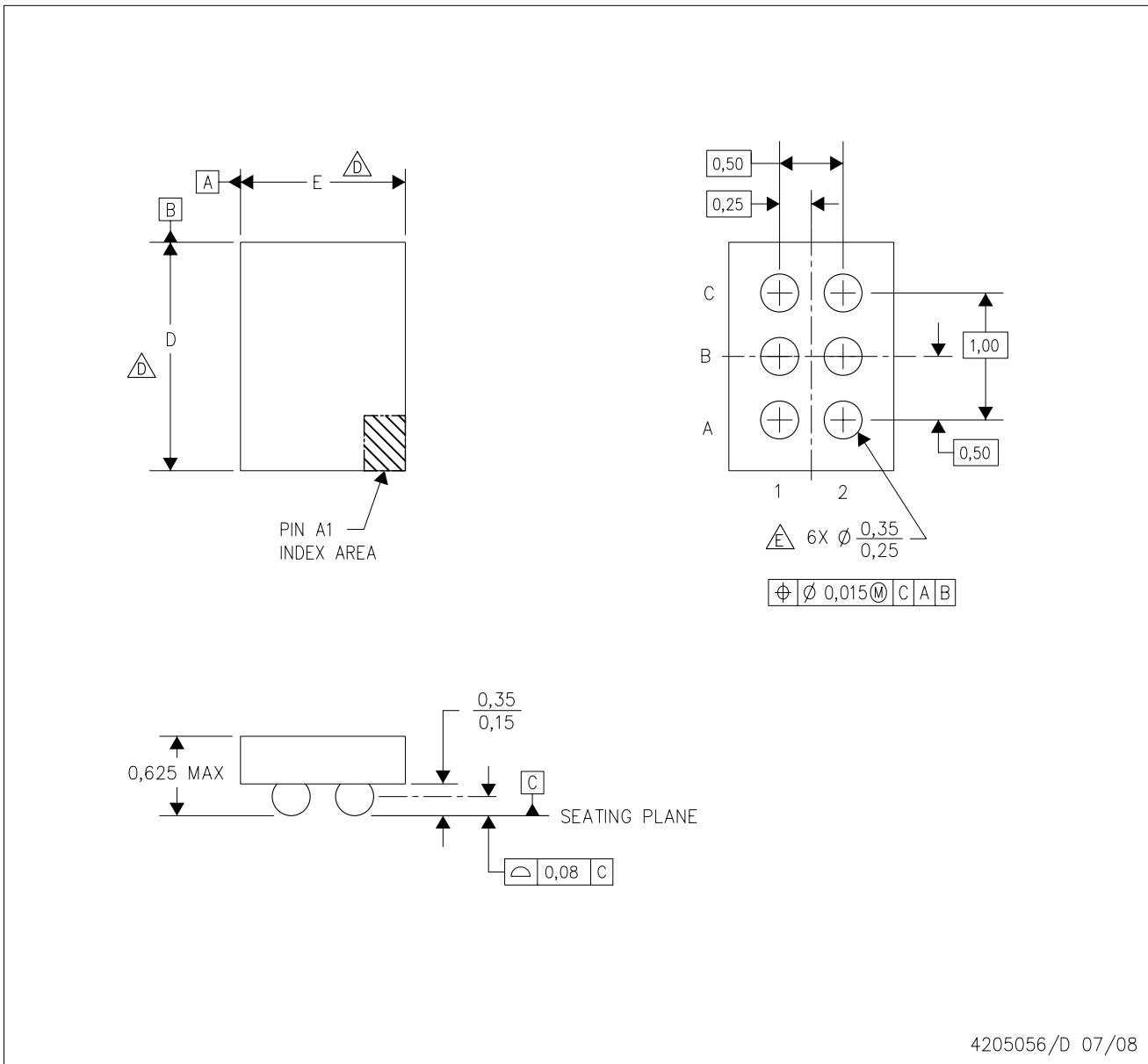
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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YZC (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



4205056/D 07/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - $\triangle D$ Devices in YZC package can have dimension D ranging from 1.44 to 2.15 mm and dimension E ranging from 0.94 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
 - E. Reference Product Data Sheet for array population.
3 x 2 matrix pattern is shown for illustration only.
 - F. This package contains lead-free balls.
Refer to YEC (Drawing #4204179) for tin-lead (SnPb) balls.

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