FAIRCHILD SEMICONDUCTOR®

June 2007

UniFET™

FDB12N50TM

N-Channel MOSFET

500V, 11.5A, 0.65Ω

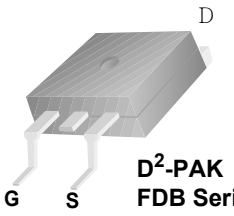
Features

- $R_{DS(on)}$ = 0.55Ω (Typ.)@ V_{GS} = 10V, I_D = 6A
- Low gate charge (Typ. 22nC)
- Low C_{rss} (Typ. 12pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant

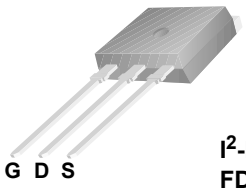
Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

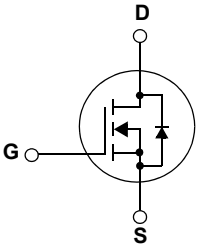
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



D^2-PAK
FDB Series



I^2-PAK
FDI Series



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		500	V
V_{GSS}	Gate to Source Voltage		±30	V
I_D	Drain Current	-Continuous (T_C = 25°C)	11.5	A
		-Continuous (T_C = 100°C)	6.9	
I_{DM}	Drain Current	- Pulsed (Note 1)	46	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	456	mJ
I_{AR}	Avalanche Current	(Note 1)	11.5	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	16.7	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)	165	W
		- Derate above 25°C	1.33	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.75	°C/W
$R_{\theta JA}$*	Thermal Resistance, Junction to Ambient*	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

*When mounted on the minimum pad size recommended (PCB Mount)

Peak Diode Recovery dv/dt Test Circuit & Waveforms