

FDB86135

N-Channel PowerTrench® MOSFET

100V, 176A, 3.5mΩ

Features

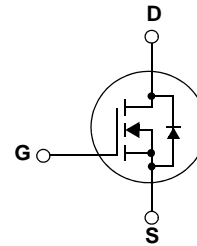
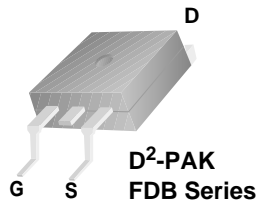
- Max $R_{DS(on)} = 3.5m\Omega$ at $V_{GS} = 10V$, $I_D = 75A$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

- DC-DC primary bridge
- DC-DC Synchronous rectification
- Hot swap



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units	
V_{DSS}	Drain to Source Voltage	100	V	
V_{GSS}	Gate to Source Voltage	± 20	V	
I_D	Drain Current - Continuous (Silicon Limited) $T_C = 25^\circ C$	176	A	
	- Continuous (Package Limited) $T_C = 25^\circ C$	120		
	- Continuous $T_C = 25^\circ C$ (Note 1a)	75	A	
	- Pulsed	704		
E_{AS}	Single Pulsed Avalanche Energy (Note 3)	658	mJ	
P_D	Power Dissipation	- $T_C = 25^\circ C$ (Note 1a)	227	W
		- $T_A = 25^\circ C$ (Note 1b)	2.4	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ C$	

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	0.66	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB86135	FDB86135	D2-PAK	330mm	24mm	800

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, $T_C = 25^\circ\text{C}$	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.07	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 75\text{A}$	-	3.0	3.5	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}$, $I_D = 75\text{A}$	-	167	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	5485	7295	pF
C_{oss}	Output Capacitance		-	2430	3230	pF
C_{rfs}	Reverse Transfer Capacitance		-	210	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 80\text{V}$, $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$	-	89	116	nC
Q_{gs}	Gate to Source Gate Charge		-	24	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	8	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	25	-	nC

Switching Characteristics

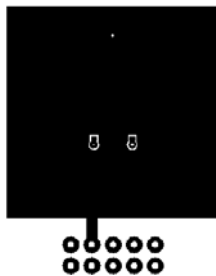
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{V}$, $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$, $R_{GEN} = 4.7\Omega$	-	22	54	ns
t_r	Turn-On Rise Time		-	54	118	ns
$t_{d(off)}$	Turn-Off Delay Time		-	37	84	ns
t_f	Turn-Off Fall Time		-	11	32	ns

Drain-Source Diode Characteristics

V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_{SD} = 75\text{A}$ (Note 2)	-	-	1.25	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}$, $I_{SD} = 75\text{A}$, $V_{DD} = 80\text{V}$	-	72	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$	-	129	-	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $40^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $62.5^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < $300\mu\text{s}$, Duty cycle < 2.0 %.

3. Starting $T_J = 25^\circ\text{C}$, $L = 1\text{ mH}$, $I_{AS} = 36.3\text{ A}$, $V_{DD} = 100\text{ V}$, $V_{GS} = 10\text{ V}$.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

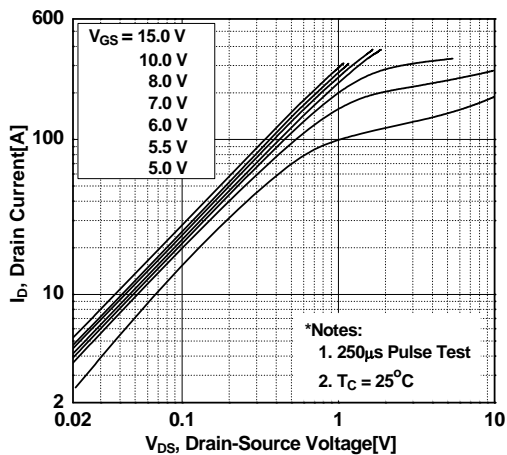


Figure 2. Transfer Characteristics

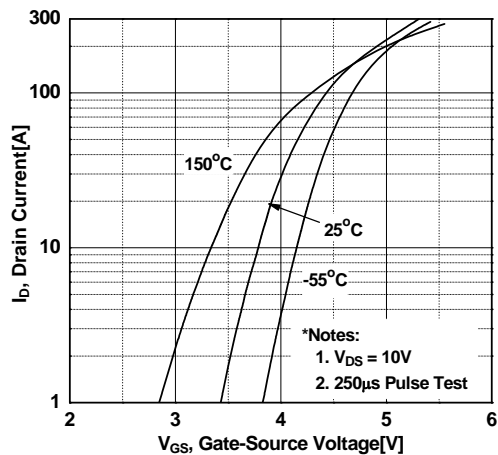


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

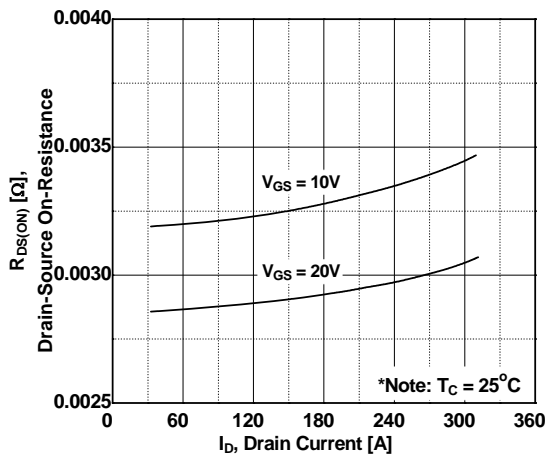


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

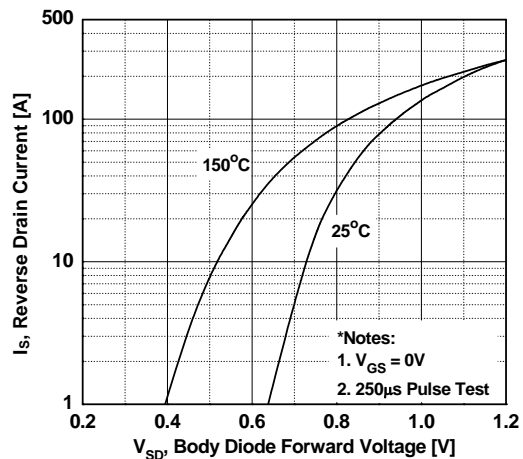


Figure 5. Capacitance Characteristics

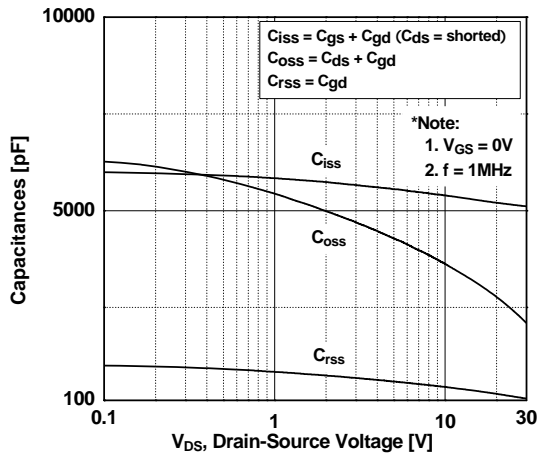
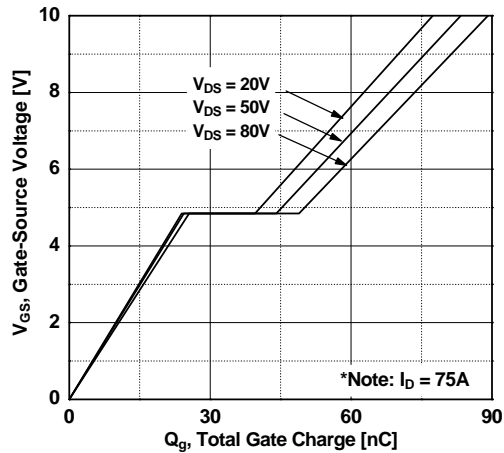


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics

Figure 7. Breakdown Voltage Variation vs. Temperature

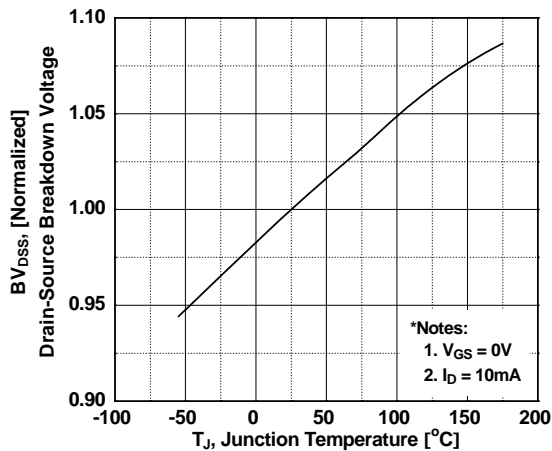


Figure 8. On-Resistance Variation vs. Temperature

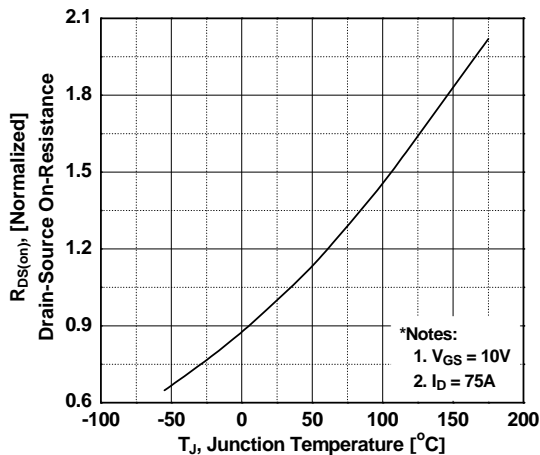


Figure 9. Maximum Safe Operating Area

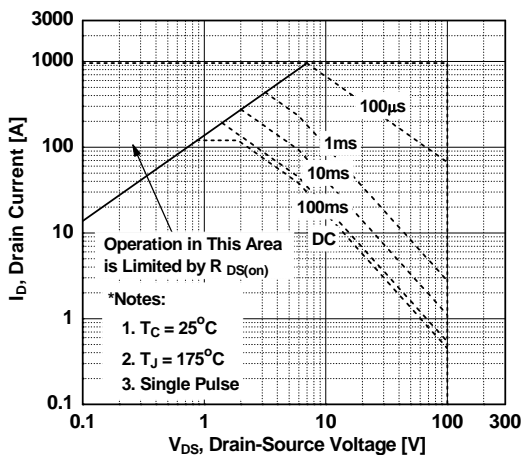


Figure 10. Maximum Drain Current vs. Case Temperature

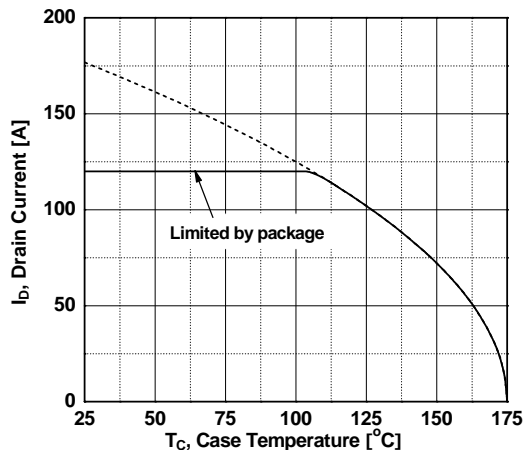
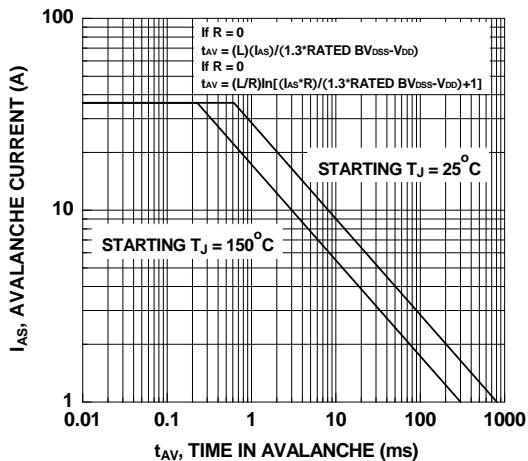
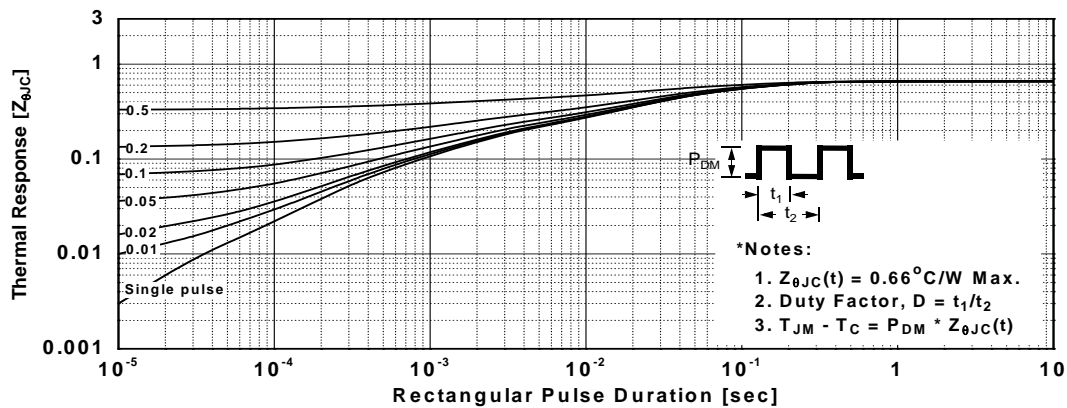


Figure 11. Unclamped Inductive Switching Capability

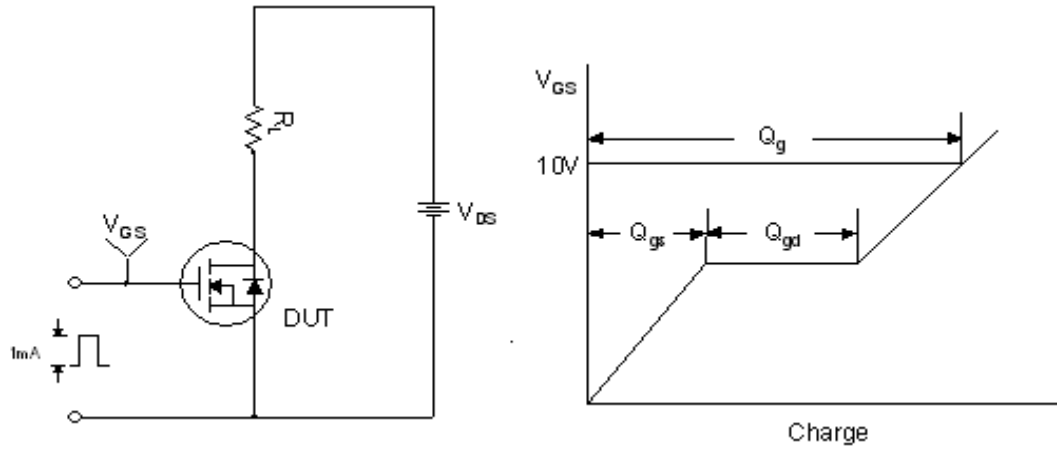


Typical Performance Characteristics

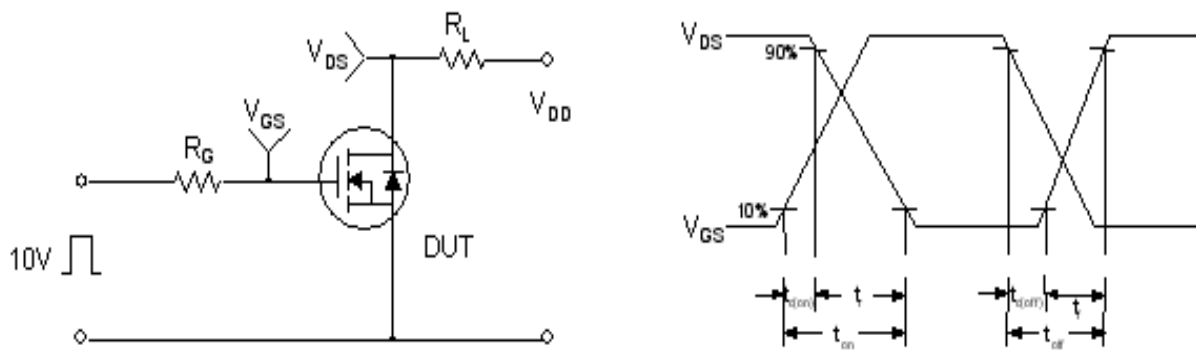
Figure 12. Transient Thermal Response Curve



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

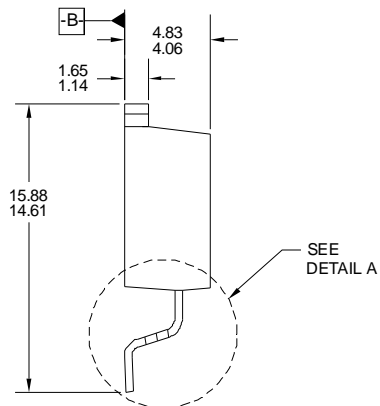
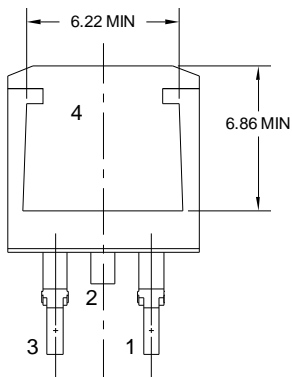
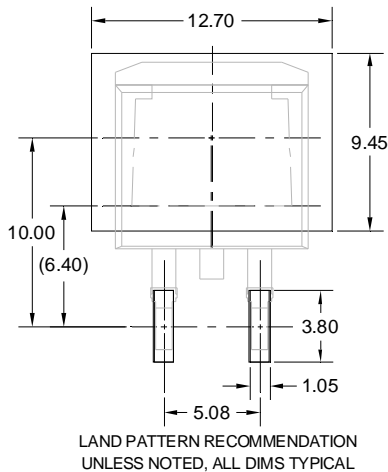
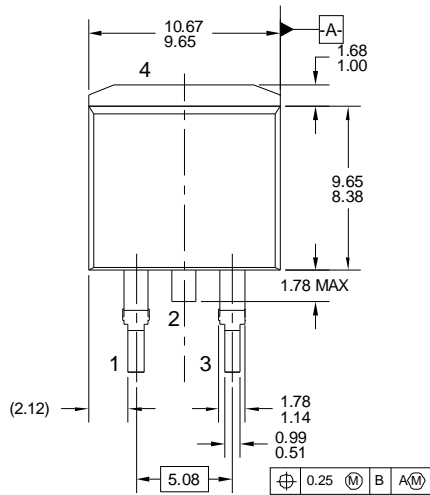


Peak Diode Recovery dv/dt Test Circuit & Waveforms

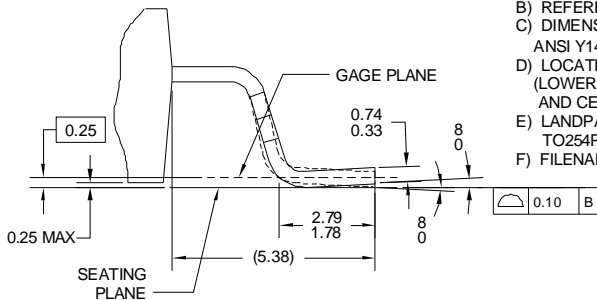


Mechanical Dimensions

D2-PAK



- NOTES: UNLESS OTHERWISE SPECIFIED
 A) ALL DIMENSIONS ARE IN MILLIMETERS.
 B) REFERENCE JEDEC, TO-263, VARIATION AB.
 C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1994.
 D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
 E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
 F) FILENAME: TO263A02REV6



Dimensions in Millimeters



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