



FP105

TR:PNP Epitaxial Planar Silicon Transistor
SBD:Schottky Barrier Diode

DC-DC Converter Applications

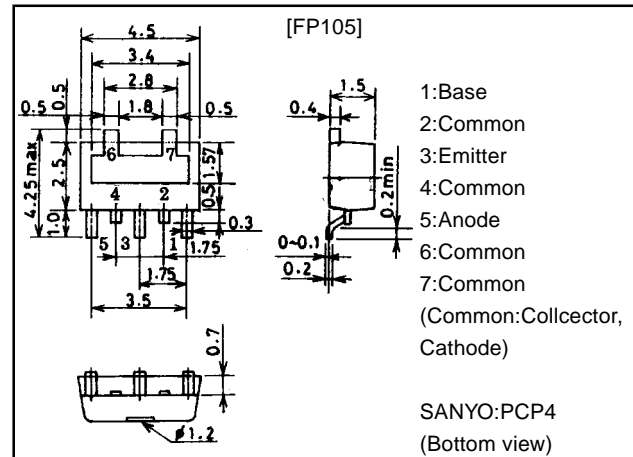
Features

- Composite type with a PNP transistor and a Schottky barrier diode contained in one package, facilitating high-density mounting.
- The FP105 is formed with 2 chips, one being equivalent to the 2SB1123 and the other the SB05-05CP, placed in one package.

Package Dimensions

unit:mm

2088A



Specifications

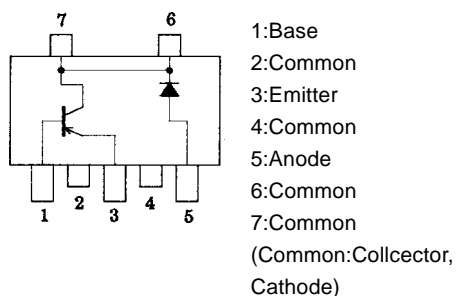
Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
[TR]				
Collector-to-Base Voltage	V_{CB0}		-60	V
Collector-to-Emitter Voltage	V_{CEO}		-50	V
Emitter-to-Base Voltage	V_{EBO}		-6	V
Collector Current	I_C		-2	A
Collector Current (Pulse)	I_{CP}		-4	A
Base Current	I_B		-400	mA
Collector Dissipation	P_C	Mounted on ceramic board (250mm ² ×0.8mm)	1.3	W
Junction Temperature	T_J		150	°C
[SBD]				
Repetitive Peak Reverse Voltage	V_{RRM}		50	V
Non-repetitive Peak Reverse Surge Voltage	V_{RSM}		55	V
Average Rectified Current	I_O		500	mA
Surge Forward Current	I_{FSM}	50Hz sine wave, 1cycle	5	A
Junction Temperature	T_J		-55 to +125	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Marking:105

Continued on next page.

Electrical Connection



SANYO Electric Co.,Ltd. Semiconductor Business Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

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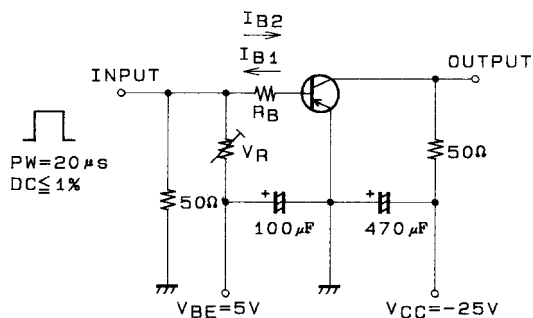
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Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[TR]						
Collector Cutoff Current	I_{CBO}	$V_{CB}=-50V, I_E=0$			-0.1	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB}=-4V, I_C=0$			-0.1	μA
DC Current Gain	h_{FE1}	$V_{CE}=-2V, I_C=-100mA$	140		560	
	h_{FE2}	$V_{CE}=-2V, I_C=-1.5A$	40			
Gain-Bandwidth Product	f_T	$V_{CE}=-10V, I_C=-50mA$		150		MHz
Output Capacitance	C_{ob}	$V_{CE}=-10V, f=1MHz$		22		pF
C-E Saturation Voltage	$V_{CE(sat)}$	$I_C=-1.0A, I_B=-50mA$		-0.3	-0.7	V
B-E Saturation Voltage	$V_{BE(sat)}$	$I_C=-1.0A, I_B=-50mA$		-0.9	-1.2	V
C-B Breakdown Voltage	$V_{(BR)CBO}$	$I_C=-10\mu A, I_E=0$	-60			V
C-E Breakdown Voltage	$V_{(BR)CEO}$	$I_C=-1mA, R_{BE}=\infty$	-50			V
E-B Breakdown Voltage	$V_{(BR)EBO}$	$I_E=-10\mu A, I_C=0$	-6			V
Turn-ON Time	t_{on}	See specified Test Circuit		60		ns
Storage Time	t_{stg}	See specified Test Circuit		450		ns
Fall Time	t_f	See specified Test Circuit		30		ns
[SBD]						
Reverse Voltage	V_R	$I_R=200\mu A$	50			V
Forward Voltage	V_F	$I_F=500mA$			0.55	V
Reverse Current	I_R	$V_R=25V$			50	μA
Interterminal Capacitance	C	$V_R=10V, f=1MHz$		22		pF
Reverse Recovery Time	t_{rr}	$I_F=I_R=100mA$, See specified Test Circuit			10	ns
Thermal Resistance	R_{thj-a}	Mounted on ceramic board (250mm ² ×0.8mm)		120		°C/W

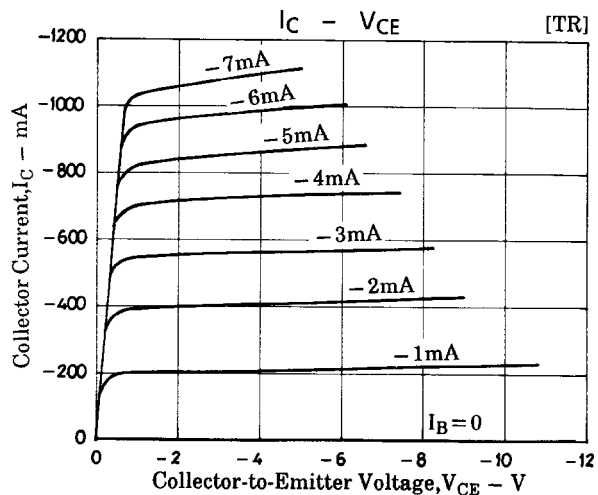
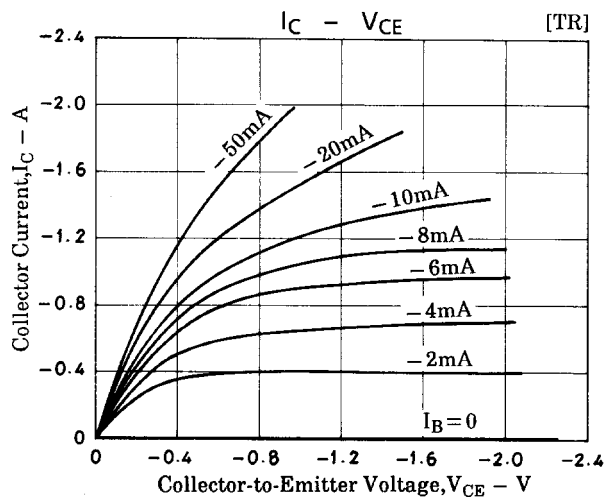
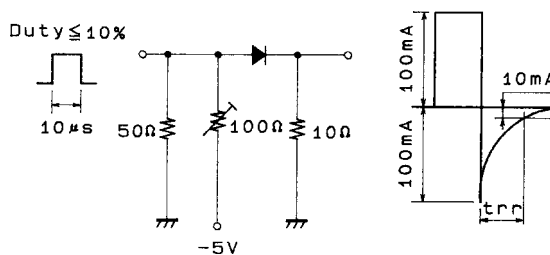
Switching Time Test Circuit

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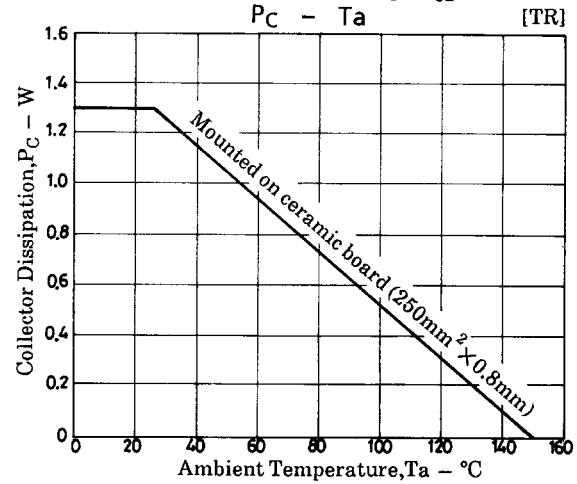
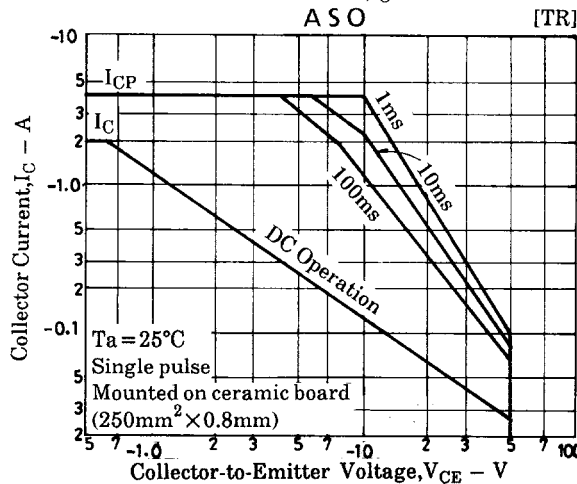
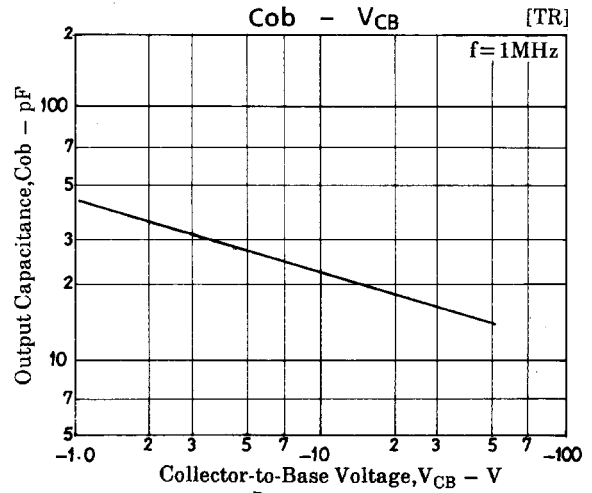
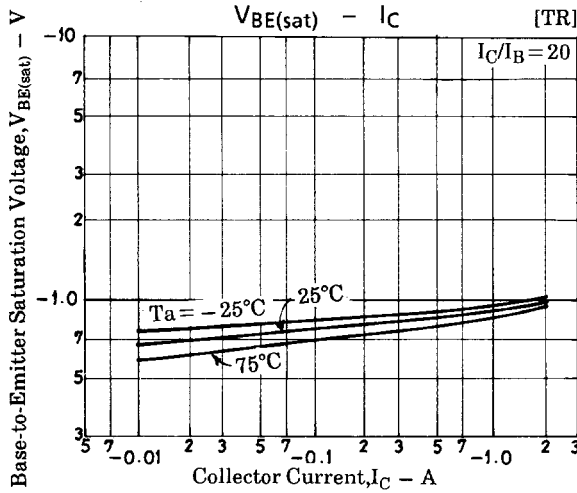
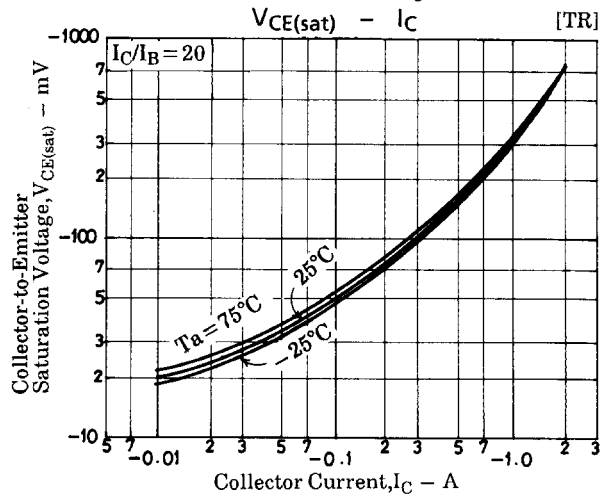
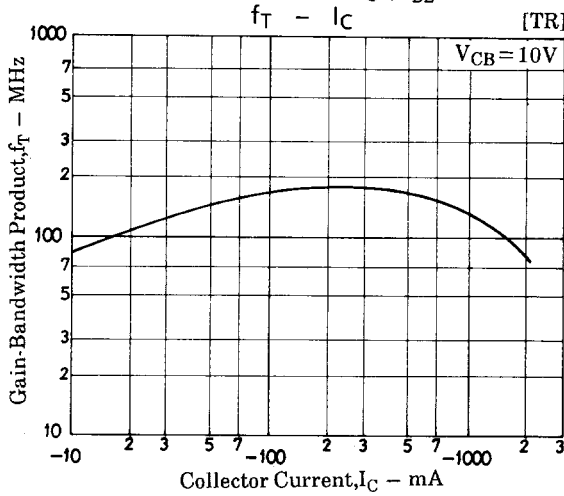
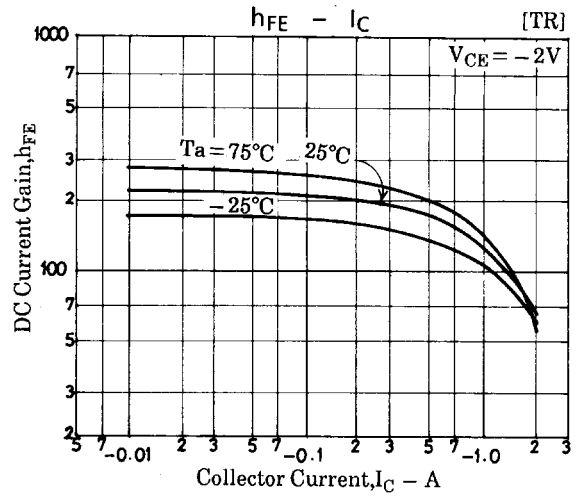
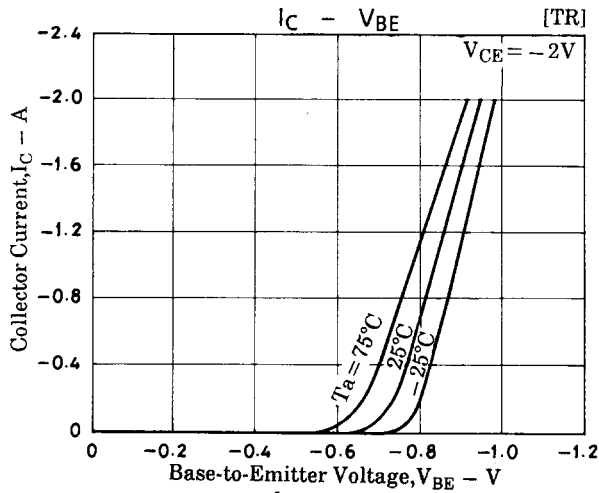


$$-10I_{B1} = 10I_{B2} = I_C = -500mA$$

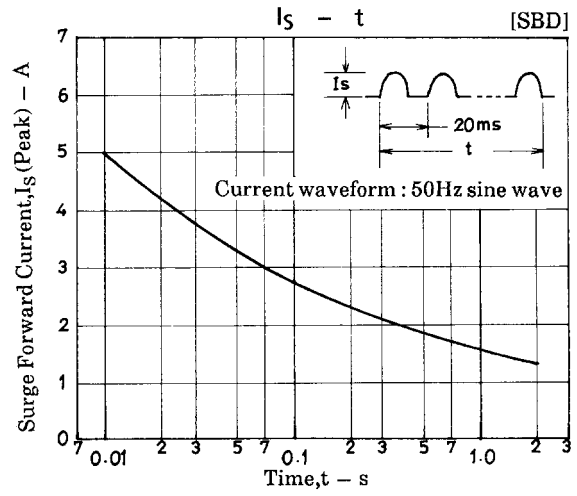
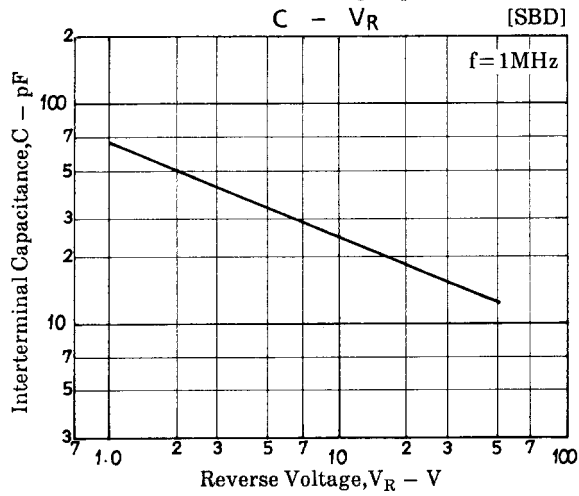
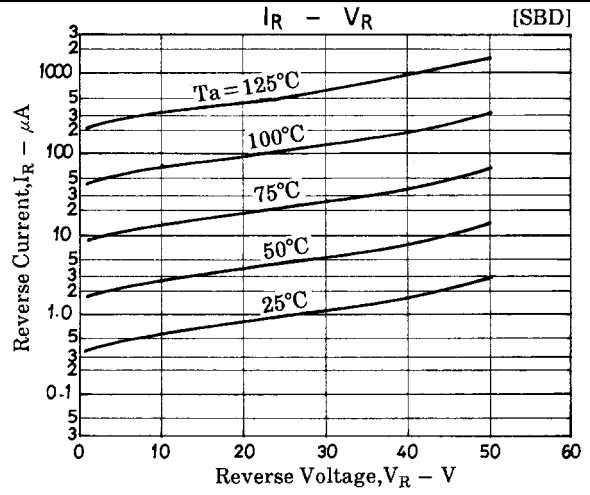
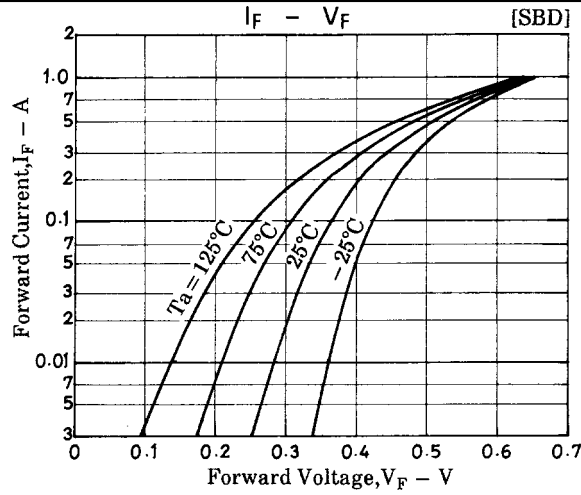
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