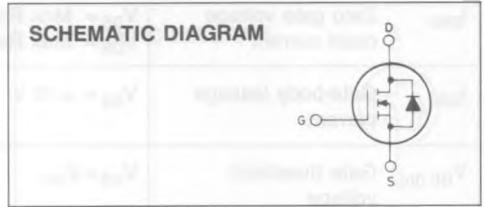


**N - CHANNEL ENHANCEMENT MODE  
POWER MOS TRANSISTOR IN DIE FORM**

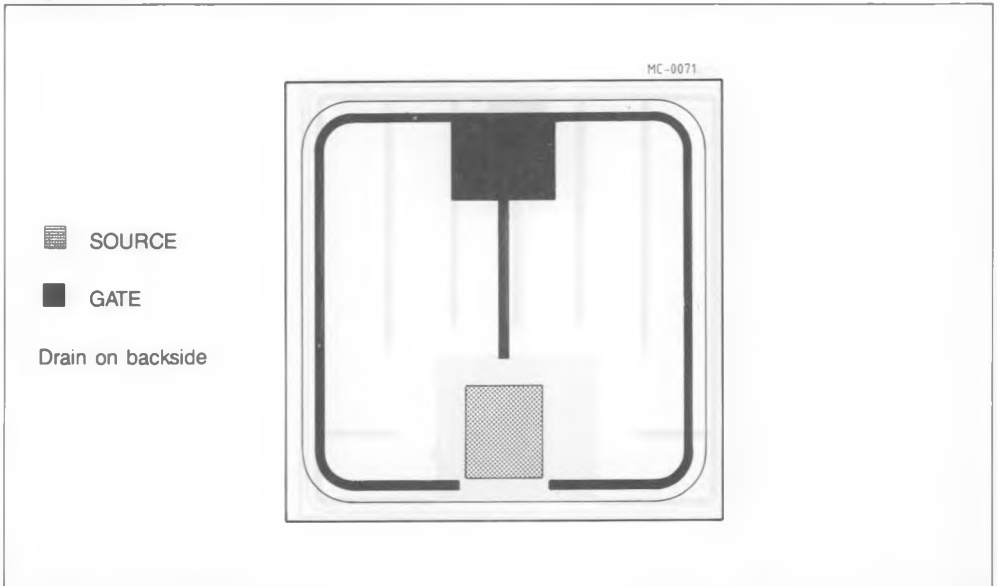
- DIE SIZE: 95 × 95 mils
- METALLIZATION:
  - Top Al
  - Back Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  - Source 28 × 30 mils
  - Gate 16 × 18 mils
- RECOMMENDED WIRE BONDING:
  - Source Al - max 10 mils
  - Gate Al - max 5 mils



$V_{DSS}$	$R_{DS(on)}$	$I_D^*$
100 V	0.27 $\Omega$	9.2 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

*Die geometry*



\* With  $R_{th-jc}$  max. 3.12°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS ( $T_j = 25^\circ\text{C}$ , Note 1)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$ Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ $V_{GS} = 0$	100			V
$I_{DSS}$ Zero gate voltage drain current	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_j = 125^\circ\text{C}$			250 1000	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$ Gate-body leakage current	$V_{GS} = \pm 20 \text{ V}$			100	nA
$V_{GS(th)}$ Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu\text{A}$	2		4	V
$R_{DS(on)}$ Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ $I_D = 1 \text{ A}$			0.27	$\Omega$

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width  $< 300 \mu\text{s}$ , duty cycle  $< 2\%$

2 - For detailed device characteristics please refer to the discrete device datasheet

