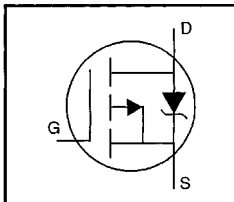


HEXFET® Power MOSFET

- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- P-Channel
- 175°C Operating Temperature
- Fast Switching



$$V_{DSS} = -100V$$

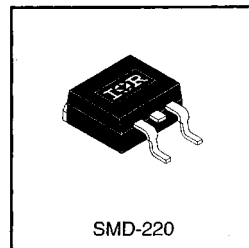
$$R_{DS(on)} = 1.2\Omega$$

$$I_D = -4.0A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SMD-220 is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



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Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-4.0	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-2.8	
I_{DM}	Pulsed Drain Current ①	-16	
$P_D @ T_C = 25^\circ C$	Power Dissipation	43	W
$P_D @ T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	3.7	
	Linear Derating Factor	0.29	W/°C
	Linear Derating Factor (PCB Mount)**	0.025	
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	200	mJ
I_{AR}	Avalanche Current ①	-4.0	A
E_{AR}	Repetitive Avalanche Energy ①	4.3	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	40	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V _{GS} =0V, I _D =-250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.091	—	V/°C	Reference to 25°C, I _D =-1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	1.2	Ω	V _{GS} =-10V, I _D =-2.4A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} =V _{GS} , I _D =-250μA
g _{fs}	Forward Transconductance	1.0	—	—	S	V _{DS} =-50V, I _D =-2.4A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	-100	μA	V _{DS} =-100V, V _{GS} =0V
		—	—	-500		V _{DS} =-80V, V _{GS} =0V, T _J =150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V _{GS} =-20V
	Gate-to-Source Reverse Leakage	—	—	100		V _{GS} =20V
Q _g	Total Gate Charge	—	—	8.7	nC	I _D =-4.0A
Q _{gs}	Gate-to-Source Charge	—	—	2.2		V _{DS} =-80V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	4.1		V _{GS} =-10V See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	10	—	ns	V _{DD} =-50V
t _r	Rise Time	—	27	—		I _D =-4.0A
t _{d(off)}	Turn-Off Delay Time	—	15	—		R _G =24Ω
t _f	Fall Time	—	17	—		R _D =11Ω See Figure 10 ④
		—	—	—		
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	200	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	94	—		V _{DS} =-25V
C _{riss}	Reverse Transfer Capacitance	—	18	—		f=1.0MHz See Figure 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-4.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-16		
V _{SD}	Diode Forward Voltage	—	—	-5.5	V	T _J =25°C, I _S =-4.0A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	82	160	ns	T _J =25°C, I _F =-4.0A
Q _{rr}	Reverse Recovery Charge	—	0.15	0.30	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DD}=-25V, starting T_J=25°C, L=18mH R_G=25Ω, I_{AS}=-4.0A (See Figure 12)
- ③ I_{SD}≤-4.0A, di/dt≤75A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤175°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.

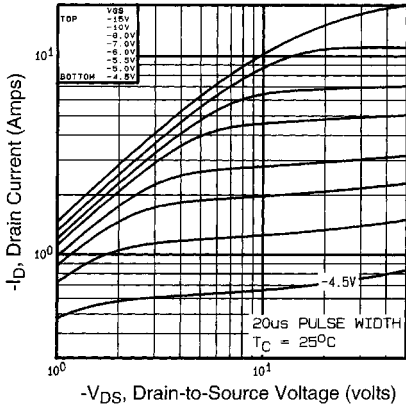


Fig 1. Typical Output Characteristics, $T_C=25^\circ\text{C}$

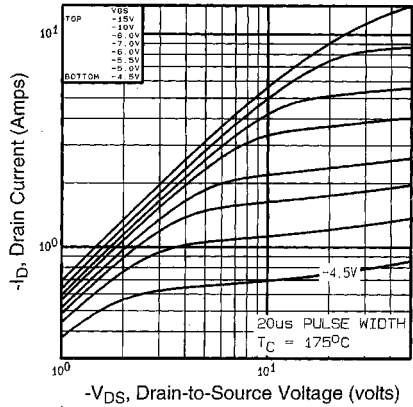


Fig 2. Typical Output Characteristics, $T_C=175^\circ\text{C}$

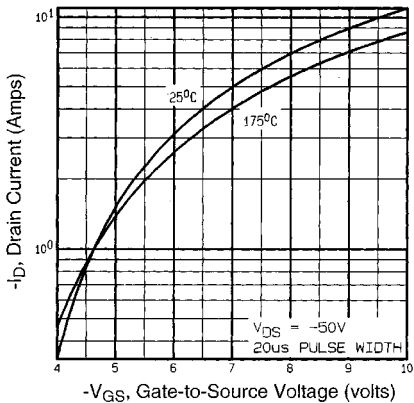


Fig 3. Typical Transfer Characteristics

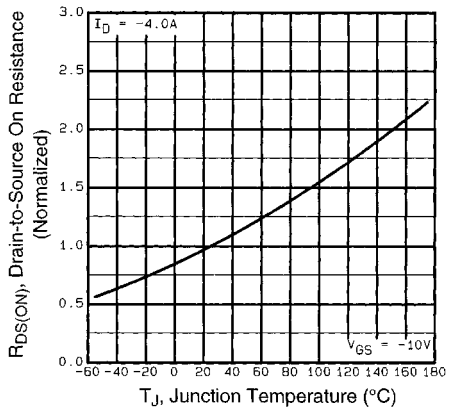


Fig 4. Normalized On-Resistance Vs. Temperature

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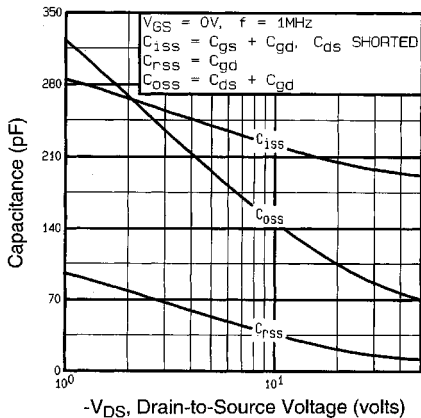


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

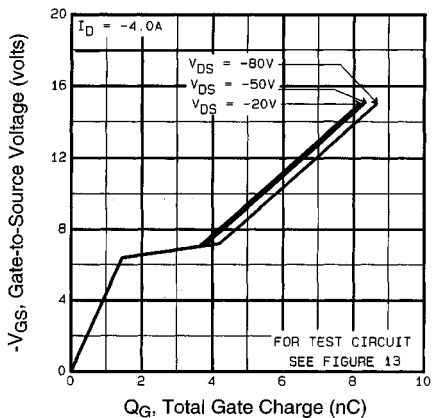


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

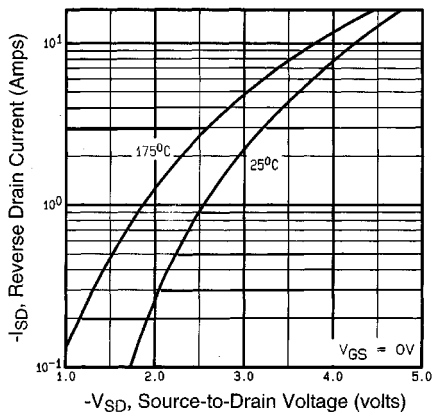


Fig 7. Typical Source-Drain Diode Forward Voltage

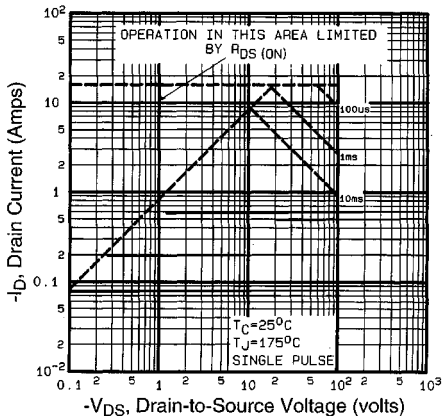


Fig 8. Maximum Safe Operating Area

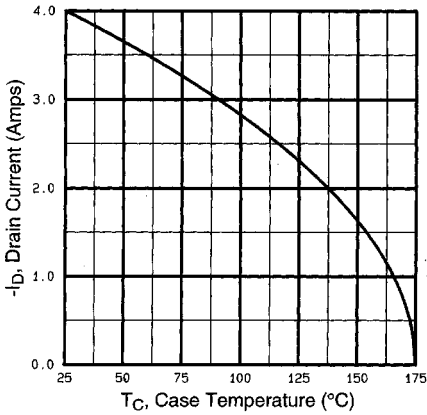


Fig 9. Maximum Drain Current Vs. Case Temperature

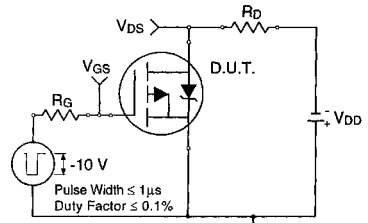


Fig 10a. Switching Time Test Circuit

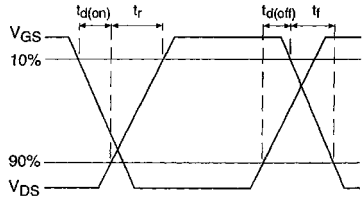


Fig 10b. Switching Time Waveforms

DATA SHEETS

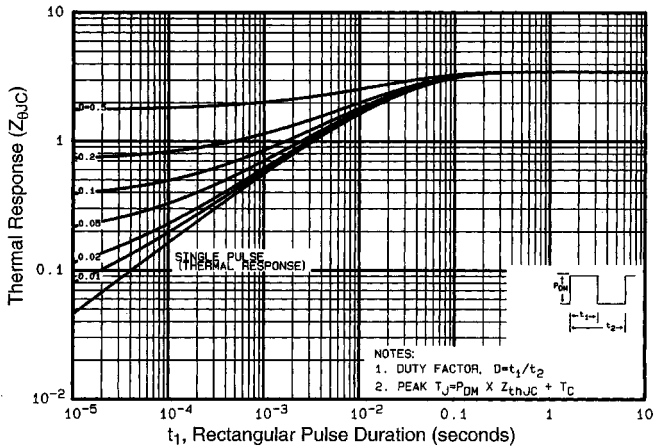


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

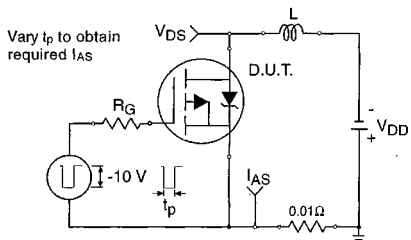


Fig 12a. Unclamped Inductive Test Circuit

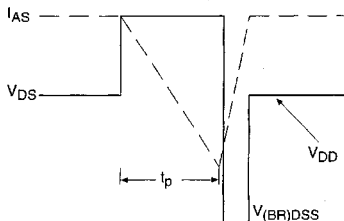


Fig 12b. Unclamped Inductive Waveforms

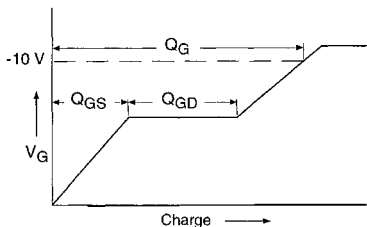


Fig 13a. Basic Gate Charge Waveform

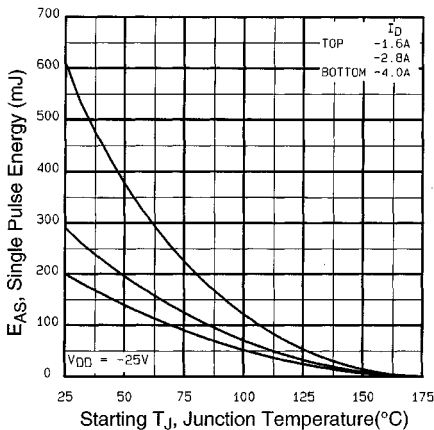


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

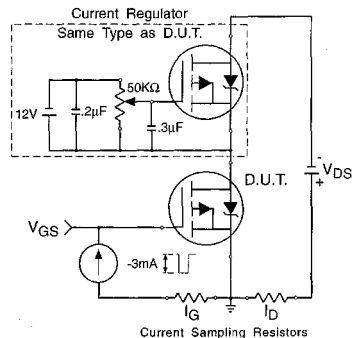


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1506

Appendix B: Package Outline Mechanical Drawing – See page 1507

Appendix C: Part Marking Information – See page 1515

Appendix D: Tape & Reel Information – See page 1519