

## IRFF310

### 1.35A, 400V, 3.600 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. They can be operated directly from integrated circuits.

### Features

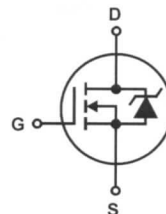
- 1.35A, 400V
- $r_{DS(ON)} = 3.600\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

### Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFF310	TO-205AF	IRFF310

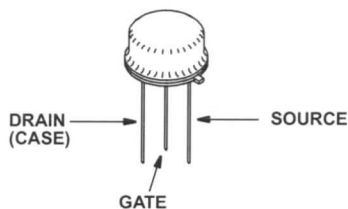
NOTE: When ordering, include the entire part number.

### Symbol



### Packaging

JEDEC TO-205AF



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# IRFF310

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

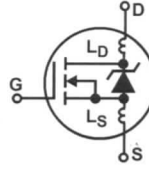
	IRFF310	UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DS}$	400 V
Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	400 V
Continuous Drain Current . . . . .	$I_D$	1.35 A
Pulsed Drain Current (Note 3) . . . . .	$I_{DM}$	5.5 A
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 20$ V
Maximum Power Dissipation . . . . .	$P_D$	15 W
Linear Derating Factor . . . . .		0.12 W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 4) . . . . .	$E_{AS}$	150 mJ
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to 150 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s. . . . .	$T_L$	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pk}$	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

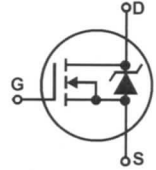
## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS		
Drain to Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$ (Figure 10)	400	-	-	V		
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V		
Zero-Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	25	$\mu\text{A}$		
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$	-	-	250	$\mu\text{A}$		
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, V_{GS} = 10\text{V}$	1.35	-	-	A		
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA		
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$V_{GS} = 10\text{V}, I_D = 0.8\text{A}$ (Figures 8, 9)	-	3.3	3.600	$\Omega$		
Forward Transconductance (Note 2)	$g_{fs}$	$V_{DS} = 10\text{V}, I_D = 1.2\text{A}$ (Figure 12)	1.0	1.2	-	S		
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \approx 0.5 \times \text{Rated } BV_{DSS}, R_G = 9.1\Omega, I_D \approx 1.35\text{A},$ $R_L = 144.5\Omega$ for $BV_{DSS} = 400\text{V},$ $R_L = 126\Omega$ for $BV_{DSS} = 350\text{V}$ (Figures 17, 18), MOSFET Switching Times are Essentially Independent of Operating Temperature	-	3	10	ns		
Rise Time	$t_r$		-	10	20	ns		
Turn-Off Delay Time	$t_{d(OFF)}$		-	5	10	ns		
Fall Time	$t_f$		-	8	15	ns		
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_g(TOT)$	$V_{GS} = 10\text{V}, I_D = 1.35\text{A}, V_{DS} = 0.8 \times \text{Rated } BV_{DSS},$ $I_{g(REF)} = 1.5\text{mA}$ (Figures 14, 19, 20), Gate Charge is Essentially Independent of Operating Temperature	-	6	7.5	nC		
Gate to Source Charge	$Q_{gs}$		-	3	-	nC		
Gate to Drain "Miller" Charge	$Q_{gd}$		-	3	-	nC		
Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1.0\text{MHz}$ (Figure 11)	-	135	-	pF		
Output Capacitance	$C_{OSS}$		-	35	-	pF		
Reverse-Transfer Capacitance	$C_{RSS}$		-	8	-	pF		
Internal Drain Inductance	$L_D$	Measured from the Drain Lead, 5mm (0.2in) from Header to Center of Die	Modified MOSFET Symbol Showing the Internal Device Inductances 		-	5.0	-	nH
Internal Source Inductance	$L_S$	Measured from the Source Lead, 5mm (0.2in) from Header and Source Bonding Pad			-	15	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	8.33	$^\circ\text{C/W}$		
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	175	$^\circ\text{C/W}$		

# IRFF310

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	$I_{SD}$	Modified MOSFET	-	-	1.35	A
Pulse Source to Drain Current (Note 3)	$I_{SDM}$	Symbol Showing the Integral Reverse P-N Junction Rectifier	-	-	5.5	A
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_{SD} = 1.35\text{A}$ , $V_{GS} = 0\text{V}$ (Figure 13)	-	-	1.6	V
Reverse Recovery Time	$t_{rr}$	$T_J = 150^\circ\text{C}$ , $I_{SD} = 1.35\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	380	-	ns
Reverse Recovered Charge	$Q_{RR}$	$T_J = 150^\circ\text{C}$ , $I_{SD} = 1.35\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	2.7	-	$\mu\text{C}$



**NOTES:**

1. Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
2. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
3.  $V_{DD} = 40\text{V}$ , start  $T_J = 25^\circ\text{C}$ ,  $L = 44.89\mu\text{H}$ ,  $R_G = 50\Omega$ , peak  $I_{AS} = 1.35\text{A}$  (See Figures 15, 16).

## Typical Performance Curves $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

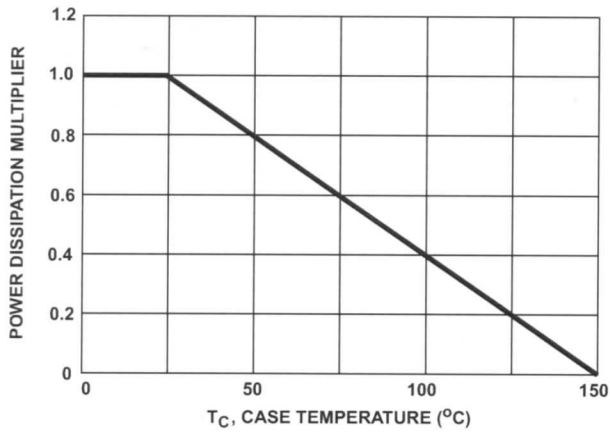


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

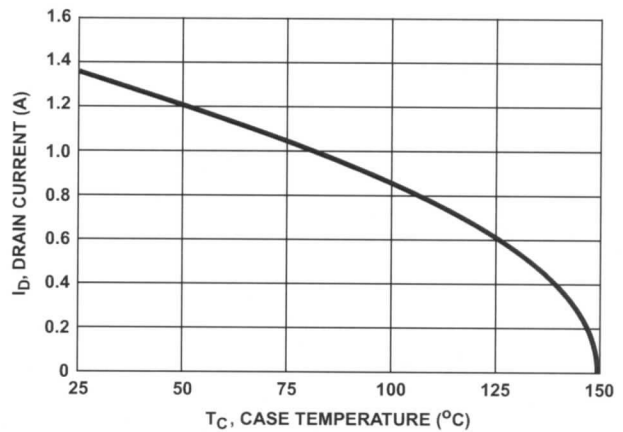


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

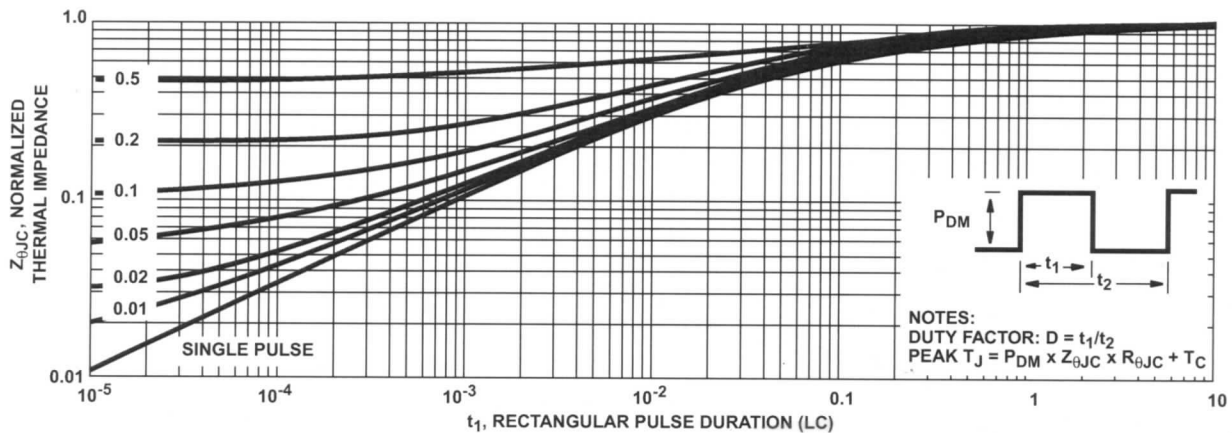


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE