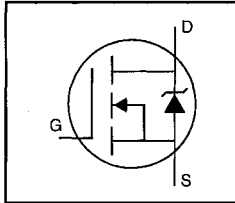


### HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KV RMS ①
- Sink to Lead Creepage Dist.= 4.8mm
- 175°C Operating Temperature
- Dynamic dv/dt Rating
- Low Thermal Resistance



$$V_{DSS} = 60V$$

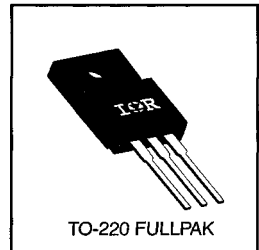
$$R_{DS(on)} = 0.10\Omega$$

$$I_D = 14A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



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
### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	14	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	10	
$I_{DM}$	Pulsed Drain Current ①	56	
$P_D @ T_C = 25^\circ C$	Power Dissipation	37	W
	Linear Derating Factor	0.24	W/°C
$V_{GS}$	Gate-to-Source Voltage	±20	V
$E_{AS}$	Single Pulse Avalanche Energy ②	100	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
$T_J$	Operating Junction and	-55 to +175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	


### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	4.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

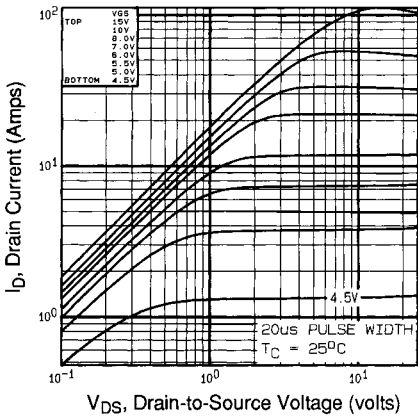
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.061	—	$\text{V}/^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.10	$\Omega$	$V_{GS}=10\text{V}$ , $I_D=8.4\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$
$g_{fs}$	Forward Transconductance	5.8	—	—	S	$V_{DS}=25\text{V}$ , $I_D=8.4\text{A}$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu\text{A}$	$V_{DS}=60\text{V}$ , $V_{GS}=0\text{V}$
		—	—	250		$V_{DS}=48\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-20\text{V}$
$Q_g$	Total Gate Charge	—	—	25	nC	$I_D=17\text{A}$
$Q_{gs}$	Gate-to-Source Charge	—	—	5.8		$V_{DS}=48\text{V}$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	11		$V_{GS}=10\text{V}$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD}=30\text{V}$
$t_r$	Rise Time	—	58	—		$I_D=17\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		$R_G=18\Omega$
$t_f$	Fall Time	—	42	—		$R_D=1.7\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	640	—	pF	$V_{GS}=0\text{V}$
$C_{oss}$	Output Capacitance	—	360	—		$V_{DS}=25\text{V}$
$C_{riss}$	Reverse Transfer Capacitance	—	79	—		$f=1.0\text{MHz}$ See Figure 5
C	Drain to Sink Capacitance	—	12	—		$f=1.0\text{MHz}$

## Source-Drain Ratings and Characteristics

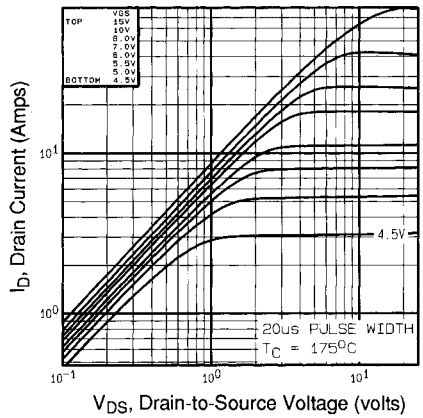
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	14	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	56		
$V_{SD}$	Diode Forward Voltage	—	—	1.5	V	$T_J=25^\circ\text{C}$ , $I_S=14\text{A}$ , $V_{GS}=0\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	90	180	ns	$T_J=25^\circ\text{C}$ , $I_r=17\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	0.32	0.64	$\mu\text{C}$	$di/dt=100\text{A}/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

### Notes:

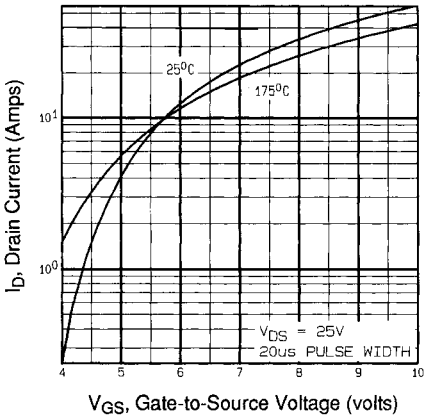
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=25\text{V}$ , starting  $T_J=25^\circ\text{C}$ ,  $L=595\mu\text{H}$ ,  $R_G=25\Omega$ ,  $I_{AS}=14\text{A}$  (See Figure 12)
- ③  $I_{SD}\leq 17\text{A}$ ,  $di/dt\leq 140\text{A}/\mu\text{s}$ ,  $V_{DS}\leq V_{(BR)DSS}$ ,  $T_J\leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$
- ⑤  $t=60\text{s}$ ,  $f=60\text{Hz}$



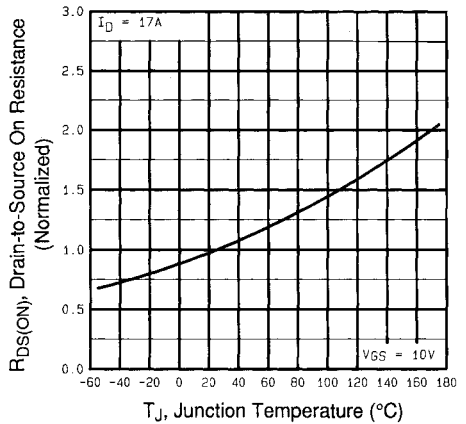
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C=175^\circ\text{C}$

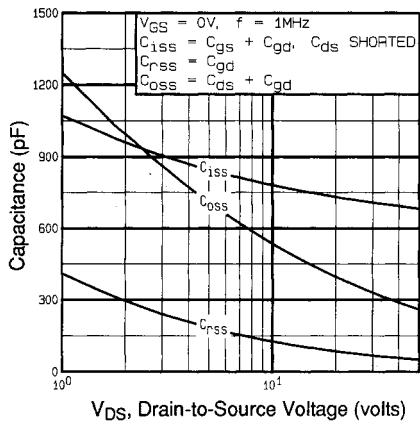


**Fig 3.** Typical Transfer Characteristics

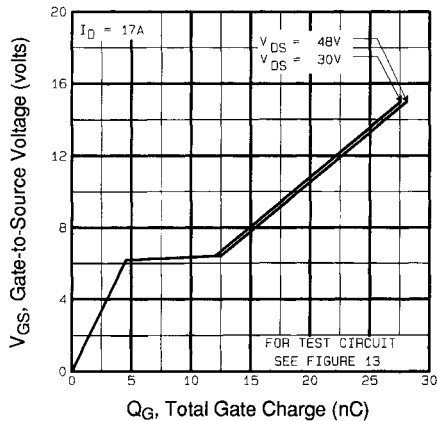


**Fig 4.** Normalized On-Resistance  
Vs. Temperature

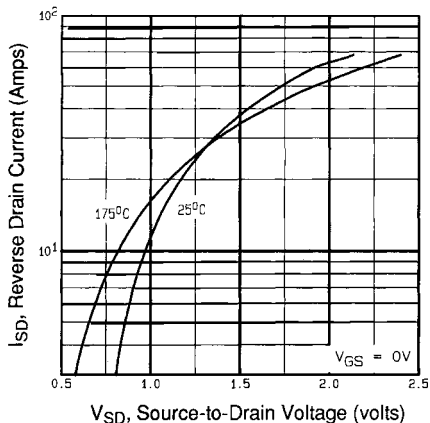
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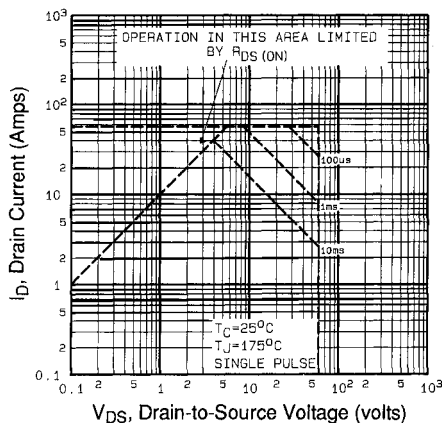
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



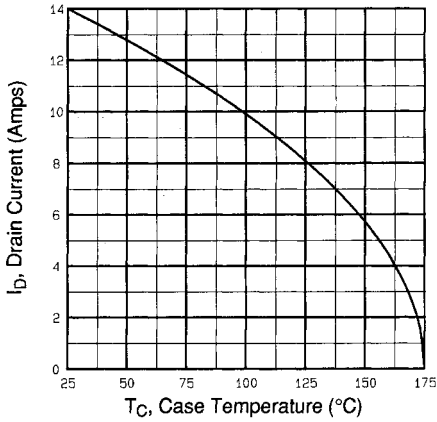
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



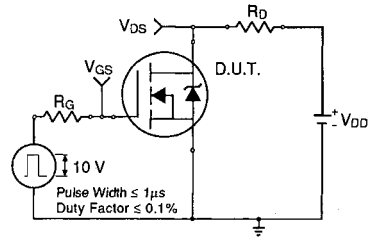
**Fig 7.** Typical Source-Drain Diode Forward Voltage



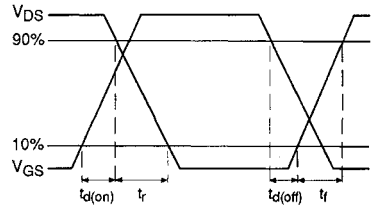
**Fig 8.** Maximum Safe Operating Area



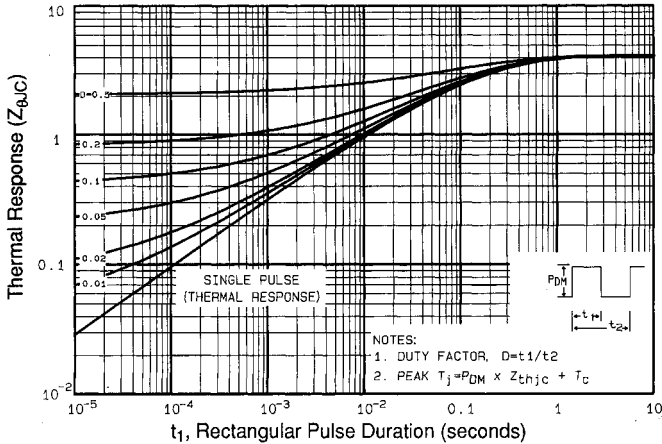
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

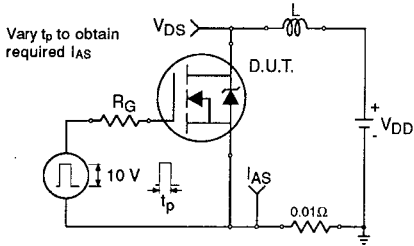


**Fig 10b.** Switching Time Waveforms

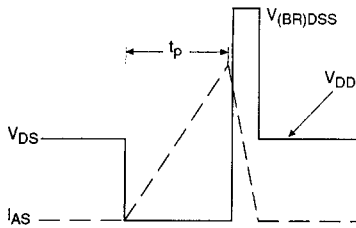


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

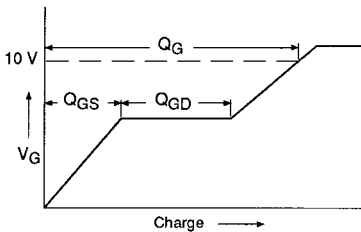
DATA SHEETS



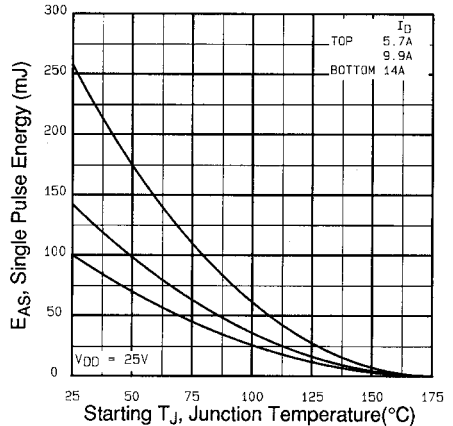
**Fig 12a.** Unclamped Inductive Test Circuit



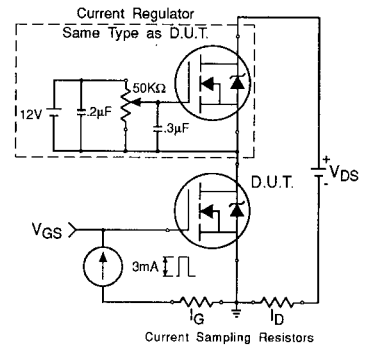
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1510

**Appendix C:** Part Marking Information – See page 1517