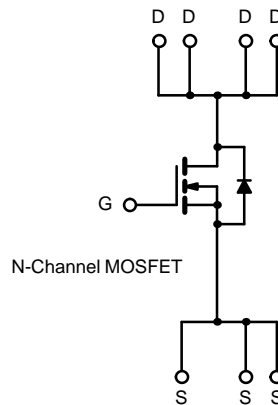
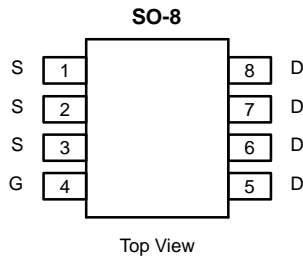




N-Channel Reduced Q_g , Fast Switching MOSFET

TrenchFET[®]
Power MOSFETs
High-Efficiency
PWM Optimized

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0085 @ $V_{GS} = 10$ V	± 13
	0.014 @ $V_{GS} = 4.5$ V	± 10



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 25	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^{a, b}	I_D	$T_A = 25^\circ\text{C}$	± 13
		$T_A = 70^\circ\text{C}$	± 10
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	± 50	A
Continuous Source Current (Diode Conduction) ^{a, b}	I_S	2.3	
Maximum Power Dissipation ^{a, b}	P_D	$T_A = 25^\circ\text{C}$	2.5
		$T_A = 70^\circ\text{C}$	1.6
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient (MOSFET) ^a	R_{thJA}		50	$^\circ\text{C}/\text{W}$	
		Steady State	70		

Notes
a. Surface Mounted on FR4 Board.
b. $t \leq 10$ sec.



MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.8			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 24\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 13\ \text{A}$		0.0069	0.0085	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 10\ \text{A}$		0.0115	0.014	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 13\ \text{A}$		26		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.3\ \text{A}, V_{GS} = 0\ \text{V}$		0.70	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}, V_{GS} = 5.0\ \text{V}, I_D = 13\ \text{A}$		19.5	25	nC
Gate-Source Charge	Q_{gs}			4.2		
Gate-Drain Charge	Q_{gd}			8.8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}, R_L = 15\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		14	22	ns
Rise Time	t_r			9	15	
Turn-Off Delay Time	$t_{d(off)}$			46	70	
Fall Time	t_f			30	45	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.3\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		35	70	

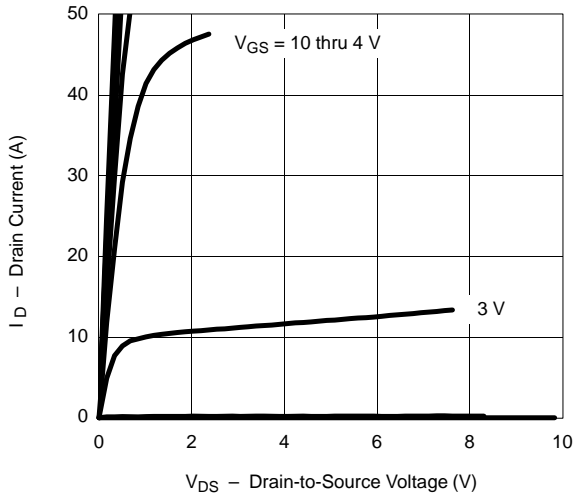
Notes

- Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

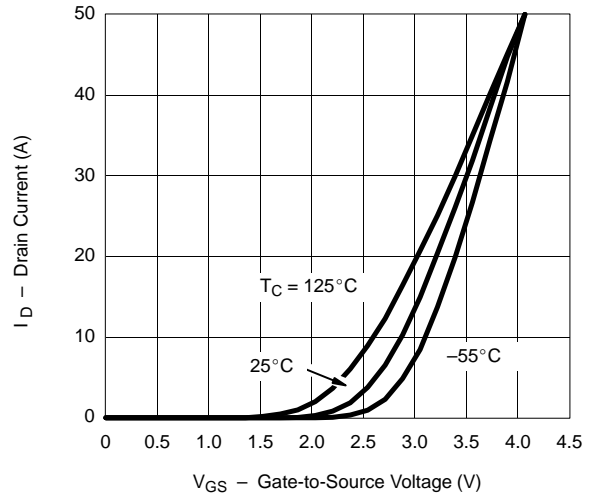


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

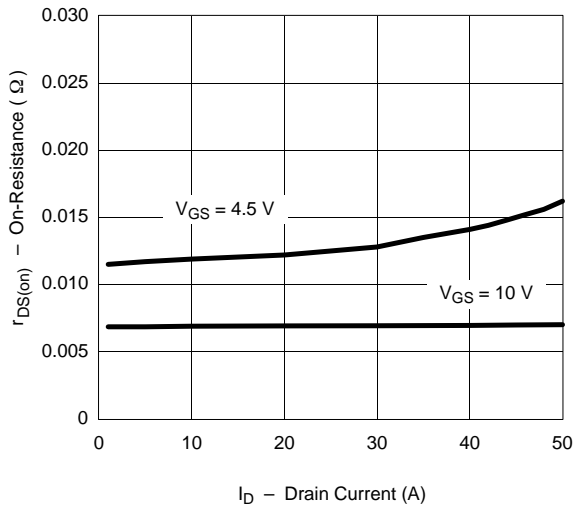
Output Characteristics



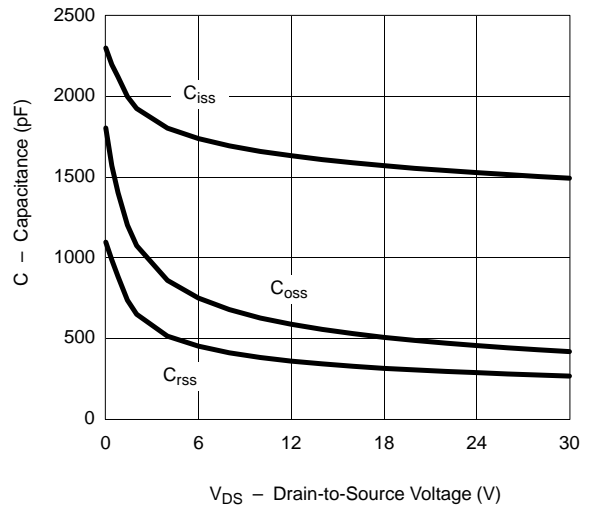
Transfer Characteristics



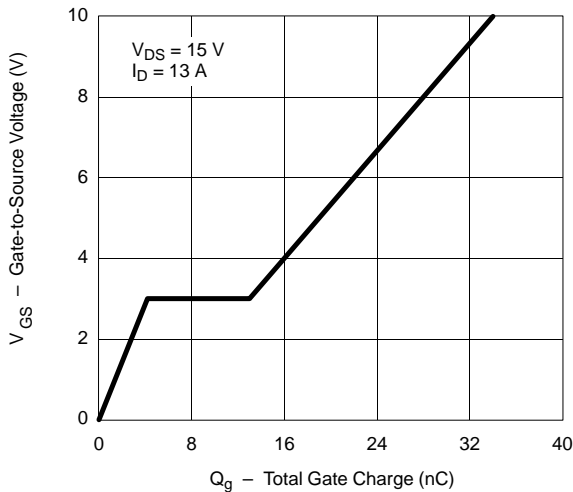
On-Resistance vs. Drain Current



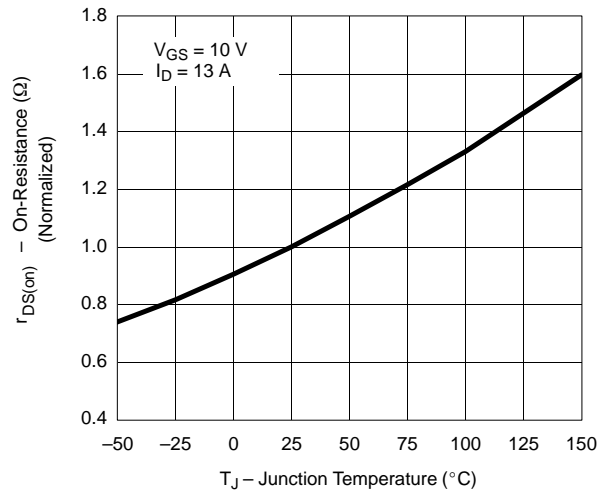
Capacitance



Gate Charge



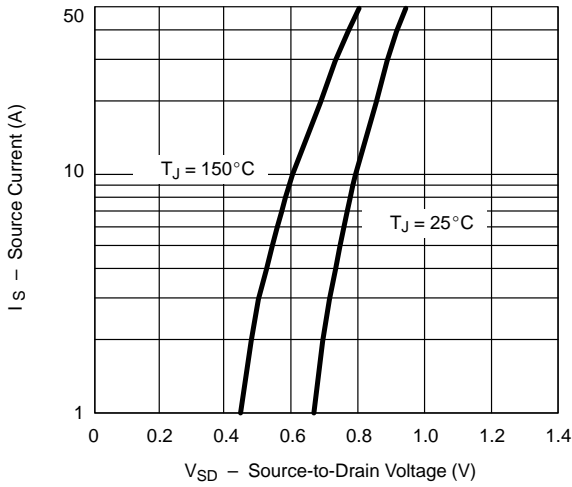
On-Resistance vs. Junction Temperature



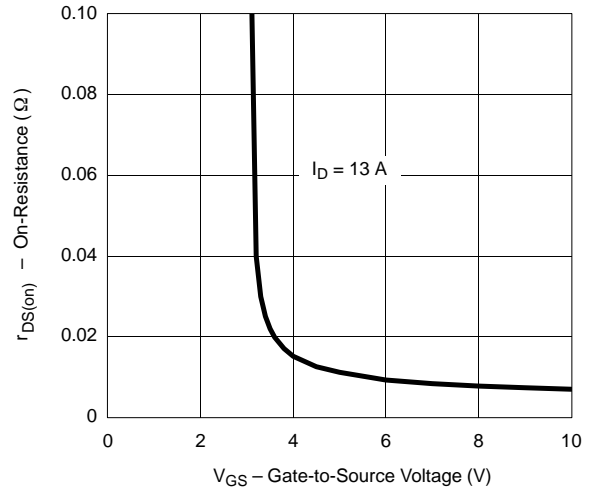


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

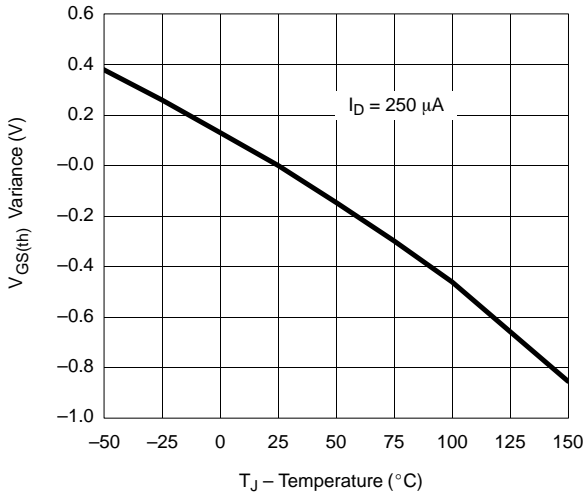
Source-Drain Diode Forward Voltage



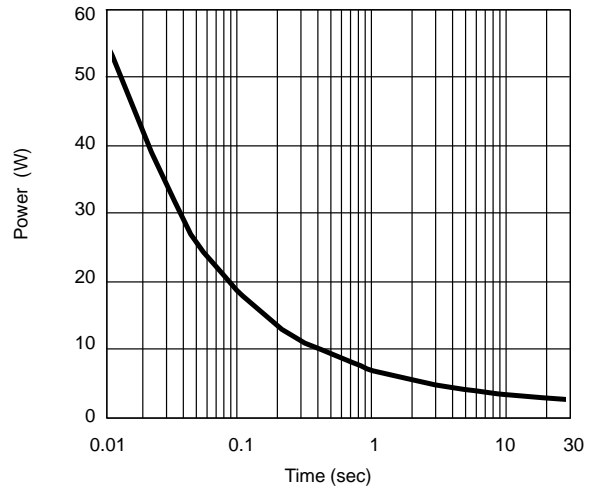
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

