

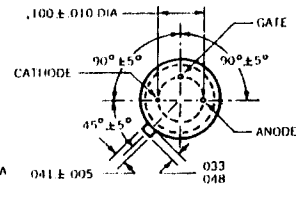
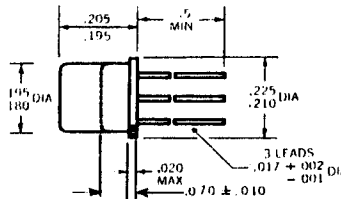
**SILICON PNP
 PASSIVATED PLANAR
 CONTROLLED SWITCH**

**2N3027
 2N3028
 2N3029**

TO-18
 2N3027
 2N3028
 2N3029



TO-18 OUTLINE



TO-18

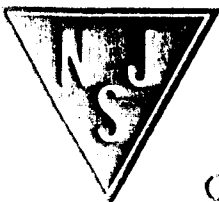
FEATURES

- Available in TO-18
- Fully characterized for "worst-case" design
- Passivated planar construction for maximum reliability and parameter uniformity — All junctions completely passivated
- Low saturation voltage and fast switching at high current levels
- 5 to 500 mA operating DC current range
- 0.15 μ S typical turn on time
- 0.7 μ S typical recovery time
- Pulse currents to 30 amps
- Voltage ratings to 100V
- 0.2 mA max. trigger current
- 0.8V max. trigger Voltage

ABSOLUTE MAXIMUM RATINGS

Continuous D.C. Forward Current,	75°C Ambient	250 mA	} Note 2
	100°C Case	500 mA	
Peak recurrent Forward Current		up to 30 amps	
Surge current, 0.05 seconds		5 amps	
Peak Gate current		250 mA	
Average Gate current		25 mA	
Reverse Gate voltage		5 volts	
Reverse Gate current		3 mA	
Storage temperature range		-65 to +200°C	
Operating temperature range		-65 to +150°C	

Note 1 Blocking voltage ratings apply over the operating temperature range, provided the gate is connected to the cathode through an appropriate resistor, or adequate gate bias is used.
 Note 2 Ambient current ratings shown apply to TO-18 units.



SPECIFICATIONS

TEST	SYMBOL	MIN.	TYPICAL	MAX.	UNITS	TEST CONDITIONS
SUBGROUP 1 Visual and Mechanical	—	—	—	—	—	MIL-STD-750 Method 2071
SUBGROUP 2 (25°C Tests)						
Forward Blocking Current	I_{FX}	—	.002	0.1	μA	$R_{GK} = 1 K, V_{FX} = \text{Rating}$
Reverse Blocking Current	I_{RX}	—	.002	0.1	μA	$R_{GK} = 1 K, V_{RX} = \text{Rating}$
Reverse Gate Voltage	BV_{KGO}	5	8	—	V	$I_{KGO} = 0.1 mA$
Gate Trigger Current	I_{GT}	-5	50	200	μA	$R_{GS} = 10 K, V_{FX} = 5V$
Gate Trigger Voltage	V_{GT}	.40	.55	.80	V	$R_{GS} = 100 \Omega, V_{FX} = 5V$
On Voltage	V_F	0.8	1.2	1.5	V	$i_F = 1 A$ (pulse test)
Holding Current	I_{HX}	0.3	1.0	5.0	mA	$R_{GK} = 1 K, V_{AA} = 5V$
SUBGROUP 3 (25°C Tests)						
Anode Voltage-Critical Rate of Rise	$dv./dt$	30	60	—	$V/\mu Sec$	$R_{GK} = 1 K, V_{FX} = 30V$
Gate Trigger-on Pulse Width	$t_{PW(on)}$	—	.07	0.2	μSec	$I_G = 10 mA, I_A = 1 A, V_{AA} = 30V$
Delay Time	t_d	—	0.1	—	μSec	$I_G = 10 mA, I_A = 1 A, V_{AA} = 30V$
Rise Time	t_r	—	0.05	—	μSec	$I_G = 10 mA, I_A = 1 A, V_{AA} = 30V$
Forward Blocking Recovery Time	t_{br}	—	0.7	2.0	μSec	$I_F = 1 A, i_R = 1 A, R_{GK} = 1 K$
SUBGROUP 4 (150°C Tests)						
High temp forward blocking current	I_{FX}	—	2	20	μA	$R_{GK} = 1 K, V_{FX} = \text{Rating}$
High temp reverse blocking current	I_{RX}	—	20	50	μA	$R_{GK} = 1 K, V_{HX} = \text{Rating}$
High temp gate trigger voltage	V_{GT}	.10	.15	0.6	V	$R_{GS} = 100 \Omega, V_{FX} = 5V$
High temp holding current	I_{HX}	.05	.30	2.0	mA	$R_{GK} = 1 K, V_{AA} = 5V$
SUBGROUP 5 (-65°C Tests)						
Low temp gate trigger voltage	V_{GT}	0.6	0.8	1.1	V	$R_{GS} = 100 \Omega, V_{FX} = 5V$
Low temp gate trigger current	I_{GT}	0	0.4	1.2	mA	$R_{GS} = 10 K, V_{FX} = 5V$
Low temp holding current	I_{HX}	0.5	5.0	10	mA	$R_{GK} = 1 K, V_{AA} = 5V$

