

2N**3870** thru 2N**3873** (SILICON)
2N**3896** thru 2N**3899**
2N**6171** thru 2N**6174**

**THYRISTORS
SILICON CONTROLLED RECTIFIERS**

... designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

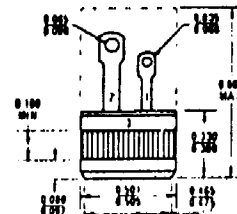
- Economical for a Wide Range of Uses
- High Surge Current - $I_{TSM} = 350$ Amp
- Practical Level Triggering and Holding Characteristics - 10 mA (Typ) @ $T_C = 25^\circ\text{C}$
- Rugged Construction in Either Pressfit, Stud or Isolated Stud Package

**THYRISTORS
PNPN**

**35 AMPERES RMS
100-600 VOLTS**



1 PIN 1 GATE
2 PIN 2 CATHODE
CASE, ANODE



**CASE 174
TO-203**

**2N3870
thru
2N3873**

An JEDEC (EIA-188) and notes apply



MAXIMUM RATINGS

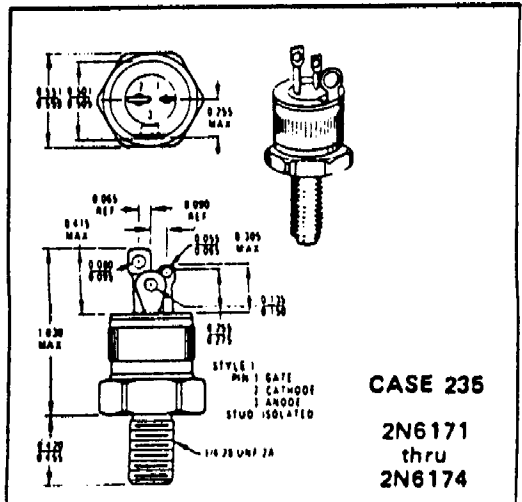
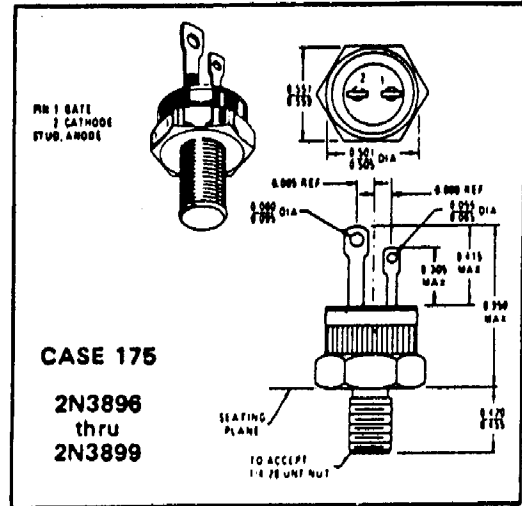
Rating	Symbol	Value	Unit
*Repetitive Peak Reverse Blocking Voltage (1) ($T_J = -40$ to $+100^\circ\text{C}$) 1/2 Sine Wave, 50 to 400 Hz, Gate Open 2N3870, 2N3896, 2N6171 2N3871, 2N3897, 2N6172 2N3872, 2N3898, 2N6173 2N3873, 2N3899, 2N6174	VDRM	100 200 400 600	Volts
*Non-Repetitive Peak Reverse Blocking Voltage ($t \leq 5.0$ ms) 2N3870, 2N3896, 2N6171 2N3871, 2N3897, 2N6172 2N3872, 2N3898, 2N6173 2N3873, 2N3899, 2N6174	VRSM	150 330 660 700	Volts
*Forward Current AVG ($T_C = -40$ to $+65^\circ\text{C}$) ($+85^\circ\text{C}$)	$I_T(\text{AV})$	22 11	Amp
*Peak Surge Current (One cycle, 60 Hz) ($T_C = +65^\circ\text{C}$)	I_{TSM}	350	Amp
Circuit Fusing Considerations ($T_J = -40$ to $+100^\circ\text{C}$) ($t = 1.0$ to 8.3 ms)	I^2t	435	A^2s
*Peak Gate Power	P_{GM}	20	Watts
*Average Gate Power	$P_{G(\text{AVG})}$	0.5	Watt
*Peak Forward Gate Current	I_{GFM}	2.0	Amp
Peak Gate Voltage	VGM	10	Volts
*Operating Junction Temperature Range	T_J	-40 to +100	$^\circ\text{C}$
*Storage Temperature Range	T_{stg}	-40 to +150	$^\circ\text{C}$
Stud Torque 2N3896 thru 2N3899 2N6171 thru 2N6174	-	30	in. lb.

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case 2N3870 thru 2N3873, 2N3896 thru 2N3899 2N6171 thru 2N6174	θ_{JC}	0.9 1.0	$^\circ\text{C}/\text{W}$

*Indicates JEDEC Registered Data.

(1) Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.



ELECTRICAL CHARACTERISTICS

At Maximum Ratings Unless Otherwise Specified and at Indicated Case Temperature (T_C)

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		FOR ALL TYPES Unless Otherwise Specified			
		MIN.	TYP.	MAX.	
Peak Off-State Current: (Gate open, $T_C = 100^\circ\text{C}$) Forward Current (I_{DOM}) at $V_D = V_{DROM}$ Reverse Current (I_{ROM}) at $V_R = V_{RROM}$ 2N3870, 2N3896, S6420A 2N3871, 2N3897, S6420B 2N3872, 2N3898, S6420D 2N3873, 2N3899, S6420M, S6400N, S6410N, S6420N	I_{DOM} or I_{ROM}	-	0.2 0.25 0.3 0.35	2* 2.5* 3* 4*	mA
Instantaneous On-State Voltage: $i_T = 69$ A (peak), $T_C = 25^\circ\text{C}$ $i_T = 100$ A (peak), $T_C = 25^\circ\text{C}$	v_T	-	- 1.7	1.85* 2.1	V
DC Gate Trigger Voltage: $V_D = 12$ V (dc), $R_L = 30 \Omega$, $T_C = -40^\circ\text{C}$ $V_D = 12$ V (dc), $R_L = 30 \Omega$, $T_C = 25^\circ\text{C}$ For other case temperatures	V_{GT}	-	1.5 1.1	3* 2	V
DC Gate Trigger Current: $V_D = 12$ V (dc), $R_L = 30 \Omega$, $T_C = 40^\circ\text{C}$ $V_D = 12$ V (dc), $R_L = 30 \Omega$, $T_C = 25^\circ\text{C}$ For other case temperatures	I_{GT}	- 1	46 25	80* 40	mA
Instantaneous Holding Current: Gate open, $T_C = 25^\circ\text{C}$ For other case temperatures	i_{HO}	0.5	30	70	mA
Gate Controlled Turn-On Time: (Delay Time + Rise Time) For $V_D = V_{DROM}$, $I_{GT} = 200$ mA, $t_r = 0.1 \mu\text{s}$, $i_T = 30$ A (peak), $T_C = 25^\circ\text{C}$ (See Fig. 12 & 14.)	t_{gt}	-	1.25	2	μs
Circuit Commutated Turn-Off Time: $V_D = V_{DROM}$, $i_T = 18$ A, pulse duration $= 50 \mu\text{s}$, $dv/dt = 20$ V/ μs , $-di/dt$ $= -30$ A/ μs , $I_{GT} = 200$ mA, $T_C = 80^\circ\text{C}$ (See Fig. 15.)	t_q	-	20	40	μs
Critical Rate of Rise of Off-State Voltage: $V_D = V_{DROM}$, exponential voltage rise, Gate open, $T_C = 100^\circ\text{C}$ (See Fig. 16.)	dv/dt	10	100	-	V/ μs
Thermal Resistance, Junction-to-Case: Steady-State Press-fit & stud types Isolated-stud types	$R_{\theta JC}$	-	-	0.9* 1	$^\circ\text{C/W}$

*In accordance with JEDEC registration data filed for the JEDEC (2N-series) types.