Intel® Core™ i7 Processor Family for the LGA-2011 Socket

Datasheet, Volume 1

Supporting Desktop Intel® Core™ i7-3960X and i7-3970X Extreme Edition Processor for the LGA-2011 Socket

Supporting Desktop Intel® Core™ i7-39xxK and i7-38xx Processor Series for the LGA-2011 Socket

This is volume 1 of 2.

February 2014

Reference Number: 326196-003

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Revision History

Revision Number	Description	Revision Date
001	• Initial Release	November 2011
002	• Updated to clarify references to PCI Express* • Added Intel® Core™ i7-3970X Extreme Edition processor	November 2012
003	• Updated Table 4-9, “Package C-State Power Specifications”	February 2014

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1 Introduction

The Intel® Core™ i7 processor family for the LGA-2011 socket is the next generation of 64-bit, multi-core desktop processor built on 32-nanometer process technology. Based on the low-power/high performance Intel® Core™ i7 processor microarchitecture, the processor is designed for a two-chip platform as opposed to the traditional three-chip platforms (processor, MCH, and ICH). The two-chip platform consists of a processor and the Platform Controller Hub (PCH) and enables higher performance, easier validation, and improved x-y footprint. Refer to Figure 1-1 for a block diagram of the processor platform.

The processor features up to 40 lanes of PCI Express* links capable of up to 8.0 GT/s, and 4 lanes of DMI2/PCI Express* 2.0 interface with a peak transfer rate of 5.0 GT/s. The processor supports up to 46 bits of physical address space and 48 bits of virtual address space.

Included in this family of processors is an integrated memory controller (IMC) and integrated I/O (IIO) (such as PCI Express* and DMI2) on a single silicon die. This single die solution is known as a monolithic processor.

This document is Volume 1 of the datasheet for the Intel® Core™ i7 processor family for the LGA-2011 socket. The complete datasheet consists of two volumes. This document provides DC electrical specifications, land and signal definitions, interface functional descriptions, power management descriptions, and additional feature information pertinent to the implementation and operation of the processor on its platform. Volume 2 provides register information. Refer to Section 1.7, "Related Documents" for access to Volume 2.

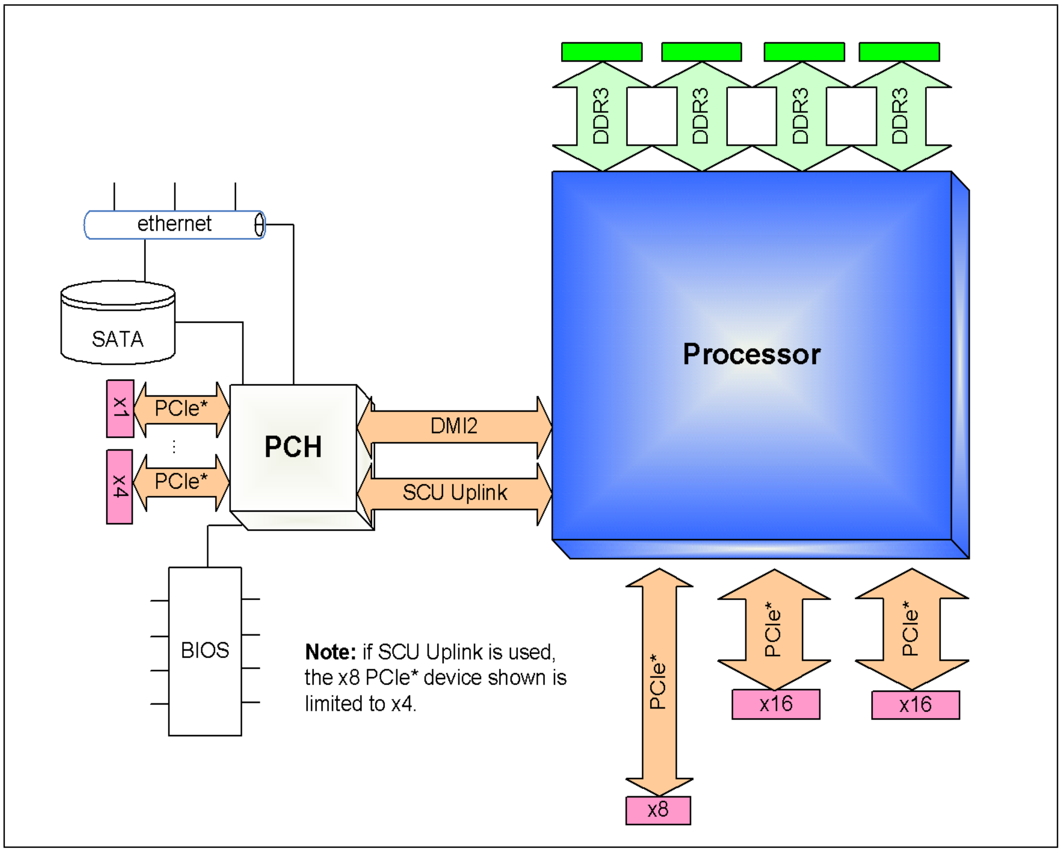
Note: Throughout this document, the Intel® Core™ i7 processor family for the LGA-2011 socket may be referred to as "processor".

Note: Throughout this document, the Desktop Intel® Core™ i7-39xxK processor series for the LGA-2011 socket refers to the i7-3930K.

Note: Throughout this document, the Desktop Intel® Core™ i7-38xx processor series for the LGA-2011 socket refers to the i7-3820.

Note: Throughout this document, the Intel® X79 Chipset Platform Controller Hub may be referred to as "PCH".

Figure 1-1. Processor Platform Block Diagram Example



1.1 Processor Feature Details

- Up to 6 Execution Cores
- Each core supports two threads (Intel® Hyper-Threading Technology) for up to 12 threads
- A 32-KB instruction and 32-KB data first-level cache (L1) for each core
- A 256-KB shared instruction/data mid-level (L2) cache for each core
- Up to 15 MB last level cache (LLC): up to 2.5 MB per core instruction/data last level cache (LLC), shared among all cores

1.1.1 Supported Technologies

- Intel® Virtualization Technology (Intel® VT)
- Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Intel® Virtualization Technology Intel® Core™ i7 processor family for the LGA-2011 socket Extensions
- Intel® 64 Architecture
- Intel® Streaming SIMD Extensions 4.1 (Intel® SSE4.1)
- Intel® Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® Advanced Vector Extensions (Intel® AVX)
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Execute Disable Bit
- Intel® Turbo Boost Technology
- Enhanced Intel® SpeedStep® Technology

1.2 Interfaces

1.2.1 System Memory Support

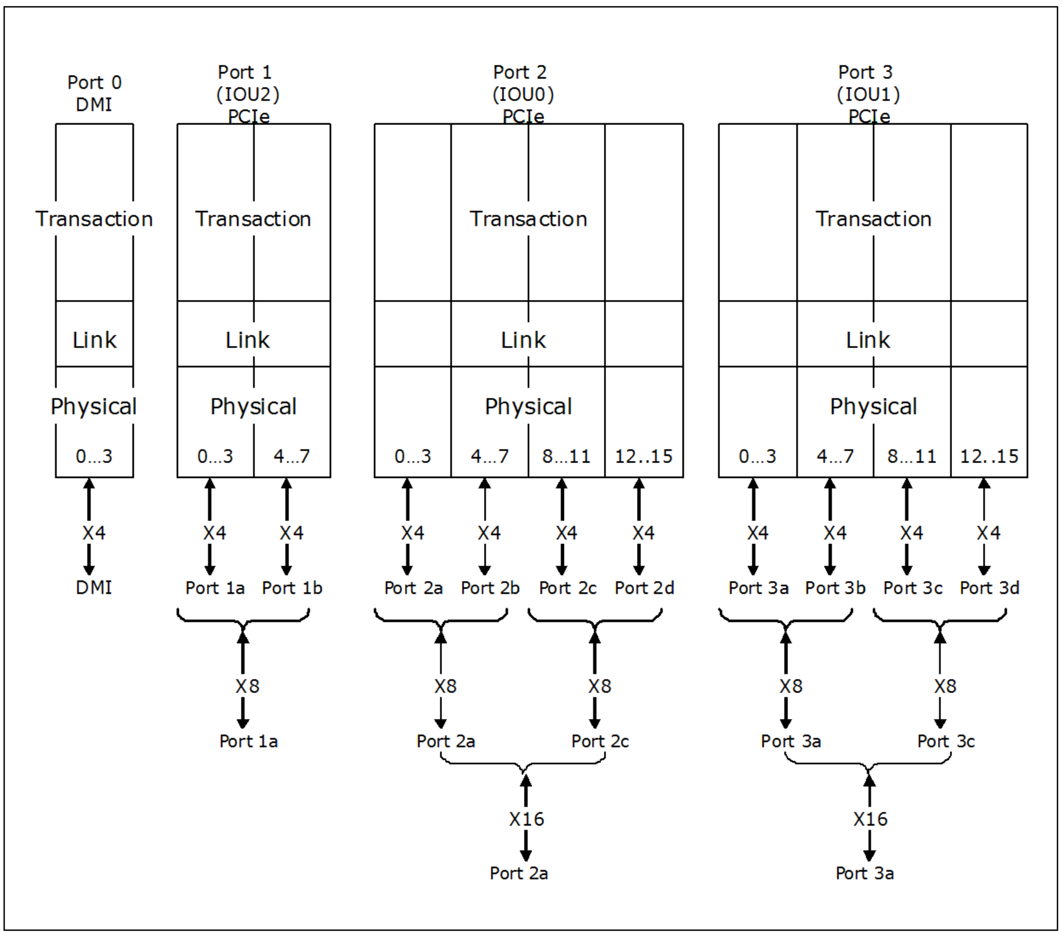
- The processor supports 4 DDR3 channels with 1 unbuffered DIMM per channel
- Unbuffered DDR3 DIMMs supported
- Data burst length of eight cycles for all memory organization modes
- Memory DDR3 data transfer rates of 1066, 1333, and 1600 MT/s
- DDR3 UDIMM standard I/O Voltage of 1.5 V
- 1-Gb, 2-Gb, and 4-Gb DDR3 DRAM technologies supported for these devices:
  — UDIMMs x8, x16
- Up to 2 ranks supported per memory channel, 1 or 2 ranks per DIMM
- Open with adaptive idle page close timer or closed page policy
- Command launch modes of 1n/2n
- Improved Thermal Throttling with dynamic CLTT
- Memory thermal monitoring support for DIMM temperature using two memory signals, MEM_HOT

1.2.2 PCI Express*

- Support for PCI Express* 2.0 (5.0 GT/s), PCI Express* (2.5 GT/s), and capable of up to PCI Express* 8.0 GT/s.
- Up to 40 lanes of PCI Express* interconnect for general purpose PCI Express devices capable of up to 8.0 GT/s speeds that are configurable for up to 10 independent ports.
- Negotiating down to narrower widths is supported, see Figure 1-2
  — x16 port (Port 2 & Port 3) may negotiate down to x8, x4, x2, or x1
  — x8 port (Port 1) may negotiate down to x4, x2, or x1
  — x4 port (Port 0) may negotiate down to x2, or x1
  — When negotiating down to narrower widths, there are caveats as to how lane reversal is supported
- Address Translation Services (ATS) 1.0 support
- Hierarchical PCI-compliant configuration mechanism for downstream devices
- Traditional PCI style traffic (asynchronous snooped, PCI ordering)
- PCI Express* extended configuration space. The first 256 bytes of configuration space aliases directly to the PCI compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
- PCI Express* Enhanced Access Mechanism. Accessing the device configuration space in a flat memory mapped fashion.

- Supports receiving and decoding 64 bits of address from PCI Express*
  - Memory transactions received from PCI Express* that go above the top of physical address space (when Intel VT-d is enabled, the check would be against the translated HPA (Host Physical Address) address) are reported as errors by the processor.
  - Outbound access to PCI Express* will always have address bits 63 to 46 cleared
- Re-issues Configuration cycles that have been previously completed with the Configuration Retry status
- Power Management Event (PME) functions
- Message Signaled Interrupt (MSI and MSI-X) messages
- Degraded Mode support and Lane Reversal support
- Static lane numbering reversal and polarity inversion support

Figure 1-2. PCI Express* Lane Partitioning and Direct Media Interface Gen 2 (DMI2)



1.2.3 Direct Media Interface Gen 2 (DMI2)

- Serves as the chip-to-chip interface to the PCH
- The DMI2 port supports x4 link width and only operates in a x4 mode when in DMI2
- Operates at PCIe2 or PCIe1 speeds
- Transparent to software
- Processor and peer-to-peer writes and reads with 64-bit address support
- APIC and Message Signaled Interrupt (MSI) support. Will send Intel-defined “End of Interrupt” broadcast message when initiated by the processor.
- System Management Interrupt (SMI), SCI, and SERR error indication
- Static lane numbering reversal support
- Supports DMI2 virtual channels VC0, VC1, VCm, and VCp

1.2.4 Platform Environment Control Interface (PECI)

The PECI is a one-wire interface that provides a communication channel between a PECI client (the processor) and a PECI master (the PCH). Refer to the processor Thermal Mechanical Specification and Design Guide (see Section 1.7, “Related Documents”) for additional details on PECI services available in the processor.

- Supports operation at up to 2 Mbps data transfers
- Link layer improvements to support additional services and higher efficiency over PECI 2.0 generation
- Services include processor thermal and estimated power information, control functions for power limiting, P-state and T-state control, and access for Machine Check Architecture registers and PCI configuration space (both within the processor package and downstream devices)
- Single domain (Domain 0) is supported

1.3 Power Management Support

1.3.1 Processor Package and Core States

- ACPI C-states as implemented by the following processor C-states
  - Package: PC0, PC1/PC1E, PC2, PC3, PC6 (Package C7 is not supported)
  - Core: CC0, CC1, CC1E, CC3, CC6, CC7
- Enhanced Intel SpeedStep® Technology

1.3.2 System States Support

- S0, S1, S3, S4, S5

1.3.3 Memory Controller

- Multiple CKE power down modes
- Multiple self-refresh modes
- Memory thermal monitoring using MEM_HOT_C01_N and MEM_HOT_C23_N Signals

1.3.4 PCI Express*

- L0s and L1 ASPM power management capability

1.4 Thermal Management Support

- Adaptive Thermal Monitor
- THERMTRIP_N and PROCHOT_N signal support
- On-Demand mode clock modulation
- Open Loop Thermal Throttling and Hybrid OLTT/CLTT support for system memory
- Fan speed control with DTS
- Two integrated SMBus masters for accessing thermal data from DIMMs
- New Memory Thermal Throttling features using MEM_HOT signals

1.5 Package Summary

The processor socket type is noted as LGA2011. The processor package is a 52.5 x 45 mm FC-LGA package (LGA2011). Refer to the processor Thermal Mechanical Specification and Design Guide (see Section 1.7, "Related Documents") for the package mechanical specifications.

1.6 Terminology

Table 1-1. Terminology (Sheet 1 of 3)

Term	Description
ASPM	Active State Power Management
Cbo	Cache and Core Box. It is a term used for internal logic providing ring interface to LLC and Core.
DDR3	Third generation Double Data Rate SDRAM memory technology that is the successor to DDR2 SDRAM
DMA	Direct Memory Access
DMI	Direct Media Interface
DMI2	Direct Media Interface Gen 2
DTS	Digital Thermal Sensor
ECC	Error Correction Code
Enhanced Intel® SpeedStep® Technology	Allows the operating system to reduce power consumption when performance is not needed.
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
Functional Operation	Refers to the normal operating conditions in which all processor specifications, including DC, AC, system bus, signal quality, mechanical, and thermal, are satisfied.
Integrated Memory Controller (IMC)	A Memory Controller that is integrated in the processor die.
Integrated I/O Controller (IIO)	An I/O controller that is integrated in the processor die.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture. Further details on Intel 64 architecture and programming model can be found at http://developer.intel.com/technology/intel64/.
Intel® Turbo Boost Technology	Intel® Turbo Boost Technology is a way to automatically run the processor core faster than the marked frequency if the part is operating under power, temperature, and current specifications limits of the Thermal Design Power (TDP). This results in increased performance of both single and multi-threaded applications.

Table 1-1. Terminology (Sheet 2 of 3)

Term	Description
Intel® Virtualization Technology (Intel® VT)	Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
Intel® VT-d	Intel® Virtualization Technology (Intel® VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
Integrated Heat Spreader (IHS)	A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
Jitter	Any timing variation of a transition edge or edges from the defined Unit Interval (UI).
IOV	I/O Virtualization
LGA2011 Socket	The 2011-land FC-LGA package mates with the system board through this surface mount, 2011-contact socket.
LLC	Last Level Cache
ME	Management Engine
NCTF	Non-Critical to Function: NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
Intel® Core™ i7 processor family for the LGA-2011 socket	Intel's 32-nm processor design, follow-on to the 32-nm 2nd Generation Intel® Core™ processor family desktop design.
PCH	Platform Controller Hub. The next generation chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features.
PCU	Power Control Unit.
PCIe*	PCI Express*
PECI	Platform Environment Control Interface
Processor	The 64-bit, single-core or multi-core component (package)
Processor Core	The term "processor core" refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache. All DC and AC timing and signal integrity specifications are measured at the processor die (pads), unless otherwise noted.
PCU	Uncore Power Manager
Rank	A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DDR3 DIMM.
SCI	System Control Interrupt. Used in ACPI protocol.
SSE	Intel® Streaming SIMD Extensions (Intel® SSE)
SKU	A processor Stock Keeping Unit (SKU) to be installed in the platform. Electrical, power and thermal specifications for these SKU's are based on specific use condition assumptions.
SMBus	System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system. It is based on the principals of the operation of the I2C* two-wire serial bus from Philips Semiconductor.
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant
TDP	Thermal Design Power
TSOD	Thermal Sensor on DIMM
UDIMM	Unbuffered Dual In-line Module

Table 1-1. Terminology (Sheet 3 of 3)

Term	Description
Unit Interval	Signaling convention that is binary and unidirectional. In this binary signaling, one bit is sent for every edge of the forwarded clock, whether it be a rising edge or a falling edge. If a number of edges are collected at instances t_1, t_2, t_n,...., t_k then the UI at instance "n" is defined as: $UI_n = t_n - t_{n-1}$
V_{CC}	Processor core power supply
V_{SS}	Processor ground
VCCD_01, VCCD_23	Power supply for the processor system memory interface. VCCD is the generic term for VCCD_01, VCCD_23.
x1	Refers to a Link or Port with one Physical Lane
x4	Refers to a Link or Port with four Physical Lanes
x8	Refers to a Link or Port with eight Physical Lanes
x16	Refers to a Link or Port with sixteen Physical Lanes

1.7 Related Documents

Refer to the following documents for additional information.

Table 1-2. Reference Documents

Document	Document Number/ Location
Intel® Core™ i7 Processor Family for the LGA-2011 Socket Datasheet, Volume 2	326197
Intel® Core™ i7 Processor Family for the LGA-2011 Socket Specification Update	326198
Desktop Intel® Core™ i7 Processor Family for the LGA-2011 Socket Thermal Mechanical Specifications and Design Guide	326199
Intel® C600 Series Chipset and Intel® X79 Express Chipset Datasheet	326514
Intel® C600 Series Chipset and Intel® X79 Express Chipset Specification Update	326515
Intel® X79 Express Chipset Thermal Mechanical Specifications and Design Guide	326202
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info
PCI Local Bus Specification	http://www.pcisig.com/specifications
PCI Express Base Specification*	http://www.pcisig.com
System Management Bus (SMBus) Specification	http://smbus.org/
DDR3 SDRAM Specification	http://www.jedec.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals • Volume 1: Basic Architecture • Volume 2A: Instruction Set Reference, A-M • Volume 2B: Instruction Set Reference, N-Z • Volume 3A: System Programming Guide • Volume 3B: System Programming Guide *Intel® 64 and IA-32 Architectures Optimization Reference Manual*	http://www.intel.com/products/processor/manuals/index.htm
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	http://download.intel.com/technology/computing/vptech/Intel(r)_VT_for_Direct_IO.pdf

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2 Interfaces

This chapter describes the functional behaviors supported by the processor.

2.1 System Memory Interface

2.1.1 System Memory Technology Support

The Integrated Memory Controller (IMC) supports DDR3 protocols with four independent 64-bit memory channels and supports 1 unbuffered DIMM per channel.

2.1.2 System Memory Timing Support

The IMC supports the following DDR3 Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1n indicates a new command may be issued every clock and 2n indicates a new command may be issued every 2 clocks. Command launch mode programming depends on the transfer rate and memory configuration.

2.2 PCI Express* Interface

This section describes the PCI Express* interface capabilities of the processor. See the *PCI Express* Base Specification* for details of PCI Express*.

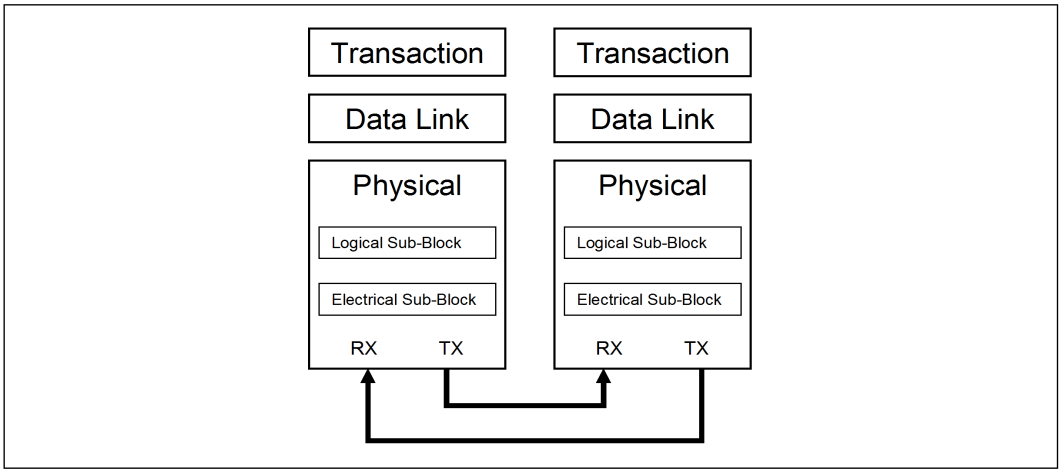
Note: The processor is capable of up to 8.0 GT/s speeds.

2.2.1 PCI Express* Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification.

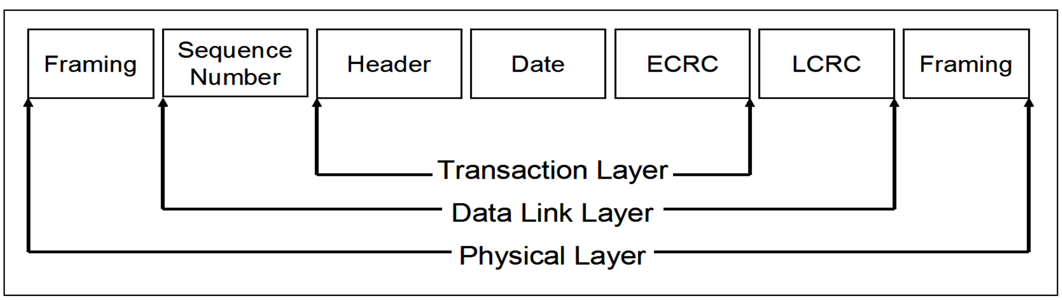
The PCI Express architecture is specified in three layers — Transaction Layer, Data Link Layer, and Physical Layer. The partitioning in the component is not necessarily along these same boundaries. Refer to Figure 2-1 for the PCI Express Layering Diagram.

Figure 2-1. PCI Express* Layering Diagram



PCI Express uses packets to communicate information between components. Packets are formed in the Transaction and Data Link Layers to carry the information from the transmitting component to the receiving component. As the transmitted packets flow through the other layers, they are extended with additional information necessary to handle packets at those layers. At the receiving side, the reverse process occurs and packets get transformed from their Physical Layer representation to the Data Link Layer representation and finally (for Transaction Layer Packets) to the form that can be processed by the Transaction Layer of the receiving device.

Figure 2-2. Packet Flow through the Layers



2.2.1.1 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

2.2.1.2 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

The transmission side of the Data Link Layer accepts TLPs assembled by the Transaction Layer, calculates and applies data protection code and TLP sequence number, and submits them to Physical Layer for transmission across the Link. The receiving Data Link Layer is responsible for checking the integrity of received TLPs and for submitting them to the Transaction Layer for further processing. On detection of TLP error(s), this layer is responsible for requesting retransmission of TLPs until information is correctly received, or the Link is determined to have failed. The Data Link Layer also generates and consumes packets which are used for Link management functions.

2.2.1.3 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry. It also includes logical functions related to interface initialization and maintenance. The Physical Layer exchanges data with the Data Link Layer in an implementation-specific format, and is responsible for converting this to an appropriate serialized format and transmitting it across the PCI Express Link at a frequency and width compatible with the remote device.

2.2.2 PCI Express* Configuration Mechanism

The PCI Express link is mapped through a PCI-to-PCI bridge structure.

PCI Express extends the configuration space to 4096 bytes per-device/function, as compared to 256 bytes allowed by the *Conventional PCI Specification*. PCI Express configuration space is divided into a PCI-compatible region (which consists of the first 256 bytes of a logical device's configuration space) and an extended PCI Express region (which consists of the remaining configuration space). The PCI-compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express configuration access mechanism described in the PCI Express Enhanced Configuration Mechanism section.

The PCI Express Host Bridge is required to translate the memory-mapped PCI Express configuration space accesses from the host processor to PCI Express configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only.

See the *PCI Express* Base Specification* for details of both the PCI-compatible and PCI Express Enhanced configuration mechanisms and transaction rules.

2.3 DMI2/PCI Express* Interface

Direct Media Interface 2 (DMI2) connects the processor to the Platform Controller Hub (PCH). DMI2 is similar to a four-lane PCI Express supporting a speed of 5 GT/s per lane. Refer to Section 6.3, "DMI2 / PCI Express* Port 0 Signals" for additional details.

Note: Only DMI2 x4 configuration is supported.

2.3.1 DMI2 Error Flow

DMI2 can only generate SERR in response to errors; never SCI, SMI, MSI, PCI INT, or GPE. Any DMI2 related SERR activity is associated with Device 0.

2.3.2 DMI2 Link Down

The DMI2 link going down is a fatal, unrecoverable error. If the DMI2 data link goes to data link down, after the link was up, then the DMI2 link hangs the system by not allowing the link to retrain to prevent data corruption. This is controlled by the PCH.

Downstream transactions that had been successfully transmitted across the link prior to the link going down may be processed as normal. No completions from downstream, non-posted transactions are returned upstream over the DMI2 link after a link down event.

2.4 Platform Environment Control Interface (PECI)

The Platform Environment Control Interface (PECI) uses a single wire for self-clocking and data transfer. The bus requires no additional control lines. The physical layer is a self-clocked one-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a logic ‘0’ or logic ‘1’. PECI also includes variable data transfer rate established with every message. In this way, it is highly flexible even though underlying logic is simple.

The interface design was optimized for interfacing to Intel processor and chipset components in both single processor and multiple processor environments. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information. Refer to the processor Thermal Mechanical Specification and Design Guide (see Section 1.7, “Related Documents”) for additional details regarding PECI and for a list of supported PECI commands.

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3 Technologies

3.1 Intel® Virtualization Technology (Intel® VT)

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets.

- **Intel® Virtualization Technology (Intel® VT) for Intel® 64 and IA-32 Intel® Architecture (Intel® VT-x)** adds hardware support in the processor to improve the virtualization performance and robustness. Intel VT-x specifications and functional descriptions are included in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B and is available at http://www.intel.com/products/processor/manuals/index.htm
- **Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)** adds processor and uncore hardware implementations to support and improve I/O virtualization performance and robustness. The Intel VT-d specification and other Intel VT documents can be referenced at http://www.intel.com/technology/virtualization/index.htm

3.1.1 Intel® Virtualization Technology (Intel® VT) for Intel® 64 and IA-32 Intel® Architecture (Intel® VT-x) Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide improved reliable virtualized platform. By using Intel VT-x, a VMM is:

- **Robust:** VMMs no longer need to use para-virtualization or binary translation. This means that they will be able to run off-the-shelf operating systems and applications without any special steps.
- **Enhanced:** Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- **More reliable:** Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- **More secure:** The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

3.1.2 Intel® Virtualization Technology (Intel® VT) for Intel® 64 and IA-32 Intel® Architecture (Intel® VT-x) Features

The processor core supports the following Intel VT-x features:

- Extended Page Tables (EPT)
  - hardware assisted page table virtualization
  - eliminates VM exits from guest OS to the VMM for shadow page-table maintenance
- Virtual Processor IDs (VPID)
  - Ability to assign a VM ID to tag processor core hardware structures (such as, TLBs)
  - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
  - Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest
  - The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees
- Descriptor-Table Exiting
  - Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
  - A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

3.1.3 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) Objectives

The key Intel VT-d objectives are abstraction and robustness. Hardware abstraction has two key benefits. First is partitioning hardware into configurable isolated environments called domains to which a subset of host physical memory is allocated. Second is greater flexibility in modifying hardware capability without direct operating system interference. Virtualization allows for the creation of one or more partitions on a single system. This could be multiple partitions in the same operating system, or there can be multiple operating system instances running on the same system. The VT-d architecture provides the flexibility to support multiple usage models and in turn complement Intel VT-x capability. This offers benefits such as system consolidation, legacy migration, activity partitioning, or security. The second objective is robustness. VT-d enables protected access to I/O devices from a given virtual machine so that it does not interfere with a different virtual machine on the same platform. Any errors or permission violation are trapped and hence the system is more robust.

3.1.3.1 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) Features Supported

The processor supports the following Intel VT-d features:

- Root entry, context entry, and default context
- Support for 4-K page sizes only
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults
  - Support for fault collapsing based on Requester ID
- Support for both leaf and non-leaf caching
- Support for boot protection of default page table
  - Support for non-caching of invalid page table entries
- Support for hardware based flushing of translated but pending writes and pending reads upon IOTLB invalidation
- Support for page-selective IOTLB invalidation
- Support for ARI (Alternative Requester ID – a PCI SIG ECR for increasing the function number count in a PCIe device) to support IOV devices

3.1.3.2 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) Processor Feature Additions

The following are new features supported in Intel VT-d on the processor:

- Improved invalidation architecture
- End point caching support (Address Translation Services)
- Interrupt remapping
- 2M/1G/512G super page support

3.1.4 Intel® Virtualization Technology Processor Extensions

The processor supports the following Intel VT Intel® Core™ i7 processor family for the LGA-2011 socket Extensions features:

- Large Intel VT-d Pages
  - Adds 2 MB and 1 GB page sizes to Intel VT-d implementations
  - Matches current support for Extended Page Tables (EPT)
  - Ability to share CPU's EPT page-table (with super-pages) with Intel VT-d
  - Benefits:
    - Less memory foot-print for I/O page-tables when using super-pages
    - Potential for improved performance – Due to shorter page-walks, allows hardware optimization for IOTLB
- Transition latency reductions expected to improve virtualization performance without the need for VMM enabling. This reduces the VMM overheads further and increase virtualization performance.

3.2 Security Technologies

3.2.1 Intel® AES New Instructions (Intel® AES-NI)

These instructions enable fast and secure data encryption and decryption using the Advanced Encryption Standard (AES), which is defined by FIPS Publication number 197. Since AES is the dominant block cipher, and it is deployed in various protocols, the new instructions will be valuable for a wide range of applications.

The architecture consists of six instructions that offer full hardware support for AES. Four instructions support the AES encryption and decryption, and the other two instructions support the AES key expansion. Together, they offer a significant increase in performance compared to pure software implementations.

The AES instructions have the flexibility to support all three standard AES key lengths, all standard modes of operation, and even some nonstandard or future variants.

Beyond improving performance, the AES instructions provide important security benefits. Since the instructions run in data-independent time and do not use lookup tables, they help in eliminating the major timing and cache-based attacks that threaten table-based software implementations of AES. In addition, these instructions make AES simple to implement, with reduced code size. This helps reducing the risk of inadvertent introduction of security flaws, such as difficult-to-detect side channel leaks.

3.2.2 Execute Disable Bit

Intel's Execute Disable Bit functionality can help prevent certain classes of malicious buffer overflow attacks when combined with a supporting operating system:

- Allows the processor to classify areas in memory by where application code can execute and where it cannot.
- When a malicious worm attempts to insert code in the buffer, the processor disables code execution, preventing damage and worm propagation.

3.3 Intel® Hyper-Threading Technology (Intel® HT Technology)

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology) that allows an execution core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

For more information on Intel Hyper-Threading Technology, see http://www.intel.com/technology/platform-technology/hyper-threading/.

3.4 Intel® Turbo Boost Technology

Intel Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating frequency if it is operating below power, temperature, and current limits. The result is increased performance in multi-threaded and single threaded workloads. It should be enabled in the BIOS for the processor to operate with maximum performance.

3.4.1 Intel® Turbo Boost Operating Frequency

The processor's rated frequency assumes that all execution cores are running an application at the thermal design power (TDP). However, under typical operation, not all cores are active. Therefore, most applications are consuming less than the TDP at the rated frequency. To take advantage of the available TDP headroom, the active cores can increase their operating frequency.

To determine the highest performance frequency amongst active cores, the processor takes the following into consideration:

- The number of cores operating in the C0 state.
- The estimated current consumption.
- The estimated power consumption.
- The temperature.

Any of these factors can affect the maximum frequency for a given workload. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

Note: Intel Turbo Boost Technology is only active if the operating system is requesting the P0 state. For more information on P-states and C-states, refer to Chapter 4, "Power Management".

3.5 Enhanced Intel® SpeedStep® Technology

The processor supports Enhanced Intel SpeedStep Technology (EIST) as an advanced means of enabling very high performance while also meeting the power-conservation needs of the platform.

Enhanced Intel SpeedStep Technology builds upon that architecture using design strategies that include the following:

- **Separation between Voltage and Frequency Changes**. By stepping voltage up and down in small increments separately from frequency changes, the processor can reduce periods of system unavailability (which occur during frequency change). Thus, the system can transition between voltage and frequency states more often, providing improved power/performance balance.
- **Clock Partitioning and Recovery**. The bus clock continues running during state transition, even when the core clock and Phase-Locked Loop are stopped, which allows logic to remain active. The core clock can also restart more quickly under Enhanced Intel SpeedStep Technology.

For additional information on Enhanced Intel SpeedStep Technology, see Section 4.2.1.

3.6 Intel® Advanced Vector Extensions (Intel® AVX)

Intel® Advanced Vector Extensions (Intel® AVX) is a new 256-bit vector SIMD extension of Intel Architecture. The introduction of Intel AVX starts with the 2nd Generation Intel® Core™ Processor Family Desktop. Intel AVX accelerates the trend of parallel computation in general purpose applications like image, video, and audio processing, engineering applications such as 3D modeling and analysis, scientific simulation, and financial analysts.

Intel AVX is a comprehensive ISA extension of the Intel 64 Architecture. The main elements of Intel AVX are:

- Support for wider vector data (up to 256-bit) for floating-point computation
- Efficient instruction encoding scheme that supports 3 operand syntax and headroom for future extensions
- Flexibility in programming environment, ranging from branch handling to relaxed memory alignment requirements
- New data manipulation and arithmetic compute primitives, including broadcast, permute, fused-multiply-add, etc

The key advantages of Intel AVX are:

- **Performance** – Intel AVX can accelerate application performance using data parallelism and scalable hardware infrastructure across existing and new application domains:
  - — 256-bit vector data sets can be processed up to twice the throughput of 128-bit data sets
  - — Application performance can scale up with number of hardware threads and number of cores
- **Power Efficiency** – Intel AVX is extremely power efficient. Incremental power is insignificant when the instructions are unused or scarcely used. Combined with the high performance that it can deliver, applications that lend themselves heavily to using Intel AVX can be much more energy efficient and realize a higher performance-per-watt.
- **Extensibility** – Intel AVX has built-in extensibility for the future vector extensions:
  - — OS context management for vector-widths beyond 256 bits is streamlined
  - — Efficient instruction encoding allows unlimited functional enhancements:
    - Vector width support beyond 256 bits
    - 256-bit Vector Integer processing
    - Additional computational and/or data manipulation primitives.
- **Compatibility** – Intel AVX is backward compatible with previous ISA extensions including Intel SSE4:
  - — Existing Intel SSE applications/library can:
    - Run unmodified and benefit from processor enhancements
    - Recompile existing Intel SSE intrinsic using compilers that generate Intel AVX code
    - Inter-operate with library ported to Intel AVX
  - — Applications compiled with Intel AVX can inter-operate with existing Intel SSE libraries

§

4 Power Management

This chapter provides information on the following power management topics:

- Advanced Configuration and Power Interface (ACPI) States
- System States
- Processor Core/Package States
- Integrated Memory Controller (IMC) and System Memory States
- Direct Media Interface Gen 2 (DMI2)/PCI Express* Link States

4.1 Advanced Configuration and Power Interface (ACPI) States Supported

The ACPI states supported by the processor are described in this section.

4.1.1 System States

Table 4-1. System States

State	Description
G0/S0	Full On
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).
G2/S5	Soft off. All power lost (except wakeup on PCH). Total reboot.
G3	Mechanical off. All power removed from system.

4.1.2 Processor Package and Core States

Table 4-2 lists the package C-state support as:

- the shallowest core C-state that allows entry into the package C-state
- the additional factors that will restrict the state from going any deeper
- the actions taken with respect to the Ring Vcc, PLL state, and LLC.

Table 4-3 lists the processor core C-states support.

Table 4-2. Package C-State Support

Package C-State	Core States	Limiting Factors	Retention and PLL-Off	LLC Fully Flushed	Notes[1]
PC0 – Active	CC0	N/A	No	No	2
PC2 – Snoopable Idle	CC3–CC7	• PCIe/PCH and Remote Socket Snoops • PCIe/PCH and Remote Socket Accesses • Interrupt response time requirement • DMI Sidebands • Configuration Constraints	VccMin Freq = MinFreq PLL = ON	No	2
PC3 – Light Retention	at least one Core in C3	• Core C-state • Snoop Response Time • Interrupt Response Time • Non Snoop Response Time	Vcc = retention PLL = OFF	No	2,3,4
PC6 – Deeper Retention	CC6–CC7	• LLC ways open • Snoop Response Time • Non Snoop Response Time • Interrupt Response Time	Vcc = retention PLL = OFF	No	2,3,4

Notes:
1. Package C7 is not supported.
2. All package states are defined to be "E" states – such that they always exit back into the LFM point upon execution resume.
3. The mapping of actions for PC3, and PC6 are suggestions – microcode will dynamically determine which actions should be taken based on the desired exit latency parameters.
4. CC3/CC6 will all use a voltage below the VccMin operational point. The exact voltage selected will be a function of the snoop and interrupt response time requirements made by the devices (PCIe* and DMI) and the operating system.

Table 4-3. Core C-State Support

Core C-State	Global Clock	PLL	L1/L2 Cache	Core VCC	Context
CC0	Running	On	Coherent	Active	Maintained
CC1	Stopped	On	Coherent	Active	Maintained
CC1E	Stopped	On	Coherent	Request LFM	Maintained
CC3	Stopped	On	Flushed to LLC	Request Retention	Maintained
CC6	Stopped	On	Flushed to LLC	Power Gate	Flushed to LLC
CC7	Stopped	Off	Flushed to LLC	Power Gate	Flushed to LLC

4.1.3 Integrated Memory Controller States

Table 4-4. System Memory Power States

State	Description
Power Up/Normal Operation	CKE asserted. Active Mode, highest power consumption.
CKE Power Down	Opportunistic, per rank control after idle time: • Active Power Down (APD) (default mode) — CKE de-asserted. Power savings in this mode, relative to active idle state is about 55% of the memory power. Exiting this mode takes 3–5 DCLK cycles. • Pre-charge Power Down Fast Exit (PPDF) — CKE de-asserted. DLL-On. Also known as Fast CKE. Power savings in this mode, relative to active idle state, is about 60% of the memory power. Exiting this mode takes 3–5 DCLK cycles. • Pre-charge Power Down Slow Exit (PPDS) — CKE de-asserted. DLL-Off. Also known as Slow CKE. Power savings in this mode, relative to active idle state, is about 87% of the memory power. Exiting this mode takes 3–5 DCLK cycles until the first command is allowed and 16 cycles until first data is allowed. • Register CKE Power Down — IBT-ON mode: Both CKE's are de-asserted, the Input Buffer Terminators (IBTs) are left "on". — IBT-OFF mode: Both CKE's are de-asserted, the Input Buffer Terminators (IBTs) are turned "off".
Self-Refresh	CKE de-asserted. In this mode, no transactions are executed and the system memory consumes the minimum possible power. Self refresh modes apply to all memory channels for the processor. • IO-MDLL Off: Option that sets the IO master DLL off when self refresh occurs. • PLL Off: Option that sets the PLL off when self refresh occurs. In addition, the register component found on registered DIMMs (RDIMMs) is complemented with the following power down states: • Self Refresh — Clock Stopped Power Down with IBT-On — Clock Stopped Power Down with IBT-Off

4.1.4 DMI2 / PCI Express* Link States

Table 4-5. DMI2/PCI Express* Link States

State	Description
L0	Full on – Active transfer state.
L1[1]	Lowest Active State Power Management (ASPM) - Longer exit latency.

Notes:

1. L1 is only supported when the DMI2/PCI Express port is operating as a PCI Express port.

4.1.5 G, S, and C State Combinations

Table 4-6. G, S, and C State Combinations

Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C6/C7	Deep Power Down	On	Deep Power Down
G1	S3	Power off	—	Off, except RTC	Suspend to RAM
G1	S4	Power off	—	Off, except RTC	Suspend to Disk
G2	S5	Power off	—	Off, except RTC	Soft Off
G3	NA	Power off	—	Power off	Hard off

4.2 Processor Core / Package Power Management

While executing code, Enhanced Intel SpeedStep® Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, lower power C-states have longer entry and exit latencies.

4.2.1 Enhanced Intel® SpeedStep® Technology

The following are the key features of Enhanced Intel SpeedStep® Technology:

- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on temperature, leakage, power delivery loadline, and dynamic capacitance.
  — If the target frequency is higher than the current frequency, V_{CC} is ramped up to an optimized voltage. This voltage is signaled by the SVID Bus to the voltage regulator. Once the voltage is established, the PLL locks on to the target frequency.
  — If the target frequency is lower than the current frequency, the PLL locks to the target frequency, then transitions to a lower voltage by signaling the target voltage on the SVID Bus.
  — All active processor cores share the same frequency and voltage. In a multi-core processor, the highest frequency P-state requested amongst all active cores is selected.
  — Software-requested transitions are accepted at any time. The processor has a new capability from the previous processor generation, it can preempt the previous transition and complete the new request without waiting for this request to complete.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of transitions per-second are possible.

4.2.2 Low-Power Idle States

When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, higher C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor core, and processor package level. Thread level C-states are available if Hyper-Threading Technology is enabled. Entry and exit of the C-States at the thread and core level are shown in Figure 4-2.

Figure 4-1. Idle Power Management Breakdown of the Processor Cores

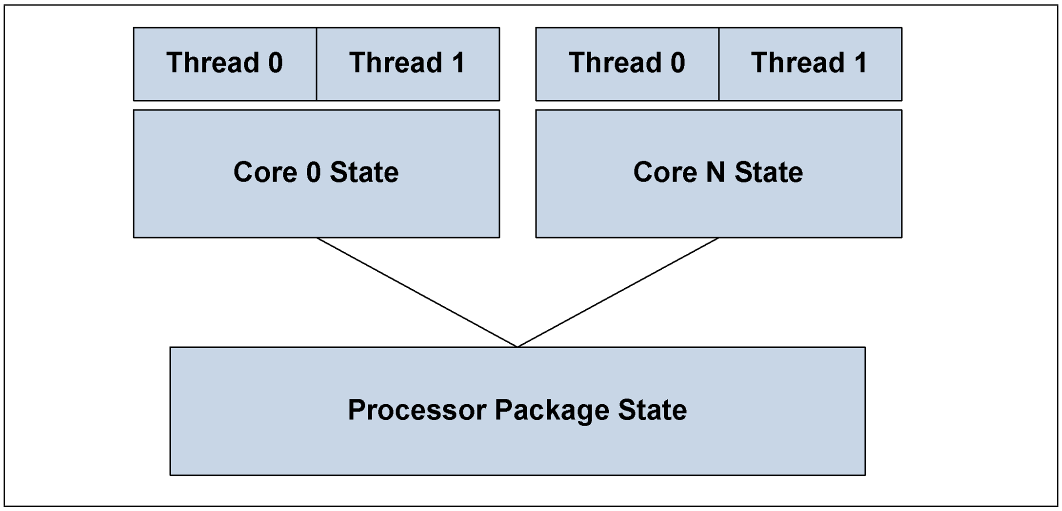
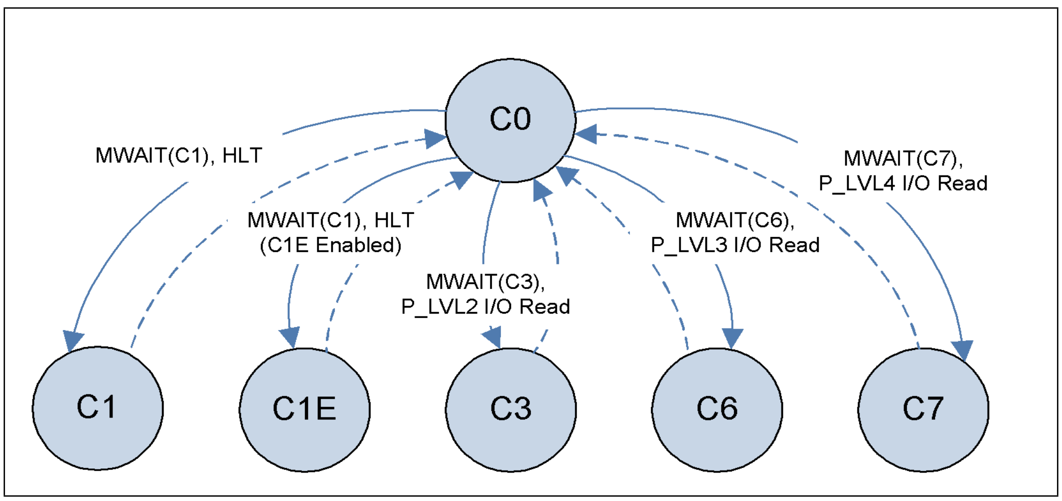


Figure 4-2. Thread and Core C-State Entry and Exit



While individual threads can request low power C-states, power saving actions only take place once the core C-state is resolved. Core C-states are automatically resolved by the processor. For thread and core C-states, a transition to and from C0 is required before entering any other C-state.

4.2.3 Requesting Low-Power Idle States

If enabled, the core C-state will be C1E if all actives cores have also resolved a core C1 state or higher.

The primary software interfaces for requesting low power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions using I/O reads.

For legacy operating systems, P_LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, must be enabled in the BIOS.

Note: The P_LVLx I/O Monitor address needs to be set up before using the P_LVLx I/O read interface. Each P-LVLx is mapped to the supported MWAIT(Cx) instruction as shown in Table 4-7.

Table 4-7. P_LVLx to MWAIT Conversion

P_LVLx	MWAIT(Cx)	Notes
P_LVL2	MWAIT(C3)	
P_LVL3	MWAIT(C6)	C6. No sub-states allowed.
P_LVL4	MWAIT(C7)	C7. No sub-states allowed.

The BIOS can write to the C-state range field of the PMG_IO_CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P_LVLx reads outside of this range do not cause an I/O redirection to MWAIT(Cx) like request. They fall through like a normal I/O instruction.

Note: When P_LVLx I/O instructions are used, MWAIT substates cannot be defined. The MWAIT substate is always zero if I/O MWAIT redirection is used. By default, P_LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF' feature that triggers a wakeup on an interrupt, even if interrupts are masked by EFLAGS.IF.

4.2.4 Core C-states

The following are general rules for all core C-states, unless specified otherwise:

- A core C-State is determined by the lowest numerical thread state (such as, Thread 0 requests C1E while Thread 1 requests C3, resulting in a core C1E state). See Table 4-6.
- A core transitions to C0 state when:
  - — an interrupt occurs.
  - — there is an access to the monitored address if the state was entered using an MWAIT instruction.
- For core C1/C1E, and core C3, an interrupt directed toward a single thread wakes only that thread. However, since both threads are no longer at the same core C-state, the core resolves to C0.
- An interrupt only wakes the target thread for both C3 and C6 states. Any interrupt coming into the processor package may wake any core.

4.2.4.1 Core C0 State

The normal operating state of a core where code is being executed.

4.2.4.2 Core C1/C1E State

C1/C1E is a low power state entered when all threads within a core execute a HLT or MWAIT(C1/C1E) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. See the *Intel® 64 and IA-32 Architecture Software Developer's Manual, Volume 3A/3B: System Programmer's Guide* for more information.

While a core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, see Section 4.2.5.2, "Package C1/C1E".

4.2.4.3 Core C3 State

Individual threads of a core can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. A core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared L3 cache, while maintaining its architectural state. All core clocks are stopped at this point. Because the core's caches are flushed, the processor does not wake any core that is in the C3 state when either a snoop is detected or when another core accesses cacheable memory.

4.2.4.4 Core C6 State

Individual threads of a core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6, the core will save its architectural state to a dedicated SRAM. Once complete, a core will have its voltage reduced to zero volts. During exit, the core is powered on and its architectural state is restored. In addition to flushing core caches core architecture state is saved to the uncore. Once the core state save is completed, core voltage is reduced to zero.

4.2.4.5 Core C7 State

Individual threads of a core can enter the C7 state by initiating a P_LVL4 I/O read to the P_BLK or by an MWAIT(C7) instruction. Core C7 and core C7 substate are the same as Core C6. The processor does not support LLC flush under any condition.

4.2.4.6 C-State Auto-Demotion

In general, deeper C-states such as C6 or C7 have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. To increase residency in deeper C-states, the processor supports C-state auto-demotion.

There are two C-State auto-demotion options:

- C6/C7 to C3
- C7/C6/C3 To C1

The decision to demote a core from C6/C7 to C3 or C3/C6/C7 to C1 is based on each core's immediate residency history. Upon each core C6/C7 request, the core C-state is demoted to C3 or C1 until a sufficient amount of residency has been established. At that point, a core is allowed to go into C3/C6 or C7. Each option can be run concurrently or individually.

This feature is disabled by default. BIOS must enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.

4.2.5 Package C-States

The processor supports C0, C1/C1E, C2, C3, and C6 power states. The following is a summary of the general rules for package C-state entry. These apply to all package C-states unless specified otherwise:

- A package C-state request is determined by the lowest numerical core C-state amongst all cores.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
  - Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
  - The platform may allow additional power savings to be realized in the processor.
- For package C-states, the processor is not required to enter C0 before entering any other C-state.

The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a core break event is received, the target core is activated and the break event message is forwarded to the target core.
  - If the break event is not masked, the target core enters the core C0 state and the processor enters package C0.
  - If the break event is masked, the processor attempts to re-enter its previous package state.
- If the break event was due to a memory access or snoop request.
  - But the platform did not request to keep the processor in a higher package C-state, the package returns to its previous C-state.
  - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

The package C-states fall into two categories – uncoordinated and coordinated. C0/C1/C1E are uncoordinated, while C2/C3/C6 are coordinated.

Starting with the 2nd Generation Intel® Core™ Processor Family Desktop, package C-states are based on exit latency requirements which are accumulated from the PCIe* devices, PCH, and software sources. The level of power savings that can be achieved is a function of the exit latency requirement from the platform. As a result, there is no fixed relationship between the coordinated C-state of a package, and the power savings that will be obtained from the state. Coordinated package C-states offer a range of power savings which is a function of the ensured exit latency requirement from the platform.

There is also a concept of Execution Allowed (EA) – when EA status is 0, the cores in a socket are in C3 or a deeper state, a socket initiates a request to enter a coordinated package C-state. The coordination is across all sockets and the PCH.

Table 4-8 shows an example of a dual-core processor package C-state resolution. Figure 4-3 summarizes package C-state transitions with package C2 as the interim between PC0 and PC1 prior to PC3 and PC6.

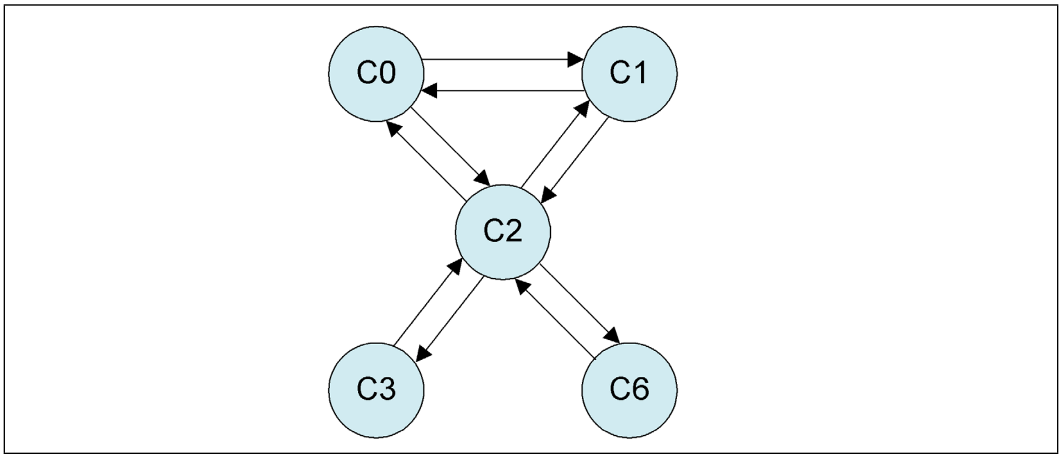
Table 4-8. Coordination of Core Power States at the Package Level

Package C-State		Core 1 C0	Core 1 C1	Core 1 C3	Core 1 C6
Core 0	C0	C0	C0	C0	C0
Core 0	C1	C0	C1[1]	C1[1]	C1[1]
Core 0	C3	C0	C1[1]	C3	C3
Core 0	C6	C0	C1[1]	C3	C6

Notes:

1. If enabled, the package C-state will be C1E if all actives cores have resolved a core C1 state or higher.

Figure 4-3. Package C-State Entry and Exit



4.2.5.1 Package C0

The normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low power state. Individual cores may be in lower power idle states while the package is in C0.

4.2.5.2 Package C1/C1E

No additional power reduction actions are taken in the package C1 state. However, if the C1E sub-state is enabled, the processor automatically transitions to the lowest supported core clock frequency, followed by a reduction in voltage. Autonomous power reduction actions that are based on idle timers can trigger depending on the activity in the system.

The package enters the C1 low power state when:

- At least one core is in the C1 state
- The other cores are in a C1 or lower power state

The package enters the C1E state when:

- All cores have directly requested C1E using MWAIT(C1) with a C1E sub-state hint
- All cores are in a power state lower that C1/C1E but the package low power state is limited to C1/C1E using the PMG_CST_CONFIG_CONTROL MSR
- All cores have requested C1 using HLT or MWAIT(C1) and C1E auto-promotion is enabled in IA32_MISC_ENABLES

No notification to the system occurs upon entry to C1/C1E.

4.2.5.3 Package C2 State

The Package C2 state is an intermediate state that represents the point at which the system level coordination is in progress. The package cannot reach this state unless all cores are in at least C3.

The package will remain in C2 when:

- it is awaiting for a coordinated response
- the coordinated exit latency requirements are too stringent for the package to take any power saving actions

If the exit latency requirements are high enough, the package will transition to C3 or C6 depending on the state of the cores.

4.2.5.4 Package C3 State

A processor enters the package C3 low power state when:

- At least one core is in the C3 state
- The other cores are in a C3 or lower power state, and the processor has been granted permission by the platform
- L3 shared cache retains context and becomes inaccessible in this state
- Additional power savings actions, as allowed by the exit latency requirements, include putting PCIe* links in L1, the uncore is not available, further voltage reduction can be taken
- In package C3, the ring will be off and as a result no accesses to the LLC are possible. The content of the LLC is preserved

4.2.5.5 Package C6 State

A processor enters the package C6 low power state when:

- At least one core is in the C6 state
- The other cores are in a C6 or lower power state, and the processor has been granted permission by the platform
- L3 shared cache retains context and becomes inaccessible in this state
- Additional power savings actions, as allowed by the exit latency requirements, include putting PCIe* links in L1, the uncore is not available, further voltage reduction can be taken

In package C6 state, all cores have saved their architectural state and have had their core voltages reduced to zero volts. The LLC retains context, but no accesses can be made to the LLC in this state, the cores must break out to the internal state package C2 for snoops to occur.

4.2.6 Package C-State Power Specifications

Table 4-9 lists the processor package C-state power specifications for various processor SKUs.

The C-state power specification is based on post-silicon validation results. The processor case temperature is assumed at 50 °C for all C-states.

Table 4-9. Package C-State Power Specifications

TDP SKUs	C1E (W)	C3 (W)	C6 (W)
6-Core			
Intel® Core™ 3970X processor Extreme Edition 150 W (6-core)	58	27	15
Intel® Core™ 3960X processor Extreme Edition 130 W (6-core)	53	35	21
Intel® Core™ 3930K processor Extreme Edition 130 W (6-core)	53	25	21
4-Core			
Intel® Core™ 3820K processor Extreme Edition 130 W (4-core)	53	28	16

4.3 System Memory Power Management

The DDR3 power states can be summarized as the following:

- Normal operation (highest power consumption)
- CKE Power-Down: Opportunistic, per rank control after idle time. There may be different levels.
  - Active Power-Down
  - Precharge Power-Down with Fast Exit
  - Precharge power Down with Slow Exit
- Self Refresh: In this mode no transaction is executed. The DDR consumes the minimum possible power.

4.3.1 CKE Power-Down

The CKE input land is used to enter and exit different power-down modes. The memory controller has a configurable activity timeout for each rank. When no reads are present to a given rank for the configured interval, the memory controller will transition the rank to power-down mode.

The memory controller transitions the DRAM to power-down by de-asserting CKE and driving a NOP command. The memory controller will tri-state all DDR interface lands except CKE (de-asserted) and ODT while in power-down. The memory controller will transition the DRAM out of power-down state by synchronously asserting CKE and driving a NOP command.

When CKE is off, the internal DDR clock is disabled and the DDR power is significantly reduced.

The DDR defines three levels of power-down:

- Active power-down: This mode is entered if there are open pages when CKE is de-asserted. In this mode the open pages are retained. Existing this mode is 3–5 DCLK cycles.
- Precharge power-down fast exit: This mode is entered if all banks in DDR are precharged when de-asserting CKE. Existing this mode is 3–5 DCLK cycles. The difference from the active power-down mode is that when waking up, all page-buffers are empty.
- Precharge power-down slow exit: In this mode the data-in DLLs on DDR are off. Existing this mode is 3–5 DCLK cycles until the first command is allowed, but about 16 cycles until first data is allowed.

4.3.2 Self Refresh

The Uncore Power Manager (PCU) may request the memory controller to place the DRAMs in self refresh state. Self refresh per channel is supported. The BIOS can put the channel in self refresh if software remaps memory to use a subset of all channels. Also processor channels can enter self refresh autonomously without PCU instruction when the package is in a package C0 state.

4.3.2.1 Self Refresh Entry

Self refresh entrance can be either disabled or triggered by an idle counter. Idle counter always clears with any access to the memory controller and remains clear as long as the memory controller is not drained. As soon as the memory controller is drained, the counter starts counting, and when it reaches the idle-count, the memory controller will place the DRAMs in self refresh state.

Power may be removed from the memory controller core at this point, but the V_{CCD} supply (1.5 V) to the DDR I/O must be maintained.

4.3.2.2 Self Refresh Exit

Self refresh exit can be either a message from an external unit (PCU in most cases, but also possibly from any message-channel master) or as reaction for an incoming transaction.

The proper actions on self refresh exit are:

- CK is enabled, and four CK cycles driven
- When proper skew between Address/Command and CK are established, assert CKE
- Issue NOPs for tXSRD cycles
- Issue ZQCL to each rank
- The global scheduler will be enabled to issue commands

4.3.2.3 DLL and PLL Shutdown

Self refresh, according to configuration, may be a trigger for master DLL shut-down and PLL shut-down. The master DLL shut-down is issued by the memory controller after the DRAMs have entered self refresh.

The PLL shut-down and wake-up is issued by the PCU. The memory controller gets a signal from PLL indicating that the memory controller can start working again.

4.3.3 DRAM I/O Power Management

Unused signals are tristated to save power. This includes all signals associated with an unused memory channel.

The I/O buffer for an unused signal should be tristated (output driver disabled), the input receiver (differential sense-amp) should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

4.4 DMI2 / PCI Express* Power Management

Active State Power Management (ASPM) support using the L1 state.

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5 Thermal Management Specifications

For thermal specifications and design guidelines, refer to the processor Thermal Mechanical Specification and Design Guide (see Section 1.7, "Related Documents").

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6 Signal Descriptions

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category.

6.1 System Memory Interface

Table 6-1. Memory Channel DDR0, DDR1, DDR2, DDR3

Signal Name	Description
DDR{0/1/2/3}_BA[2:0]	Bank Address. Defines the bank which is the destination for the current Activate, Read, Write, or Precharge command.
DDR{0/1/2/3}_CAS_N	Column Address Strobe.
DDR{0/1/2/3}_CKE[3:0]	Clock Enable.
DDR{0/1/2/3}_CLK_DN[3:0] DDR{0/1/2/3}_CLK_DP[3:0]	Differential clocks to the DIMM. All command and control signals are valid on the rising edge of clock.
DDR{0/1/2/3}_CS_N[1:0] DDR{0/1/2/3}_CS_N[5:4]	Chip Select. Each signal selects one rank as the target of the command and address.
DDR{0/1/2/3}_DQ[63:00]	Data Bus. DDR3 Data bits.
DDR{0/1/2/3}_DQS_DP[08:00] DDR{0/1/2/3}_DQS_DN[08:00]	Data strobes. Differential pair, Data Strobe. Differential strobes latch data for each DRAM. Driven with edges in center of data, receive edges are aligned with data edges.
DDR{0/1/2/3}_ECC[7:0]	Check bits. An error correction code is driven along with data on these lines for DIMMs that support that capability. **Note:** ECC DIMMs are not supported on the processor; thus, these signals are not used.
DDR{0/1/2/3}_MA[15:00]	Memory Address. Selects the Row address for Reads and writes, and the column address for activates. Also used to set values for DRAM configuration registers.
DDR{0/1/2/3}_ODT[3:0]	On Die Termination. Enables DRAM on die termination during Data Write or Data Read transactions.
DDR{0/1/2/3}_RAS_N	Row Address Strobe.
DDR{0/1/2/3}_WE_N	Write Enable.

Table 6-2. Memory Channel Miscellaneous

Signal Name	Description
DDR_RESET_C01_N DDR_RESET_C23_N	System memory reset: Reset signal from processor to DRAM devices on the DIMMs. DDR_RESET_C01_N is used for memory channels 0 and 1 while DDR_RESET_C23_N is used for memory channels 2 and 3.
DDR_SCL_C01 DDR_SCL_C23	SMBus clock for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs. DDR_SCL_C01 is used for memory channels 0 and 1 while DDR_SCL_C23 is used for memory channels 2 and 3.
DDR_SDA_C01 DDR_SDA_C23	SMBus data for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs. DDR_SDA_C1 is used for memory channels 0 and 1 while DDR_SDA_C23 is used for memory channels 2 and 3.
DDR_VREFDQRX_C01 DDR_VREFDQRX_C23	Voltage reference for system memory reads. DDR_VREFDQRX_C01 is used for memory channels 0 and 1 while DDR_VREFDQRX_C23 is used for memory channels 2 and 3.
DDR_VREFDQTX_C01 DDR_VREFDQTX_C23	Voltage reference for system memory writes. DDR_VREFDQTX_C01 is used for memory channels 0 and 1 while DDR_VREFDQTX_C23 is used for memory channels 2 and 3. ***Note:*** Future implementation option, not included in first silicon.
DDR{01/23}_RCOMP[2:0]	System memory impedance compensation. Impedance compensation must be terminated on the system board using a precision resistor.
DRAM_PWR_OK_C01 DRAM_PWR_OK_C23	Power good input signal used to indicate that the VCCD power supply is stable for memory channels 0 & 1 and channels 2 & 3.

6.2 PCI Express* Based Interface Signals

Note: PCI Express* Ports 1, 2, and 3 Signals are receive and transmit differential pairs.

Table 6-3. PCI Express* Port 1 Signals

Signal Name	Description
PE1A_RX_DN[3:0] PE1A_RX_DP[3:0]	PCIe Receive Data Input
PE1B_RX_DN[7:4] PE1B_RX_DP[7:4]	PCIe Receive Data Input
PE1A_TX_DN[3:0] PE1A_TX_DP[3:0]	PCIe Transmit Data Output
PE1B_TX_DN[7:4] PE1B_TX_DP[7:4]	PCIe Transmit Data Output

Table 6-4. PCI Express* Port 2 Signals

Signal Name	Description
PE2A_RX_DN[3:0] PE2A_RX_DP[3:0]	PCIe Receive Data Input
PE2B_RX_DN[7:4] PE2B_RX_DP[7:4]	PCIe Receive Data Input
PE2C_RX_DN[11:8] PE2C_RX_DP[11:8]	PCIe Receive Data Input
PE2D_RX_DN[15:12] PE2D_RX_DP[15:12]	PCIe Receive Data Input
PE2A_TX_DN[3:0] PE2A_TX_DP[3:0]	PCIe Transmit Data Output
PE2B_TX_DN[7:4] PE2B_TX_DP[7:4]	PCIe Transmit Data Output
PE2C_TX_DN[11:8] PE2C_TX_DP[11:8]	PCIe Transmit Data Output
PE2D_TX_DN[15:12] PE2D_TX_DP[15:12]	PCIe Transmit Data Output

Table 6-5. PCI Express* Port 3 Signals

Signal Name	Description
PE3A_RX_DN[3:0] PE3A_RX_DP[3:0]	PCIe Receive Data Input
PE3B_RX_DN[7:4] PE3B_RX_DP[7:4]	PCIe Receive Data Input
PE3C_RX_DN[11:8] PE3C_RX_DP[11:8]	PCIe Receive Data Input
PE3D_RX_DN[15:12] PE3D_RX_DP[15:12]	PCIe Receive Data Input
PE3A_TX_DN[3:0] PE3A_TX_DP[3:0]	PCIe Transmit Data Output
PE3B_TX_DN[7:4] PE3B_TX_DP[7:4]	PCIe Transmit Data Output
PE3C_TX_DN[11:8] PE3C_TX_DP[11:8]	PCIe Transmit Data Output
PE3D_TX_DN[15:12] PE3D_TX_DP[15:12]	PCIe Transmit Data Output

Table 6-6. PCI Express* Miscellaneous Signals

Signal Name	Description
PE_RBIAS	This input is used to control PCI Express* bias currents. A 50 ohm 1% tolerance resistor must be connected from this land to V_{SS} by the platform. PE_RBIAS is required to be connected as if the link is being used even when PCIe* is not used.
PE_RBIAS_SENSE	Provides dedicated bias resistor sensing to minimize the voltage drop caused by packaging and platform effects. PE_RBIAS_SENSE is required to be connected as if the link is being used even when PCIe* is not used.
PE_VREF_CAP	PCI Express* voltage reference used to measure the actual output voltage and comparing it to the assumed voltage. A 0.01 uF capacitor must be connected from this land to V_{SS}.

6.3 DMI2 / PCI Express* Port 0 Signals

Table 6-7. DMI2 to Port 0 Signals

Signal Name	Description
DMI_RX_DN[3:0] DMI_RX_DP[3:0]	DMI2 Receive Data Input
DMI_TX_DP[3:0] DMI_TX_DN[3:0]	DMI2 Transmit Data Output

6.4 Platform Environment Control Interface (PECI) Signal

Table 6-8. PECI Signals

Signal Name	Description
PECI	PECI (Platform Environment Control Interface) is the serial sideband interface to the processor and is used primarily for thermal, power and error management.

6.5 System Reference Clock Signals

Table 6-9. System Reference Clock (BCLK{0/1}) Signals

Signal Name	Description
BCLK{0/1}_D[N/P]	Reference Clock Differential input. These pins provide the PLL reference clock differential input into the processor.

6.6 JTAG and TAP Signals

Table 6-10. JTAG and TAP Signals

Signal Name	Description
BPM_N[7:0]	Breakpoint and Performance Monitor Signals: I/O signals from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. These are 100 MHz signals.
EAR_N	External Alignment of Reset, used to bring the processor up into a deterministic state. This signal is pulled up on the die; refer to Table 7-6 for details.
PRDY_N	Probe Mode Ready is a processor output used by debug tools to determine processor debug readiness.
PREQ_N	Probe Mode Request is used by debug tools to request debug operation of the processor.
TCK	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TMS	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRST_N	TRST_N (Test Reset) resets the Test Access Port (TAP) logic. TRST_N must be driven low during power on Reset.

6.7 Serial VID Interface (SVID) Signals

Table 6-11. SVID Signals

Signal Name	Description
SVIDALERT_N	Serial VID alert.
SVIDCLK	Serial VID clock.
SVIDDATA	Serial VID data out.

6.8 Processor Asynchronous Sideband and Miscellaneous Signals

Table 6-12. Processor Asynchronous Sideband Signals (Sheet 1 of 2)

Signal Name	Description
BIST_ENABLE	Input which allows the platform to enable or disable built-in self test (BIST) on the processor. This signal is pulled up on the die; refer to Table 7-6 for details.
CAT_ERR_N	Indicates that the system has experienced a fatal or catastrophic error and cannot continue to operate. The processor will assert CAT_ERR_N for nonrecoverable machine check errors and other internal unrecoverable errors. It is expected that every processor in the system will wire-OR CAT_ERR_N for all processors. Since this is an I/O land, external agents are allowed to assert this land, which will cause the processor to take a machine check exception. This signal is sampled after PWRGOOD assertion. On the processor, CAT_ERR_N is used for signaling the following types of errors: • Legacy MCERR's, CAT_ERR_N is asserted for 16 BCLKs. • Legacy IERR's, CAT_ERR_N remains asserted until warm or cold reset.
CPU_ONLY_RESET	Resets all the processors on the platform without resetting the DMI2 links.
ERROR_N[2:0]	Error status signals for integrated I/O (IIO) unit: 0 = Hardware correctable error (no operating system or firmware action necessary) 1 = Non-fatal error (operating system or firmware action required to contain and recover) 2 = Fatal error (system reset likely required to recover)
MEM_HOT_C01_N MEM_HOT_C23_N	Memory throttle control. MEM_HOT_C01_N and MEM_HOT_C23_N signals have two modes of operation – input and output mode. Input mode is externally asserted and is used to detect external events such as VR_HOT# from the memory voltage regulator and causes the processor to throttle the appropriate memory channels. Output mode is asserted by the processor known as level mode. In level mode, the output indicates that a particular branch of memory subsystem is hot. MEM_HOT_C01_N is used for memory channels 0 & 1 while MEM_HOT_C23_N is used for memory channels 2 & 3.
PMSYNC	Power Management Sync. A sideband signal to communicate power management status from the Platform Controller Hub (PCH) to the processor.
PROCHOT_N	PROCHOT_N will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal can also be driven to the processor to activate the Thermal Control Circuit. This signal is sampled after PWRGOOD assertion. If PROCHOT_N is asserted at the deassertion of RESET_N, the processor will tristate its outputs.
PWRGOOD	Power Good is a processor input. The processor requires this signal to be a clean indication that BCLK, V_{TTA}/V_{TTD}, V_{SA}, V_{CCPLL}, V_{CCD_01} and V_{CCD_23} supplies are stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. PWRGOOD transitions from inactive to active when all supplies except V_{CC} are stable. V_{CC} has a VBOOT of zero volts and is not included in PWRGOOD indication in this phase. However, for the active to inactive transition, if any processor power supply (V_{CC}, V_{TTA}/V_{TTD}, V_{SA}, V_{CCD}, or V_{CCPLL}) is about to fail or is out of regulation, the PWRGOOD is to be negated. The signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. **Note:** V_{CC} has a Vboot setting of 0.0 V and is not included in the PWRGOOD indication and V_{SA} has a Vboot setting of 0.9 V.

Table 6-12. Processor Asynchronous Sideband Signals (Sheet 2 of 2)

Signal Name	Description
RESET_N	Asserting the RESET_N signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. Some PLL and error states are not effected by reset and only PWRGOOD forces them to a known state.
TEST[4:0]	Test[4:0] must be individually connected to an appropriate power source or ground through a resistor for proper processor operation.
THERMTRIP_N	Assertion of THERMTRIP_N (Thermal Trip) indicates one of two possible critical over-temperature conditions: One, the processor junction temperature has reached a level beyond which permanent silicon damage may occur and Two, the system memory interface has exceeded a critical temperature limit set by BIOS. Measurement of the processor junction temperature is accomplished through multiple internal thermal sensors that are monitored by the Digital Thermal Sensor (DTS). Simultaneously, the Power Control Unit (PCU) monitors external memory temperatures using the dedicated SMBus interface to the DIMMs. If any of the DIMMs exceed the BIOS defined limits, the PCU will signal THERMTRIP_N to prevent damage to the DIMMs. Once activated, the processor will stop all execution and shut down all PLLs. To further protect the processor, its core voltage (V_{CC}), V_{TTA}, V_{TTD}, V_{SA}, V_{CCPLL}, V_{CCD} supplies must be removed following the assertion of THERMTRIP_N. Once activated, THERMTRIP_N remains latched until RESET_N is asserted. While the assertion of the RESET_N signal may de-assert THERMTRIP_N, if the processor's junction temperature remains at or above the trip level, THERMTRIP_N will again be asserted after RESET_N is de-asserted. This signal can also be asserted if the system memory interface has exceeded a critical temperature limit set by BIOS. This signal is sampled after PWRGOOD assertion.

Table 6-13. Miscellaneous Signals

Signal Name	Description
BCLK_SELECT[1:0]	These configuration straps are used to inform the processor that a non-standard value for BCLK is going to is been applied at reset. A "11" encoding on these inputs will inform the processor to run at DEFAULT BCLK = 100 MHz. These signals have internal pull-up to V_{TT}. The encoding is as follows: **BCLK_SELECT1 — BCLK_SELECT0 — BCLK Selected** X — X — 100 MHz (default) 1 — 1 — 100 MHz 1 — 0 — 125 MHz 0 — 1 — Reserved 0 — 0 — Reserved
CORE_VREF_CAP	A capacitor must be connected from this land.
CORE_RBIAS	This input is used to control bias currents.
CORE_RBIAS_SENSE	Provides dedicated bias resistor sensing to minimize the voltage drop caused by packaging and platform effects.
PROC_SEL_N	This output can be used by the platform to determine if the installed processor is a Intel® Core™ i7 processor family for the LGA-2011 socket or a future processor planned for the platforms. There is no connection to the processor silicon for this signal. This signal is also used by the V_{CCPLL} and V_{TT} rails to switch their output voltage to support future processors.
RSVD	RESERVED. All signals that are RSVD must be left unconnected on the board. Refer to Section 7.1.9 for details.
SKTOCC_N	SKTOCC_N (Socket occupied) is used to indicate that a processor is present. This is pulled to ground on the processor package; there is no connection to the processor silicon for this signal.
TESTHI_BH48 TESTHI_BF48 TESTHI_AT50	TESTHI_XX signal must be pulled up on the board.

6.9 Processor Power and Ground Supplies

Table 6-14. Power and Ground Signals

Signal Name	Description
VCC	Variable power supply for the processor cores, lowest level caches (LLC), ring interface, and home agent. It is provided by a VR12 compliant regulator. The output voltage of this supply is selected by the processor using the serial voltage ID (SVID) bus. **Note:** VCC has a Vboot setting of 0.0 V and is not included in the PWRGOOD indication.
VCC_SENSE VSS_VCC_SENSE	VCC_SENSE and VSS_VCC_SENSE provide an isolated, low impedance connection to the processor core power and ground. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage (that is, processor voltage) remains within specification.
VSA_SENSE VSS_VSA_SENSE	VSA_SENSE and VSS_VSA_SENSE provide an isolated, low impedance connection to the processor system agent (VSA) power plane. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage (that is, processor voltage) remains within specification.
VTTD_SENSE VSS_VTTD_SENSE	VTTD_SENSE and VSS_VTTD_SENSE provide an isolated, low impedance connection to the processor I/O power plane. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage (that is, processor voltage) remains within specification.
VCCD_01 and VCCD_23	Power supply for the processor system memory interface. Provided by two VR12 compliant regulators or two non-VR12 voltage regulators (simple switching VRs for example). VCCD_01 and VCCD_23 are used for memory channels 0, 1 & 2, 3 respectively. VCCD_01 and VCCD_23 will also be referred to as VCCD. VCCD is generic for VCCD_01, VCCD_23. ***Note:*** The processor must be provided VCCD_01 and VCCD_23 for proper operation, even in configurations where no memory is populated. A VR12.0 controller is recommended, but not required.
VCCPLL	Fixed power supply (1.8 V) for the processor phased lock loop (PLL).
VSA	Variable power supply for the processor system agent units. These include logic (non-I/O) for the integrated I/O controller, the integrated memory controller (iMC), and the Power Control Unit (PCU). The output voltage of this supply is selected by the processor, using the serial voltage ID (SVID) bus. **Note:** VSA has a Vboot setting of 0.9 V.
VSS	Processor ground node.
VTTA VTTD	Combined fixed analog and digital power supply for I/O sections of Direct Media Interface Gen 2 (DMI2) interface and PCI Express* interface. Will also be referred to as VTT.

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7 Electrical Specifications

7.1 Processor Signaling

The processor includes 2011 lands that use various signaling technologies. Signals are grouped by electrical characteristics and buffer type into various signal groups. These include DDR3 (Reference Clock, Command, Control, and Data), PCI Express*, DMI2, Platform Environmental Control Interface (PECI), System Reference Clock, SMBus, JTAG and Test Access Port (TAP), SVID Interface, Processor Asynchronous Sideband, Miscellaneous, and Power/Other signals. Refer to Table 7-5 for details.

Intel strongly recommends performing analog simulations of all interfaces. Refer to Section 1.7, "Related Documents" for signal integrity model availability.

7.1.1 System Memory Interface Signal Groups

The system memory interface uses DDR3 technology that consists of numerous signal groups. These groups include – Reference Clocks, Command Signals, Control Signals, and Data Signals. Each group consists of numerous signals that may use various signaling technologies. Refer to Table 7-5 for further details. Throughout this chapter, the system memory interface maybe referred to as DDR3.

7.1.2 PCI Express* Signals

The PCI Express Signal Group consists of PCI Express* ports 1, 2, and 3, and PCI Express miscellaneous signals. Refer to Table 7-5 for further details.

Note: The processor is capable of up to 8.0 GT/s speeds.

7.1.3 DMI2/PCI Express* Signals

The Direct Media Interface (DMI2) Gen 2 sends and receives packets and/or commands to the PCH. The DMI2 is an extension of the standard PCI Express Specification. The DMI2/PCI Express Signals consist of DMI2 receive and transmit input/output signals and a control signal. Refer to Table 7-5 for further details.

7.1.4 Platform Environmental Control Interface (PECI)

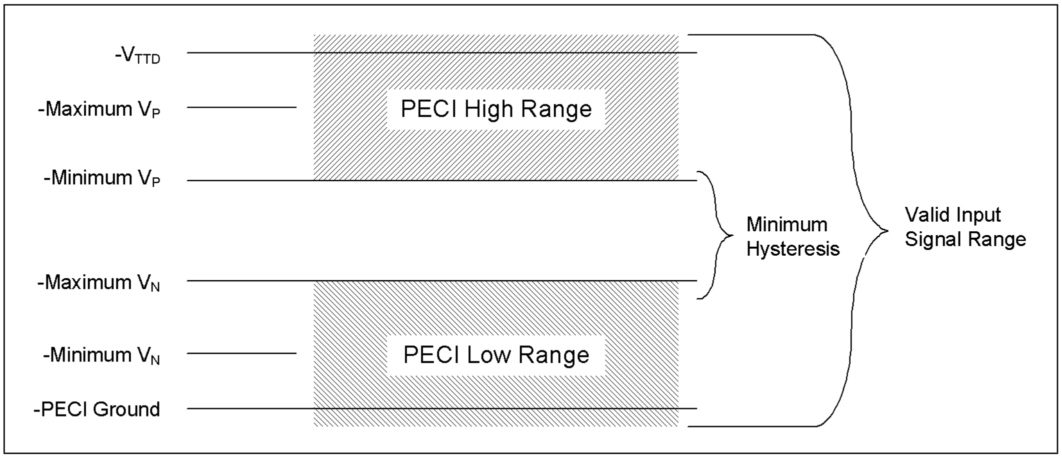
PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external system management logic and thermal monitoring devices. The processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read processor temperature, perform processor manageability functions, and manage processor interface tuning and diagnostics. Refer to Section 2.4, "Platform Environment Control Interface (PECI)" for processor specific implementation details for PECI. Refer to the processor Thermal Mechanical Specification and Design Guide (see Section 1.7, "Related Documents") for additional details regarding PECI and for a list of supported PECI commands.

The PECI interface operates at a nominal voltage set by V_{TTD}. The set of DC electrical specifications shown in Table 7-13 is used with devices normally operating from a V_{TTD} interface supply.

7.1.4.1 Input Device Hysteresis

The PECI client and host input buffers must use a Schmitt-triggered input design for improved noise immunity. Refer to Figure 7-1 and Table 7-13.

Figure 7-1. Input Device Hysteresis



7.1.5 System Reference Clocks (BCLK{0/1}_DP, BCLK{0/1}_DN)

The processor core, processor uncore, PCI Express*, and DDR3 memory interface frequencies are generated from BCLK{0/1}_DP and BCLK{0/1}_DN signals. The processor maximum core frequency and DDR memory frequency are set during manufacturing. It is possible to override the processor core frequency setting using software. This permits operation at lower core frequencies than the factory set maximum core frequency.

The processor core frequency is configured during reset by using values stored within the device during manufacturing. The stored value sets the lowest core multiplier at which the particular processor can operate. If higher speeds are desired, the appropriate ratio can be configured using the IA32_PERF_CTL MSR (MSR 199h); Bits 15:0.

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK{0/1}_DP, BCLK{0/1}_DN input, with exceptions for spread spectrum clocking. DC specifications for the BCLK{0/1}_DP, BCLK{0/1}_DN inputs are provided in Table 7-14.

7.1.5.1 PLL Power Supply

An on-die PLL filter solution is implemented on the processor. Refer to Table 7-9 and Table 7-10 for DC specifications.

7.1.6 JTAG and Test Access Port (TAP) Signals

Due to the voltage levels supported by other components in the JTAG and Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

7.1.7 Processor Sideband Signals

The processor includes asynchronous sideband signals that provide asynchronous input, output or I/O signals between the processor and the platform or Platform Controller Hub. Details can be found in Table 7-5.

All processor Asynchronous Sideband signals are required to be asserted/deasserted for a defined number of BCLKs in order for the processor to recognize the proper signal state. These are outlined in Table 7-18 (DC specifications).

7.1.8 Power, Ground and Sense Signals

Processors also include various other signals including power/ground and sense points. Details can be found in Table 7-5.

7.1.8.1 Power and Ground Lands

All VCC, VCCPLL, VSA, VCCD, VTTA, and VTTD lands must be connected to their respective processor power planes, while all VSS lands must be connected to the system ground plane.

For clean on-chip power distribution, processors include lands for all required voltage supplies. These are listed in Table 7-1.

Table 7-1. Power and Ground Lands

Power and Ground Lands	Comments
VCC	Each VCC land must be supplied with the voltage determined by the SVID Bus signals. Table 7-3 defines the voltage level associated with each core SVID pattern. **Note:** V_{CC} has a VBOOT setting of 0.0 V.
VCCPLL	Each VCCPLL land is connected to a 1.80 V supply, power the Phase Lock Loop (PLL) clock generation circuitry. An on-die PLL filter solution is implemented within the processor.
VCCD_01 VCCD_23	Each VCCD land is connected to a 1.50 V supply to provide power to the processor DDR3 interface. These supplies also power the DDR3 memory subsystem. V_{CCD} may be controlled by the SVID Bus using a VR12 controller and or a non-VR12 regulator may be used. VCCD is the generic term for VCCD_01, VCCD_23.
VTTA	VTTA lands must be supplied by a fixed 1.05 V supply.
VTTD	VTTD lands must be supplied by a fixed 1.05 V supply.
VSA	Each VSA land must be supplied with the voltage determined by the SVID Bus signals, typically set at 0.85 V. VSA has a VBOOT setting of 0.9 V.
VSS	Ground

7.1.8.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Large electrolytic bulk capacitors (C_{BULK}), help maintain the output voltage during current transients; for example, coming out of an idle condition. Care must be taken in the baseboard design to ensure that the voltages provided to the processor remains within the specifications listed in Table 7-9. Failure to do so can result in timing violations or reduced lifetime of the processor.

7.1.8.3 Voltage Identification (VID)

The Voltage Identification (VID) specification for the $V_{CC,}$ V_{SA}, and optionally the V_{CCD} voltage are defined by the *VR12/IMVP7 Pulse Width Modulation (PWM) Specification*. The reference voltage or the VID setting is set using the SVID communication bus between the processor and the voltage regulator controller chip. The VID setting is the nominal voltage to be delivered to the processor VCC, VSA, and the VCCD lands. Table 7-3 specifies the reference voltage level corresponding to the VID value transmitted over serial VID. The VID codes will change due to temperature and/or current load changes to minimize the power and to maximize the performance of the part. The specifications are set so that a voltage regulator can operate with all supported frequencies.

Individual processor VID values may be calibrated during manufacturing such that two processor units with the same core frequency may have different default VID settings.

The processor uses voltage identification signals to support automatic selection of $V_{CC,}$ V_{SA}, and if desired the V_{CCD} power supply voltages. If the processor socket is empty (SKTOCC_N high), or a “not supported” response is received from the SVID bus, then the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself or not power on. Vout MAX register (30h) is programmed by the processor to set the maximum supported VID code and if the programmed VID code is higher than the VID supported by the VR, then VR will respond with a “not supported” acknowledgement.

7.1.8.3.1 SVID Commands

The processor provides the ability to operate while transitioning to a new VID and its associated processor core voltage. This is represented by a DC shift in the loadline. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target voltage. Transitions above the maximum specified VID are not supported. The processor supports the following VR commands:

- SetVID_fast (20 mV/μs for V_{CC}, 10m V/μs for $V_{CC}/V_{SA}/V_{CCD}$),
- SetVID_slow (5m V/μs for V_{CC}, 2.5 mV/μs for $V_{CC}/V_{SA}/V_{CCD}$), and
- Slew Rate Decay (downward voltage only and it’s a function of the output capacitance’s time constant) commands. Table 7-3 and Table 7-17 includes SVID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 7-8.

The VR used must be capable of regulating its output to the value defined by the new VID. Power source characteristics must be ensured to be stable whenever the supply to the voltage regulator is stable.

7.1.8.3.2 SetVID Fast Command

The SetVID-fast command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a fast slew rate as defined in the slew rate data register; typically 10 to 20 mV/us depending on platform, voltage rail, and the amount of decoupling capacitance.

The SetVID-fast command is preemptive, the VR interrupts its current processes and moves to the new VID. The SetVID-fast command operates on 1 VR address at a time. This command is used in the processor for package C6 fast exit and entry.

7.1.8.3.3 SetVID Slow

The SetVID-slow command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a “slow” slew rate as defined in the slow slew rate data register. The SetVID_Slow is 1/4 slower than the SetVID_fast slew rate.

The SetVID-slow command is preemptive, the VR interrupts its current processes and moves to the new VID. This is the instruction used for normal P-state voltage change. This command is used in the processor for the Intel Enhanced SpeedStep Technology transitions.

7.1.8.3.4 SetVID Decay

The SetVID-Decay command is the slowest of the DVID transitions. It is only used for VID down transitions. The VR does not control the slew rate, the output voltage declines with the output load current only.

The SetVID-Decay command is preemptive; that is, the VR interrupts its current processes and moves to the new VID.

7.1.8.3.5 SVID Power State Functions – SetPS

The processor has three power state functions and these will be set seamlessly using the SVID bus using the SetPS command. Based on the power state command, the SetPS commands sends information to VR controller to configure the VR to improve efficiency, especially at light loads. For example, typical power states are:

- PS(00h): Represents full power or active mode
- PS(01h): Represents a light load 5 A to 20 A
- PS(02h): Represents a very light load <5 A

The VR may change its configuration to meet the processor's power needs with greater efficiency. For example, it may reduce the number of active phases, transition from CCM (Continuous Conduction Mode) to DCM (Discontinuous Conduction Mode) mode, reduce the switching frequency or pulse skip, or change to asynchronous regulation. For example, typical power states are 00h = run in normal mode; a command of 01h = shed phases mode, and an 02h = pulse skip.

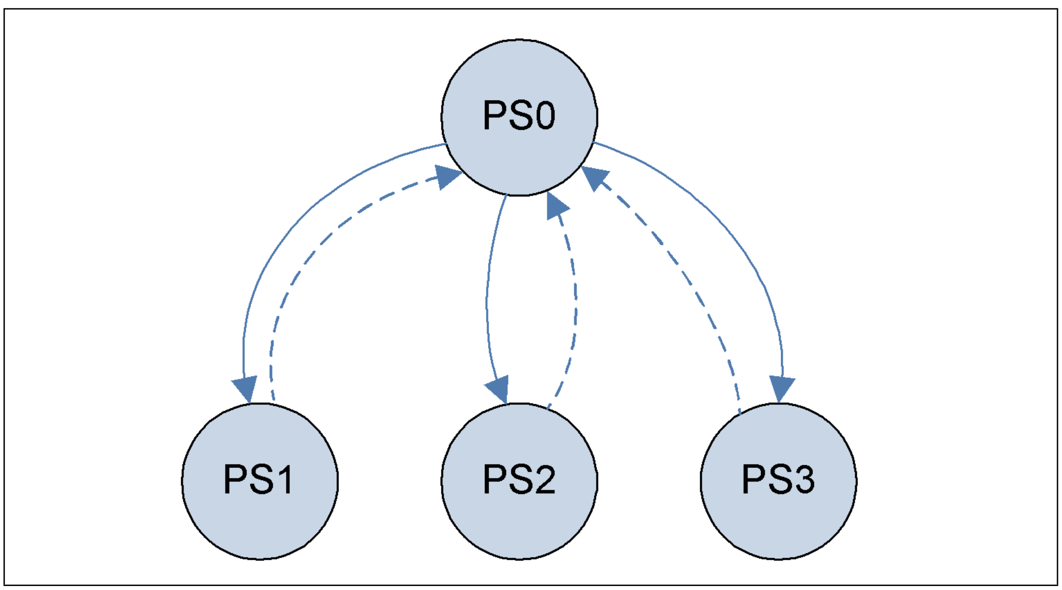
The VR may reduce the number of active phases from PS(00h) to PS(01h) or PS(02h) for example. There are multiple VR design schemes that can be used to maintain a greater efficiency in these different power states, please work with your VR controller suppliers for optimizations.

The SetPS command sends a byte that is encoded as to what power state the VR should transition to.

If a power state is not supported by the controller, the slave should acknowledge with command rejected (11b)

If the VR is in a low power state and receives a SetVID command moving the VID up, then the VR exits the low power state to normal mode (PS0) to move the voltage up as fast as possible. The processor must re-issue low power state (PS1, PS2, or PS3) command if it is in a low current condition at the new higher voltage. See Figure 7-2 for VR power state transitions.

Figure 7-2. VR Power-State Transitions



7.1.8.3.6 SVID Voltage Rail Addressing

The processor addresses 4 different voltage rail control segments within VR12 (VCC, VCCD_01, VCCD_23, and VSA). The SVID data packet contains a 4-bit addressing code.

Table 7-2. SVID Address Usage

PWM Address (HEX)	Processor
00	V_{cc}
01	V_{sa}
02	V_{CCD_01}
03	+1 not used
04	V_{CCD_23}
05	+1 not used

Notes:
1. Check with VR vendors for determining the physical address assignment method for their controllers.
2. VR addressing is assigned on a per voltage rail basis.
3. Dual VR controllers will have two addresses with the lowest order address, always being the higher phase count.
4. For future platform flexibility, the VR controller should include an address offset, as shown with +1 not used.

Table 7-3. Voltage Identification Definition

HEX	Vcc	HEX	Vcc & Vsa	HEX	Vcc & Vsa	HEX	Vcc & Vsa	HEX	Vcc & Vsa	HEX	Vcc
00	0.00000	55	0.67000	78	0.84500	9B	1.02000	BE	1.19500	E1	1.37000
33	0.50000	56	0.67500	79	0.85000	9C	1.02500	BF	1.20000	E2	1.37500
34	0.50500	57	0.68000	7A	0.85500	9D	1.03000	C0	1.20500	E3	1.38000
35	0.51000	58	0.68500	7B	0.86000	9E	1.03500	C1	1.21000	E4	1.38500
36	0.51500	59	0.69000	7C	0.86500	9F	1.04000	C2	1.21500	E5	1.39000
37	0.52000	5A	0.69500	7D	0.87000	A0	1.04500	C3	1.22000	E6	1.39500
38	0.52500	5B	0.70000	7E	0.87500	A1	1.05000	C4	1.22500	E7	1.40000
39	0.53000	5C	0.70500	7F	0.88000	A2	1.05500	C5	1.23000	E8	1.40500
3A	0.53500	5D	0.71000	80	0.88500	A3	1.06000	C6	1.23500	E9	1.41000
3B	0.54000	5E	0.71500	81	0.89000	A4	1.06500	C7	1.24000	EA	1.41500
3C	0.54500	5F	0.72000	82	0.89500	A5	1.07000	C8	1.24500	EB	1.42000
3D	0.55000	60	0.72500	83	0.90000	A6	1.07500	C9	1.25000	EC	1.42500
3E	0.55500	61	0.73000	84	0.90500	A7	1.08000	CA	1.25500	ED	1.43000
3F	0.56000	62	0.73500	85	0.91000	A8	1.08500	CB	1.26000	EE	1.43500
40	0.56500	63	0.74000	86	0.91500	A9	1.09000	CC	1.26500	EF	1.44000
41	0.57000	64	0.74500	87	0.92000	AA	1.09500	CD	1.27000	F0	1.44500
42	0.57500	65	0.75000	88	0.92500	AB	1.10000	CE	1.27500	F1	1.45000
43	0.58000	66	0.75500	89	0.93000	AC	1.10500	CF	1.28000	F2	1.45500
44	0.58500	67	0.76000	8A	0.93500	AD	1.11000	D0	1.28500	F3	1.46000
45	0.59000	68	0.76500	8B	0.94000	AE	1.11500	D1	1.29000	F4	1.46500
46	0.59500	69	0.77000	8C	0.94500	AF	1.12000	D2	1.29500	F5	1.47000
47	0.60000	6A	0.77500	8D	0.95000	B0	1.12500	D3	1.30000	F6	1.47500
48	0.60500	6B	0.78000	8E	0.95500	B1	1.13000	D4	1.30500	F7	1.48000
49	0.61000	6C	0.78500	8F	0.96000	B2	1.13500	D5	1.31000	F8	1.48500
4A	0.61500	6D	0.79000	90	0.96500	B3	1.14000	D6	1.31500	F9	1.49000
4B	0.62000	6E	0.79500	91	0.97000	B4	1.14500	D7	1.32000	FA	1.49500
4C	0.62500	6F	0.80000	92	0.97500	B5	1.15000	D8	1.32500	FB	1.50000
4D	0.63000	70	0.80500	93	0.98000	B6	1.15500	D9	1.33000	FC	1.50500
4E	0.63500	71	0.81000	94	0.98500	B7	1.16000	DA	1.33500	FD	1.51000
4F	0.64000	72	0.81500	95	0.99000	B8	1.16500	DB	1.34000	FE	1.51500
50	0.64500	73	0.82000	96	0.99500	B9	1.17000	DC	1.34500	FF	1.52000
51	0.65000	74	0.82500	97	1.00000	BA	1.17500	DD	1.35000		
52	0.65500	75	0.83000	98	1.00500	BB	1.18000	DE	1.35500		
53	0.66000	76	0.83500	99	1.01000	BC	1.18500	DF	1.36000		
54	0.66500	77	0.84000	9A	1.01500	BD	1.19000	E0	1.36500		

Notes:
1. 00h = Off State
2. VID Range HEX 01–32 are not used by the processor.
3. For VID Ranges supported, see Table 7-9
4. V_{CCD} is a fixed voltage of 1.5 V.

7.1.9 Reserved or Unused Signals

All Reserved (RSVD) signals must not be connected. Connection of these signals to V_{CC}, V_{TTA}, V_{TTD}, V_{CCD}, V_{CCPLL}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Chapter 8, "Processor Land Listing," for a land listing of the processor and the location of all Reserved signals.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability.

7.2 Signal Group Summary

Signals are grouped by buffer type and similar characteristics as listed in Table 7-4. The buffer type indicates which signaling technology and specifications apply to the signals.

Table 7-4. Signal Description Buffer Types

Signal	Description
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation
Asynchronous[1]	Signal has no timing relationship with any system reference clock.
CMOS	CMOS buffers: 1.05 V or 1.5 V tolerant
DDR3	DDR3 buffers: 1.5 V tolerant
DMI2	Direct Media Interface Gen 2 signals. These signals are compatible with PCI Express* 2.0 and 1.0 Signaling Environment AC Specifications.
Open Drain CMOS	Open Drain CMOS (ODCMOS) buffers: 1.05 V tolerant
PCI Express*	PCI Express* interface signals. These signals are compatible with PCI Express* Signalling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Refer to the PCIe specification.
Reference	Voltage reference signal.
SSTL	Source Series Terminated Logic. (JEDEC SSTL_15)

Note:
1. Qualifier for a buffer type.

Table 7-5. Signal Groups (Sheet 1 of 3)

Differential/Single Ended	Buffer Type	Signals[1]
DDR3 Reference Clocks[2]		
Differential	SSTL Output	DDR{0/1/2/3}_CLK_D[N/P][3:0]
DDR3 Command Signals[2]		
Single ended	SSTL Output	DDR{0/1/2/3}_BA[2:0] DDR{0/1/2/3}_CAS_N DDR{0/1/2/3}_MA[15:00] DDR{0/1/2/3}_MA_PAR DDR{0/1/2/3}_RAS_N DDR{0/1/2/3}_WE_N
	CMOS1.5v Output	DDR_RESET_C{01/23}_N
DDR3 Control Signals[2]		
Single ended	CMOS1.5v Output	DDR{0/1/2/3}_CS_N[1:0] DDR{0/1/2/3}_CS_N[5:4] DDR{0/1/2/3}_ODT[3:0] DDR{0/1/2/3}_CKE[3:0]
	Reference Output	DDR_VREFDQTX_C{01/23}
	Reference Input	DDR_VREFDQRX_C{0/1/2/3} DDR{01/23}_RCOMP[2:0]
DDR3 Data Signals[2]		
Differential	SSTL Input/Output	DDR{0/1/2/3}_DQS_D[N/P][08:00]
Single ended	SSTL Input/Output	DDR{0/1/2/3}_DQ[63:00] DDR{0/1/2/3}_ECC[7:0][3]
DDR3 Miscellaneous Signals[2]		
Single ended	CMOS1.5v Input	DRAM_PWR_OK_C{0/1/2/3}
PCI Express* Port 1, 2, & 3 Signals		
Differential	PCI Express* Input	PE1A_RX_D[N/P][3:0] PE1B_RX_D[N/P][7:4] PE2A_RX_D[N/P][3:0] PE2B_RX_D[N/P][7:4] PE2C_RX_D[N/P][11:8] PE2D_RX_D[N/P][15:12] PE3A_RX_D[N/P][3:0] PE3B_RX_D[N/P][7:4] PE3C_RX_D[N/P][11:8] PE3D_RX_D[N/P][15:12]
Differential	PCI Express* Output	PE1A_TX_D[N/P][3:0] PE1B_TX_D[N/P][7:4] PE2A_TX_D[N/P][3:0] PE2B_TX_D[N/P][7:4] PE2C_TX_D[N/P][11:8] PE2D_TX_D[N/P][15:12] PE3A_TX_D[N/P][3:0] PE3B_TX_D[N/P][7:4] PE3C_TX_D[N/P][11:8] PE3D_TX_D[N/P][15:12]

Table 7-5. Signal Groups (Sheet 2 of 3)

Differential/Single Ended	Buffer Type	Signals[1]
PCI Express* Miscellaneous Signals		
Single ended	Analog Input	PE_RBIAS_SENSE
	Reference Input/Output	PE_RBIAS PE_VREF_CAP
DMI2/PCI Express* Signals		
Differential	DMI2 Input	DMI_RX_D[N/P][3:0]
	DMI2 Output	DMI_TX_D[N/P][3:0]
Platform Environmental Control Interface (PECI)		
Single ended	PECI	PECI
System Reference Clock (BCLK{0/1})		
Differential	CMOS1.05v Input	BCLK{0/1}_D[N/P]
SMBus		
Single ended	Open Drain CMOS Input/Output	DDR_SCL_C{01/23} DDR_SDA_C{01/23}
JTAG & TAP Signals		
Single ended	CMOS1.05v Input	TCK, TDI, TMS, TRST_N
	CMOS1.05v Input/Output	PREQ_N
	Open Drain CMOS Input/Output	BPM_N[7:0] EAR_N
	CMOS1.05v Output	PRDY_N
	Open Drain CMOS Output	TDO
Serial VID Interface (SVID) Signals		
Single ended	CMOS1.05v Input	SVIDALERT_N
	Open Drain CMOS Input/Output	SVIDDATA
	Open Drain CMOS Output	SVIDCLK
Processor Asynchronous Sideband Signals		
Single ended	CMOS1.05v Input	PWRGOOD PMSYNC RESET_N
	Open Drain CMOS Input/Output	CAT_ERR_N CPU_ONLY_RESET MEM_HOT_C{01/23}_N PROCHOT_N
	Open Drain CMOS Output	THERMTRIP_N
Miscellaneous Signals		
Single ended	CMOS1.05v Input	BIST_ENABLE BCLK_SELECT[1:0]
N/A	Output	PROC_SEL_N SKTOCC_N
Single ended	Analog Input	CORE_RBIAS_SENSE
	Analog Input/Output	CORE_RBIAS

Table 7-5. Signal Groups (Sheet 3 of 3)

Differential/Single Ended	Buffer Type	Signals[1]
Power/Other Signals		
	Power / Ground	VCC, VTTA, VTTD, VCCD_01, VCCD_23,VCCPLL, VSA and VSS
	Sense Points	VCC_SENSE VSS_VCC_SENSE VSS_VTTD_SENSE VTTD_SENSE VSA_SENSE VSS_VSA_SENSE

Notes:

1. Refer to Chapter 6, "Signal Descriptions," for signal description details.
2. DDR{0/1/2/3} refers to DDR3 Channel 0, DDR3 Channel 1, DDR3 Channel 2, and DDR3 Channel 3.
3. ECC DIMMs are not supported on the processor; thus, these signals are not used.

Table 7-6. Signals with On-Die Termination

Signal Name	Pull Up /Pull Down	Rail	Value	Units	Notes
BCLK_SELECT[1:0]	Pull up	VTT	2K	Ohm	
BIST_ENABLE	Pull Up	VTT	2K	Ohm	
EAR_N	Pull Up	VTT	2K	Ohm	1

Notes:
1. Refer to Table 7-16 for details on the R_{ON} (Buffer on Resistance) value for this signal.

7.3 Power-On Configuration (POC) Options

Several configuration options can be configured by hardware. The processor samples its hardware configuration at reset, on the active-to-inactive transition of RESET_N, or upon assertion of PWRGOOD (inactive-to-active transition). For specifics on these options, refer to Table 7-7.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset transition of the latching signal (RESET_N or PWRGOOD).

Table 7-7. Power-On Configuration Option Lands

Configuration Option	Land Name	Notes
BCLK input select	BCLK_SELECT[1:0]	
Execute BIST (Built-In Self Test)	BIST_ENABLE	1
Power-up Sequence Halt for ITP configuration	EAR_N	2

Notes:
1. BIST_ENABLE is sampled at RESET_N de-assertion.
2. This signal is sampled at PWRGOOD assertion.

7.4 Absolute Maximum and Minimum Ratings

Table 7-8 specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits (but within the absolute maximum and minimum ratings) the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

Although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Table 7-8. Processor Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{CC}	Processor core voltage with respect to Vss	-0.3	1.4	V	1
V_{CCPLL}	Processor PLL voltage with respect to Vss	-0.3	2.0	V	1
V_{CCD}	Processor I/O supply voltage for DDR3 with respect to Vss	-0.3	1.85	V	1
V_{SA}	Processor SA voltage with respect to Vss	-0.3	1.4	V	1
V_{TTA} V_{TTD}	Processor analog I/O voltage with respect to Vss	-0.3	1.4	V	1

Notes:
1. For functional operation, all processor electrical, signal quality, mechanical, and thermal specifications must be satisfied.

7.4.1 Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity limits to which the device is exposed to while being stored in a Moisture Barrier Bag. The storage condition specifications are included in the processor Thermal Mechanical Specification and Design Guide (see Section 1.7, “Related Documents”).

7.5 DC Specifications

DC specifications are defined at the processor pads, unless otherwise noted. DC specifications are only valid while meeting the thermal specifications as specified in the processor Thermal Mechanical Specification and Design Guide (see Section 1.7, "Related Documents"), clock frequency, and input voltages. Care should be taken to read all notes associated with each specification.

7.5.1 Voltage and Current Specifications

Table 7-9. Voltage Specification

Symbol	Parameter	Voltage Plane	Min	Typ	Max	Unit	Notes[1]
V_{CC}VID	V_{CC} VID Range	-	0.6		1.35	V	2, 3, 18
V_{CC}LL	V_{CC} Loadline Slope	V_{CC}	0.8			mΩ	3, 4, 7, 8, 12, 17
V_{CC}TOB	V_{CC} Tolerance Band	V_{CC}	15			mV	3, 4, 7, 8, 12, 17
V_{CC}Ripple	V_{CC} Ripple	Vcc	5			mV	3, 4, 7, 8, 12, 17
V_{CCPLL}	PLL Voltage	V_{CCPLL}	0.955*V_{CCPLL_TYP}	1.8	1.045*V_{CCPLL_TYP}	V	10, 11
V_{CCD} (V_{CCD_01}, V_{CCD_23})	I/O Voltage for DDR3	V_{CCD}	0.95*V_{CCD_TYP}	1.5	1.05*V_{CCD_TYP}	V	11, 14, 15
V_{TT} (V_{TTA}, VTTD)	V_{TT} Uncore Voltage	V_{TT}	0.957*V_{TT_TYP}	1.05	1.043*V_{TT_TYP}	V	3, 5, 9, 11
V_{SA_VID}	V_{SA} VID Range	V_{SA}	0.6	0.965	1.20	V	2, 3, 13, 18
V_{SA}TOB	V_{SA} Tolerance Band (DC+AC+Ripple+Ground Noise)	V_{SA}	64			mV	3, 6, 16, 18

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processors. These specifications are based on pre-silicon characterization and will be updated as further data becomes available.
2. Individual processor VID values may be calibrated during manufacturing such that two devices at the same speed may have different settings.
3. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required.
4. The V_{CC} voltage specification requirements are measured across the remote sense pin pairs (VCC_SENSE and VSS_VCC_SENSE) on the processor package. Voltage measurement should be taken with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using a 1.5 pF maximum probe capacitance, and 1 M Ω minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
5. The $V_{TTA,}$ and V_{TTD} voltage specification requirements are measured across the remote sense pin pairs (VTTD_SENSE and VSS_VTTD_SENSE) on the processor package. Voltage measurement should be taken with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using a 1.5 pF maximum probe capacitance, and 1 M Ω minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
6. The V_{SA} voltage specification requirements are measured across the remote sense pin pairs (VSA_SENSE and VSS_VSA_SENSE) on the processor package. Voltage measurement should be taken with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using a 1.5 pF maximum probe capacitance, and 1 M Ω minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
7. The processor should not be subjected to any static V_{CC} level that exceeds the V_{CC_MAX} associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
8. Minimum V_{CC} and maximum I_{CC} are specified at the maximum processor temperature. Refer to the Thermal Mechanical Specification and Design Guide (see Section 1.7, "Related Documents") for thermal specifications. I_{CC_MAX} is specified at the relative V_{CC_MAX} point on the V_{CC} load line. The processor is capable of drawing I_{CC_MAX} for up to 10 ms.

9. The processor should not be subjected to any static V_{TTA}, V_{TTD} level that exceeds the V_{TT_MAX} associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
10. Baseboard bandwidth is limited to 20 MHz.
11. DC + AC + Ripple specification.
12. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCC_SENSE and VSS_SENSE lands.
13. V_{SA_VID} does not have a loadline, the output voltage is expected to be the VID value.
14. V_{CCD} tolerance at processor pins. Tolerance for VR at remote sense is ±3.3%*V_{CCD}.
15. The V_{CCPLL}, V_{CCD01}, V_{CCD23} voltage specification requirements are measured across vias on the platform. Choose V_{CCPLL}, V_{CCD01}, or V_{CCD23} vias close to the socket and measure with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
16. DC + AC + Ripple + Ground Noise specification.
17. VCC has a Vboot setting of 0.0 V and is not included in the PWRGOOD indication.
18. VSA has a Vboot setting of 0.9 V.

Table 7-10. Current (Icc_Max and Icc_TDC) Specification

Symbol	Parameter	Voltage Plane	4-Core Max	6-Core Max	Unit	Notes[1]
I_{CC_MAX}						
I_{CC_MAX} I_{TT_MAX} I_{SA_MAX} $I_{CCD\_01\_MAX}$ $I_{CCD\_23\_MAX}$ I_{CCPLL_MAX}	Max. Processor Current: (TDP - 130W)	V_{CC} V_{TTA}/V_{TTD} V_{SA} V_{CCD_01} V_{CCD_23} V_{CCPLL}	150 24 24 4 4 2	165 24 24 4 4 2	A A A A A A	4, 5
I_{CC_TDC}						
I_{CC_TDC} I_{TT_TDC} I_{SA_TDC} $I_{CCD\_01\_TDC}$ $I_{CCD\_23\_TDC}$ I_{CCPLL_TDC}	Thermal Design Current: (TDP - 130 W)	V_{CC} V_{TTA}/V_{TTD} V_{SA} V_{CCD_01} V_{CCD_23} V_{CCPLL}	115 20 20 3 3 2	135 20 20 3 3 2	A A A A A A	2, 5
I_{CCD_S3}	DDR3 System Memory Interface Supply Current in Standby State	V_{CCD_01} V_{CCD_23}	TBD	TBD	A	3, 4

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processors. These specifications are based on pre-silicon characterization and will be updated as further data becomes available.
2. I_{CC_TDC} (Thermal Design Current) is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator thermal assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion.
3. Specification is at T_{CASE} = 50 °C. Characterized by design (not tested).
4. $I_{CCD\_01\_MAX}$ and $I_{CCD\_23\_MAX}$ refers only to the processor's current draw and does not account for the current consumption by the memory devices.
5. Minimum V_{CC} and maximum I_{CC} are specified at the maximum processor temperature. Refer to the processor Thermal Mechanical Specification and Design Guide (see Section 1.7, "Related Documents") for thermal specifications. ICC_MAX is specified at the relative V_{CC_MAX} point on the V_{CC} load line. The processor is capable of drawing I_{CC_MAX} for up to 10 ms.

7.5.2 Die Voltage Validation

Core voltage (V_{CC}) overshoot events at the processor must meet the specifications in Table 7-11 when measured across the VCC_SENSE and VSS_VCC_SENSE lands. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

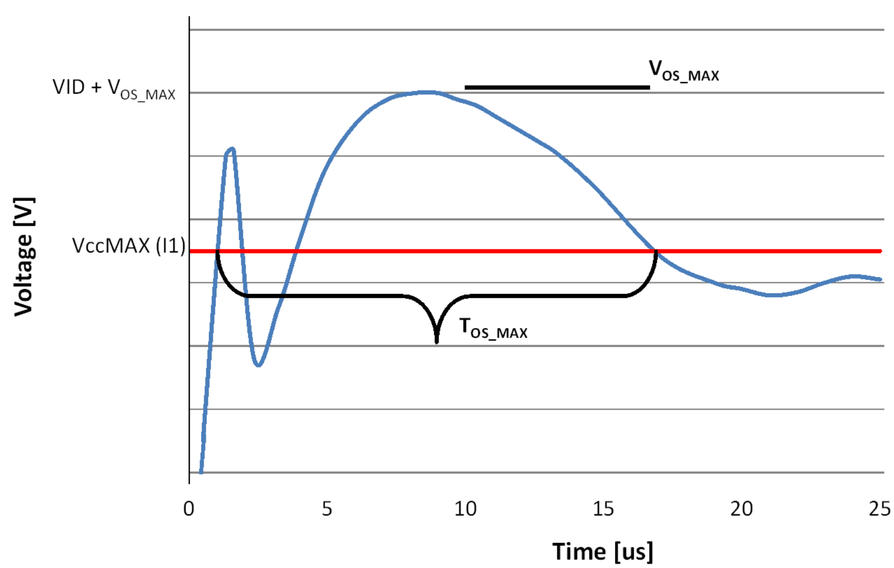
7.5.2.1 V_{CC} Overshoot Specifications

The processor can tolerate short transient overshoot events where V_{CC} exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID + V_{OS_MAX} (V_{OS_MAX} is the maximum allowable overshoot above VID). These specifications apply to the processor die voltage as measured across the VCC_SENSE and VSS_VCC_SENSE lands.

Table 7-11. V_{CC} Overshoot Specifications

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CC} overshoot above VID	—	65	mV	7-3	
T_{OS_MAX}	Time duration of V_{CC} overshoot above VccMAX value at the new lighter load	—	25	ms	7-3	

Figure 7-3. V_{CC} Overshoot Example Waveform



Notes:
1. V_{OS} is the measured overshoot voltage.
2. T_{OS_MAX} is the measured time duration above VccMAX(I1).
3. Istep: Load Release Current Step, for example, I2 to I1, where I2 > I1.
4. VccMAX(I1) = VID - I1*RLL + 15 mV

7.5.3 Signal DC Specifications

DC specifications are defined at the processor pads, unless otherwise noted. DC specifications are only valid while meeting specifications for case temperature (T_{CASE} specified in the processor Thermal Mechanical Specification and Design Guide; see Section 1.7, "Related Documents"), clock frequency, and input voltages. Care should be taken to read all notes associated with each specification.

Table 7-12. DDR3 Signal DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
I_{IL}	Input Leakage Current	-500	—	+500	uA	10
Data Signals						
V_{IL}	Input Low Voltage	—	—	$0.43*V_{CCD}$	V	2, 3
V_{IH}	Input High Voltage	$0.57*V_{CCD}$	—		V	2, 4, 5
R_{ON}	DDR3 Data Buffer On Resistance	21	—	31	Ω	6
Data ODT	On-Die Termination for Data Signals	45 90	—	55 110	Ω	8
Reference Clock Signals, Command, and Data Signals						
V_{OL}	Output Low Voltage	—	$(V_{CCD}/ 2)* (R_{ON} /(R_{ON}+R_{VTT\_TERM}))$	—	V	2, 7
V_{OH}	Output High Voltage	—	$V_{CCD} – ((V_{CCD}/ 2)* (R_{ON}/(R_{ON}+R_{VTT\_TERM}))$	—	V	2, 5, 7
Reference Clock Signal						
R_{ON}	DDR3 Clock Buffer On Resistance	21	—	31	Ω	6
Command Signals						
R_{ON}	DDR3 Command Buffer On Resistance	16	—	24	Ω	6
R_{ON}	DDR3 Reset Buffer On Resistance	25	—	75	Ω	6
$V_{OL\_CMOS1.5v}$	Output Low Voltage, Signals DDR_RESET_ C{01/23}_N	—	—	$0.2*V_{CCD}$	V	1, 2
$V_{OH\_CMOS1.5v}$	Output High Voltage, Signals DDR_RESET_ C{01/23}_N	$0.9*V_{CCD}$	—	—	V	1, 2
IIL_CMOS1.5v	Input Leakage Current	-100	—	+100	uA	1, 2
Control Signals						
R_{ON}	DDR3 Control Buffer On Resistance	21	—	31	Ω	6
DDR01_RCOMP[0]	COMP Resistance	128.7	130	131.3	Ω	9, 12
DDR01_RCOMP[1]	COMP Resistance	25.839	26.1	26.361	Ω	9, 12
DDR01_RCOMP[2]	COMP Resistance	198	200	202	Ω	9, 12
DDR23_RCOMP[0]	COMP Resistance	128.7	130	131.3	Ω	9, 12
DDR23_RCOMP[1]	COMP Resistance	25.839	26.1	26.361	Ω	9, 12
DDR23_RCOMP[2]	COMP Resistance	198	200	202	Ω	9, 12
Miscellaneous Signals						
V_{IL}	Input Low Voltage DRAM_PWR_OK_C{01/23}	—	—	0.55*VCCD – 0.2	V	2, 3, 11, 13
V_{IH}	Input High Voltage DRAM_PWR_OK_C{01/23}	0.55*VCCD +0.2	—	—	V	2, 4, 5, 11, 13

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The voltage rail V_{CCD} will be set to 1.50 V nominal.
3. V_{IL} is the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
4. V_{IH} is the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{CCD}.

6. This is the pull-down driver resistance. Reset drive does not have a termination.
7. R_{VTT_TERM} is the termination on the DIMM and not controlled by the processor. Refer to the applicable DIMM datasheet.
8. The minimum and maximum values for these signals are programmable by BIOS to one of the pairs.
9. COMP resistance must be provided on the system board with 1% resistors.
10. Input leakage current is specified for all DDR3 signals.
11. DRAM_PWR_OK_C{01/23} must have a maximum of 30 ns rise or fall time over VCCD * 0.55 + 300 mV and -200 mV and the edge must be monotonic.
12. The DDR01/23_RCOMP error tolerance is ±5% from the compensated value.
13. DRAM_PWR_OK_C{01/23}: Data Scrambling should be enabled for production environments. Disabling Data scrambling can be used for debug and testing purposes only. Running systems with Data Scrambling off will make the configuration out of specification. For details, refer to Volume 2 of the Datasheet.

Table 7-13. PECI DC Specifications

Symbol	Definition and Conditions	Min	Max	Units	Figure	Notes[1]
V_{In}	Input Voltage Range	-0.150	V_{TTD}	V		
$V_{Hysteresis}$	Hysteresis	0.100 * V_{TTD}	—	V		
V_N	Negative-edge threshold voltage	0.275 * V_{TTD}	0.500 * V_{TTD}	V	7-1	2
V_P	Positive-edge threshold voltage	0.550 * V_{TTD}	0.725 * V_{TTD}	V	7-1	2
I_{SOURCE}	High level output source V_{OH} = 0.75 * V_{TT}	-6.0	—	mA		
I_{Leak+}	High impedance state leakage to V_{TTD} (V_{leak} = V_{OL})	N/A	50	µA		3
I_{Leak-}	High impedance leakage to GND (V_{leak} = V_{OH})	N/A	25	µA		3
C_{Bus}	Bus capacitance per node	N/A	10	pF		4,5
V_{Noise}	Signal noise immunity above 300 MHz	0.100 * V_{TTD}	N/A	V_{p-p}		

Notes:
1. V_{TTD} supplies the PECI interface. PECI behavior does not affect V_{TTD} min/max specification
2. It is expected that the PECI driver will take into account, the variance in the receiver input thresholds and consequently, be able to drive its output within safe limits (-0.150 V to 0.275*V_{TTD} for the low level and 0.725*V_{TTD} to V_{TTD}+0.150 V for the high level).
3. The leakage specification applies to powered devices on the PECI bus.
4. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.
5. Excessive capacitive loading on the PECI line may slow down the signal rise/fall times and consequently limit the maximum bit rate at which the interface can operate.

Table 7-14. System Reference Clock (BCLK{0/1}) DC Specifications

Symbol	Parameter	Signal	Min	Max	Unit	Figure	Notes[1]
$V_{BCLK\_diff\_ih}$	Differential Input High Voltage	Differential	0.150	N/A	V		
$V_{BCLK\_diff\_il}$	Differential Input Low Voltage	Differential	—	-0.150	V		
V_{cross} (abs)	Absolute Crossing Point	Single Ended	0.250	0.550	V		2, 4, 7
V_{cross}(rel)	Relative Crossing Point	Single Ended	0.250 + 0.5*(VH_{avg} – 0.700)	0.550 + 0.5*(VH_{avg} – 0.700)	V		3, 4, 5
ΔV_{cross}	Range of Crossing Points	Single Ended	N/A	0.140	V		6
V_{TH}	Threshold Voltage	Single Ended	Vcross – 0.1	Vcross + 0.1	V		
I_{IL}	Input Leakage Current	N/A	—	1.50	µA		8
C_{pad}	Pad Capacitance	N/A	0.9	1.1	pF		

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as the instantaneous voltage value when the rising edge of BCLK{0/1}_DN is equal to the falling edge of BCLK{0/1}_DP.
3. V_{Havg} is the statistical average of the VH measured by the oscilloscope.
4. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
5. V_{Havg} can be measured directly using “Vtop” on Agilent* and “High” on Tektronix oscilloscopes.
6. V_{CROSS} is defined as the total variation of all crossing voltages as defined in Note 3.
7. The rising edge of BCLK{0/1}_DN is equal to the falling edge of BCLK{0/1}_DP.
8. For Vin between 0 and V_{ih}.

Table 7-15. SMBus DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	—	$0.3*V_{TT}$	V	
V_{IH}	Input High Voltage	0.7*VTT	—	V	
V_{OL}	Output Low Voltage	—	$0.2*V_{TT}$	V	
V_{OH}	Output High Voltage	—	$V_{TT(max)}$	V	
R_{ON}	Buffer On Resistance	—	14	Ω	
I_L	Leakage Current, Signals DDR_SCL_C{01/23}, DDR_SDA_C{01/23}	-100	+100	µA	

Table 7-16. JTAG and TAP Signals DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	—	0.3*VTT	V	
V_{IH}	Input High Voltage	0.7*VTT	—	V	
V_{OL}	Output Low Voltage (R_{TEST} = 500 ohm)	—	0.12*V_{TT}	V	
V_{OH}	Output High Voltage (R_{TEST} = 500 ohm)	0.88*V_{TT}	—	V	
R_{ON}	Buffer On Resistance Signals BPM[7:0], TDO, EAR_N	—	14	Ω	
I_{IL}	Input Leakage Current, Signals PREQ_N, TCK, TDI, TMS, TRST_N	-50	+50	µA	
I_{IL}	Input Leakage Current, Signals BPM_N[7:0], TDO, EAR_N (R_{TEST} = 50 ohm)	—	+900	µA	
I_O	Output Current, Signal PRDY_N (R_{TEST} = 500 ohm)	-1.50	+1.50	mA	
	Input Edge Rate Signals: BPM_N[7:0], EAR_N, PREQ_N, TCK, TDI, TMS, TRST_N	0.05	—	V/ns	1

Notes:
1. These are measured between V_{IL} and V_{IH}.

Table 7-17. Serial VID Interface (SVID) DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{TT}	CPU I/O Voltage	VTT - 3%	1.05	VTT + 3%	V	
V_{IL}	Input Low Voltage SVIDDATA, SVIDALERT_N	—	—	0.3*V_{TT}	V	1
V_{IH}	Input High Voltage SVIDDATA, SVIDALERT_N	0.7*V_{TT}	—	—	V	1
V_{OH}	Output High Voltage SVIDCLK, SVIDDATA	—	—	$V_{TT(max)}$	V	1
R_{ON}	Buffer On Resistance SVIDCLK, SVIDDATA	—		14	Ω	2
I_{IL}	Input Leakage Current, Signals SVIDCLK, SVIDDATA	—	—	+900	µA	3
I_{IL}	Input Leakage Current, Signal SVIDALERT_N	-500	—	+500	µA	3

Notes:
1. V_{TT} refers to instantaneous V_{TT}.
2. Measured at 0.31*V_{TT}
3. Vin between 0 V and V_{TT}

Table 7-18. Processor Asynchronous Sideband DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
	Input Edge Rate Signals: CAT_ERR_N, MEM_HOT_C{01/23}_N, PMSYNC, PROCHOT_N, PWRGOOD, RESET_N	0.05	—	V/ns	5
CMOS1.05 V Signals					
$V_{IL\_CMOS1.05v}$	Input Low Voltage	—	$0.3*V_{TT}$	V	1,2
$V_{IH\_CMOS1.05v}$	Input High Voltage	$0.7*V_{TT}$		V	1,2
V_{IL_MAX}	Input Low Voltage Signal PWRGOOD	—	0.320	V	1,2,4
V_{IH_MIN}	Input High Voltage Signal PWRGOOD	0.640	—	V	1,2,4
$V_{OL\_CMOS1.05v}$	Output Low Voltage	—	$0.12*V_{TT}$	V	1,2
$V_{OH\_CMOS1.05v}$	Output High Voltage	$0.88*V_{TT}$	—	V	1,2
$I_{IL\_CMOS1.05v}$	Input Leakage Current	-50	+50	µA	1,2
$I_{O\_CMOS1.05v}$	Output Current (R_{TEST} = 500 ohm)	-1.50	+1.50	mA	1,2
A_{NM_Rise}	Non-Monotonicity Amplitude, Rising Edge Signal PWRGOOD	—	0.135	V	4
A_{NM_Fall}	Non-Monotonicity Amplitude, Falling Edge Signal PWRGOOD	—	0.165	V	4
Open Drain CMOS (ODCMOS) Signals					
V_{IL_ODCMOS}	Input Low Voltage	—	$0.3*V_{TT}$	V	1,2
V_{IH_ODCMOS}	Input High Voltage	$0.7*V_{TT}$	—	V	1,2
V_{OH_ODCMOS}	Output High Voltage, Signals CAT_ERR_N, ERROR_N[2:0], THERMTRIP_N, PROCHOT_N, CPU_ONLY_RESET	—	$V_{TT(max)}$	V	1,2
I_{OL}	Output Leakage Current, Signal: MEM_HOT_C{01/23}_N	-100	+100	µA	3
I_{OL}	Output Leakage Current (R_{TEST} = 50 ohm)	—	+900	µA	3
R_{ON}	Buffer On Resistance, Signals: CAT_ERR_N, CPU_ONLY_RESET, ERROR_N[2:0], MEM_HOT_C{01/23}_N, PROCHOT_N, THERMTRIP_N	—	14	Ω	1,2

Note:
1. This table applies to the miscellaneous signals specified in Table 7-5.
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. For Vin between 0 and V_{OH}.
4. PWRGOOD Non Monotonicity duration (T_{NM}) time is maximum 1.3 ns.
5. These are measured between V_{IL} and V_{IH} and the edge must be monotonic.

Table 7-19. Miscellaneous Signals DC Specifications

Symbol	Parameter	Min	Typical	Max	Units	Notes
PROC_SEL_N Signal						
$V_{O\_ABS\_MAX}$	Output Absolute Max Voltage	—	1.10	1.80	V	1
I_O	Output Current	—	—	0	µA	1
SKTOCC_N Signal						
$V_{O\_ABS\_MAX}$	Output Absolute Max Voltage	—	3.30	3.50	V	
I_{OMAX}	Output Max Current	—	—	1	mA	

Notes:
1. 10 kΩ pull-up and 4 kΩ pull-down to a voltage divider from +3.3 V.

7.5.3.1 PCI Express* DC Specifications

The DC specifications for the PCI Express* are available in the *PCI Express* Base Specification*. This document will provide only the processor exceptions to the *PCI Express* Base Specification*.

Note: The processor is capable of up to 8.0 GT/s speeds.

7.5.3.2 DMI2/PCI Express* DC Specifications

The DC specifications for the DMI2/PCI Express* are available in the *PCI Express®* Base Specification 2.0 and 1.0. This document will provide only the processor exceptions to the *PCI Express®* Base Specification 2.0 and 1.0.

7.5.3.3 Reset and Miscellaneous Signal DC Specifications

For a power-on Reset, RESET_N must stay active for at least 3.5 milliseconds after V_{CC} and BCLK have reached their proper specifications. RESET_N must not be kept asserted for more than 100 ms while PWRGOOD is asserted. RESET_N must be held asserted for at least 3.5 milliseconds before it is deasserted again. RESET_N must be held asserted before PWRGOOD is asserted. This signal does not have on-die termination and must be terminated on the system board.

§

8 Processor Land Listing

This chapter provides sorted land list. Table 8-1 is a listing of all processor lands ordered alphabetically by land name. Table 8-2 is a listing of all processor lands ordered by land number.

Table 8-1. Land Name (Sheet 1 of 45)

Land Name	Land No.	Buffer Type	Direction
BCLK_SELECT[0]	BD48	CMOS	I
BCLK_SELECT[1]	AJ55	CMOS	I
BCLK0_DN	CM44	CMOS	I
BCLK0_DP	CN43	CMOS	I
BCLK1_DN	BA45	CMOS	I
BCLK1_DP	AW45	CMOS	I
BIST_ENABLE	AT48	CMOS	I
BPM_N[0]	AR43	ODCMOS	I/O
BPM_N[1]	AT44	ODCMOS	I/O
BPM_N[2]	AU43	ODCMOS	I/O
BPM_N[3]	AV44	ODCMOS	I/O
BPM_N[4]	BB44	ODCMOS	I/O
BPM_N[5]	AW43	ODCMOS	I/O
BPM_N[6]	BA43	ODCMOS	I/O
BPM_N[7]	AY44	ODCMOS	I/O
CAT_ERR_N	CC51	ODCMOS	I/O
CORE_RBIAS	CE53	Analog	I/O
CORE_RBIAS_SENSE	CC53	Analog	I
CORE_VREF_CAP	CU51		I/O
CPU_ONLY_RESET	AN43	ODCMOS	I/O
DDR_RESET_C01_N	CB18	CMOS1.5v	O
DDR_RESET_C23_N	AE27	CMOS1.5v	O
DDR_SCL_C01	CY42	ODCMOS	I/O
DDR_SCL_C23	U43	ODCMOS	I/O
DDR_SDA_C01	CW41	ODCMOS	I/O
DDR_SDA_C23	R43	ODCMOS	I/O
DDR_VREFDQRX_C01	BY16	DC	I
DDR_VREFDQRX_C23	J1	DC	I
DDR_VREFDQTX_C01	CN41	DC	O
DDR_VREFDQTX_C23	P42	DC	O
DDR0_BA[0]	CM28	SSTL	O
DDR0_BA[1]	CN27	SSTL	O
DDR0_BA[2]	CM20	SSTL	O
DDR0_CAS_N	CL29	SSTL	O
DDR0_CKE[0]	CL19	SSTL	O
DDR0_CKE[1]	CM18	SSTL	O
DDR0_CKE[2]	CH20	SSTL	O
DDR0_CKE[3]	CP18	SSTL	O
DDR0_CLK_DN[0]	CF24	SSTL	O
DDR0_CLK_DN[1]	CE23	SSTL	O
DDR0_CLK_DN[2]	CE21	SSTL	O
DDR0_CLK_DN[3]	CF22	SSTL	O
DDR0_CLK_DP[0]	CH24	SSTL	O
DDR0_CLK_DP[1]	CG23	SSTL	O
DDR0_CLK_DP[2]	CG21	SSTL	O

Table 8-1. Land Name (Sheet 2 of 45)

Land Name	Land No.	Buffer Type	Direction
DDR0_CLK_DP[3]	CH22	SSTL	O
DDR0_CS_N[0]	CN25	SSTL	O
DDR0_CS_N[1]	CH26	SSTL	O
DDR0_CS_N[4]	CG27	SSTL	O
DDR0_CS_N[5]	CF26	SSTL	O
DDR0_DQ[00]	CC7	SSTL	I/O
DDR0_DQ[01]	CD8	SSTL	I/O
DDR0_DQ[02]	CK8	SSTL	I/O
DDR0_DQ[03]	CL9	SSTL	I/O
DDR0_DQ[04]	BY6	SSTL	I/O
DDR0_DQ[05]	CA7	SSTL	I/O
DDR0_DQ[06]	CJ7	SSTL	I/O
DDR0_DQ[07]	CL7	SSTL	I/O
DDR0_DQ[08]	CB2	SSTL	I/O
DDR0_DQ[09]	CB4	SSTL	I/O
DDR0_DQ[10]	CH4	SSTL	I/O
DDR0_DQ[11]	CJ5	SSTL	I/O
DDR0_DQ[12]	CA1	SSTL	I/O
DDR0_DQ[13]	CA3	SSTL	I/O
DDR0_DQ[14]	CG3	SSTL	I/O
DDR0_DQ[15]	CG5	SSTL	I/O
DDR0_DQ[16]	CK12	SSTL	I/O
DDR0_DQ[17]	CM12	SSTL	I/O
DDR0_DQ[18]	CK16	SSTL	I/O
DDR0_DQ[19]	CM16	SSTL	I/O
DDR0_DQ[20]	CG13	SSTL	I/O
DDR0_DQ[21]	CL11	SSTL	I/O
DDR0_DQ[22]	CJ15	SSTL	I/O
DDR0_DQ[23]	CL15	SSTL	I/O
DDR0_DQ[24]	BY10	SSTL	I/O
DDR0_DQ[25]	BY12	SSTL	I/O
DDR0_DQ[26]	CB12	SSTL	I/O
DDR0_DQ[27]	CD12	SSTL	I/O
DDR0_DQ[28]	BW9	SSTL	I/O
DDR0_DQ[29]	CA9	SSTL	I/O
DDR0_DQ[30]	CH10	SSTL	I/O
DDR0_DQ[31]	CF10	SSTL	I/O
DDR0_DQ[32]	CE31	SSTL	I/O
DDR0_DQ[33]	CC31	SSTL	I/O
DDR0_DQ[34]	CE35	SSTL	I/O
DDR0_DQ[35]	CC35	SSTL	I/O
DDR0_DQ[36]	CD30	SSTL	I/O
DDR0_DQ[37]	CB30	SSTL	I/O
DDR0_DQ[38]	CD34	SSTL	I/O
DDR0_DQ[39]	CB34	SSTL	I/O

Table 8-1. Land Name (Sheet 3 of 45)

Land Name	Land No.	Buffer Type	Direction
DDR0_DQ[40]	CL31	SSTL	I/O
DDR0_DQ[41]	CJ31	SSTL	I/O
DDR0_DQ[42]	CL35	SSTL	I/O
DDR0_DQ[43]	CJ35	SSTL	I/O
DDR0_DQ[44]	CK30	SSTL	I/O
DDR0_DQ[45]	CH30	SSTL	I/O
DDR0_DQ[46]	CK34	SSTL	I/O
DDR0_DQ[47]	CH34	SSTL	I/O
DDR0_DQ[48]	CB38	SSTL	I/O
DDR0_DQ[49]	CD38	SSTL	I/O
DDR0_DQ[50]	CE41	SSTL	I/O
DDR0_DQ[51]	CD42	SSTL	I/O
DDR0_DQ[52]	CC37	SSTL	I/O
DDR0_DQ[53]	CE37	SSTL	I/O
DDR0_DQ[54]	CC41	SSTL	I/O
DDR0_DQ[55]	CB42	SSTL	I/O
DDR0_DQ[56]	CH38	SSTL	I/O
DDR0_DQ[57]	CK38	SSTL	I/O
DDR0_DQ[58]	CH42	SSTL	I/O
DDR0_DQ[59]	CK42	SSTL	I/O
DDR0_DQ[60]	CJ37	SSTL	I/O
DDR0_DQ[61]	CL37	SSTL	I/O
DDR0_DQ[62]	CJ41	SSTL	I/O
DDR0_DQ[63]	CL41	SSTL	I/O
DDR0_DQS_DN[00]	CG7	SSTL	I/O
DDR0_DQS_DN[01]	CE3	SSTL	I/O
DDR0_DQS_DN[02]	CH14	SSTL	I/O
DDR0_DQS_DN[03]	CD10	SSTL	I/O
DDR0_DQS_DN[04]	CE33	SSTL	I/O
DDR0_DQS_DN[05]	CL33	SSTL	I/O
DDR0_DQS_DN[06]	CB40	SSTL	I/O
DDR0_DQS_DN[07]	CH40	SSTL	I/O
DDR0_DQS_DN[08]	CE17	SSTL	I/O
DDR0_DQS_DP[00]	CH8	SSTL	I/O
DDR0_DQS_DP[01]	CF4	SSTL	I/O
DDR0_DQS_DP[02]	CK14	SSTL	I/O
DDR0_DQS_DP[03]	CE11	SSTL	I/O
DDR0_DQS_DP[04]	CC33	SSTL	I/O
DDR0_DQS_DP[05]	CJ33	SSTL	I/O
DDR0_DQS_DP[06]	CD40	SSTL	I/O
DDR0_DQS_DP[07]	CK40	SSTL	I/O
DDR0_DQS_DP[08]	CC17	SSTL	I/O
DDR0_ECC[0]	CE15	SSTL	I/O
DDR0_ECC[1]	CC15	SSTL	I/O
DDR0_ECC[2]	CH18	SSTL	I/O

Table 8-1. Land Name (Sheet 4 of 45)

Land Name	Land No.	Buffer Type	Direction
DDR0_ECC[3]	CF18	SSTL	I/O
DDR0_ECC[4]	CB14	SSTL	I/O
DDR0_ECC[5]	CD14	SSTL	I/O
DDR0_ECC[6]	CG17	SSTL	I/O
DDR0_ECC[7]	CK18	SSTL	I/O
DDR0_MA[00]	CL25	SSTL	O
DDR0_MA[01]	CR25	SSTL	O
DDR0_MA[02]	CG25	SSTL	O
DDR0_MA[03]	CK24	SSTL	O
DDR0_MA[04]	CM24	SSTL	O
DDR0_MA[05]	CL23	SSTL	O
DDR0_MA[06]	CN23	SSTL	O
DDR0_MA[07]	CM22	SSTL	O
DDR0_MA[08]	CK22	SSTL	O
DDR0_MA[09]	CN21	SSTL	O
DDR0_MA[10]	CK26	SSTL	O
DDR0_MA[11]	CL21	SSTL	O
DDR0_MA[12]	CK20	SSTL	O
DDR0_MA[13]	CG29	SSTL	O
DDR0_MA[14]	CG19	SSTL	O
DDR0_MA[15]	CN19	SSTL	O
DDR0_ODT[0]	CE25	SSTL	O
DDR0_ODT[1]	CE27	SSTL	O
DDR0_ODT[2]	CH28	SSTL	O
DDR0_ODT[3]	CF28	SSTL	O
DDR0_RAS_N	CE29	SSTL	O
DDR0_WE_N	CN29	SSTL	O
DDR01_RCOMP[0]	CA17	Analog	I
DDR01_RCOMP[1]	CC19	Analog	I
DDR01_RCOMP[2]	CB20	Analog	I
DDR1_BA[0]	DB26	SSTL	O
DDR1_BA[1]	DC25	SSTL	O
DDR1_BA[2]	DF18	SSTL	O
DDR1_CAS_N	CY30	SSTL	O
DDR1_CKE[0]	CT20	SSTL	O
DDR1_CKE[1]	CU19	SSTL	O
DDR1_CKE[2]	CY18	SSTL	O
DDR1_CKE[3]	DA17	SSTL	O
DDR1_CLK_DN[0]	CV20	SSTL	O
DDR1_CLK_DN[1]	CV22	SSTL	O
DDR1_CLK_DN[2]	CY24	SSTL	O
DDR1_CLK_DN[3]	DA21	SSTL	O
DDR1_CLK_DP[0]	CY20	SSTL	O
DDR1_CLK_DP[1]	CY22	SSTL	O
DDR1_CLK_DP[2]	CV24	SSTL	O

Table 8-1. Land Name (Sheet 5 of 45)

Land Name	Land No.	Buffer Type	Direction
DDR1_CLK_DP[3]	DC21	SSTL	O
DDR1_CS_N[0]	DB24	SSTL	O
DDR1_CS_N[1]	CU23	SSTL	O
DDR1_CS_N[4]	CU25	SSTL	O
DDR1_CS_N[5]	CT24	SSTL	O
DDR1_DQ[00]	CP4	SSTL	I/O
DDR1_DQ[01]	CP2	SSTL	I/O
DDR1_DQ[02]	CV4	SSTL	I/O
DDR1_DQ[03]	CY4	SSTL	I/O
DDR1_DQ[04]	CM4	SSTL	I/O
DDR1_DQ[05]	CL3	SSTL	I/O
DDR1_DQ[06]	CV2	SSTL	I/O
DDR1_DQ[07]	CW3	SSTL	I/O
DDR1_DQ[08]	DA7	SSTL	I/O
DDR1_DQ[09]	DC7	SSTL	I/O
DDR1_DQ[10]	DC11	SSTL	I/O
DDR1_DQ[11]	DE11	SSTL	I/O
DDR1_DQ[12]	CY6	SSTL	I/O
DDR1_DQ[13]	DB6	SSTL	I/O
DDR1_DQ[14]	DB10	SSTL	I/O
DDR1_DQ[15]	DF10	SSTL	I/O
DDR1_DQ[16]	CR7	SSTL	I/O
DDR1_DQ[17]	CU7	SSTL	I/O
DDR1_DQ[18]	CT10	SSTL	I/O
DDR1_DQ[19]	CP10	SSTL	I/O
DDR1_DQ[20]	CP6	SSTL	I/O
DDR1_DQ[21]	CT6	SSTL	I/O
DDR1_DQ[22]	CW9	SSTL	I/O
DDR1_DQ[23]	CV10	SSTL	I/O
DDR1_DQ[24]	CR13	SSTL	I/O
DDR1_DQ[25]	CU13	SSTL	I/O
DDR1_DQ[26]	CR17	SSTL	I/O
DDR1_DQ[27]	CU17	SSTL	I/O
DDR1_DQ[28]	CT12	SSTL	I/O
DDR1_DQ[29]	CV12	SSTL	I/O
DDR1_DQ[30]	CT16	SSTL	I/O
DDR1_DQ[31]	CV16	SSTL	I/O
DDR1_DQ[32]	CT30	SSTL	I/O
DDR1_DQ[33]	CP30	SSTL	I/O
DDR1_DQ[34]	CT34	SSTL	I/O
DDR1_DQ[35]	CP34	SSTL	I/O
DDR1_DQ[36]	CU29	SSTL	I/O
DDR1_DQ[37]	CR29	SSTL	I/O
DDR1_DQ[38]	CU33	SSTL	I/O
DDR1_DQ[39]	CR33	SSTL	I/O

Table 8-1. Land Name (Sheet 6 of 45)

Land Name	Land No.	Buffer Type	Direction
DDR1_DQ[40]	DA33	SSTL	I/O
DDR1_DQ[41]	DD32	SSTL	I/O
DDR1_DQ[42]	DC35	SSTL	I/O
DDR1_DQ[43]	DA35	SSTL	I/O
DDR1_DQ[44]	DA31	SSTL	I/O
DDR1_DQ[45]	CY32	SSTL	I/O
DDR1_DQ[46]	DF34	SSTL	I/O
DDR1_DQ[47]	DE35	SSTL	I/O
DDR1_DQ[48]	CR37	SSTL	I/O
DDR1_DQ[49]	CU37	SSTL	I/O
DDR1_DQ[50]	CR41	SSTL	I/O
DDR1_DQ[51]	CU41	SSTL	I/O
DDR1_DQ[52]	CT36	SSTL	I/O
DDR1_DQ[53]	CV36	SSTL	I/O
DDR1_DQ[54]	CT40	SSTL	I/O
DDR1_DQ[55]	CV40	SSTL	I/O
DDR1_DQ[56]	DE37	SSTL	I/O
DDR1_DQ[57]	DF38	SSTL	I/O
DDR1_DQ[58]	DD40	SSTL	I/O
DDR1_DQ[59]	DB40	SSTL	I/O
DDR1_DQ[60]	DA37	SSTL	I/O
DDR1_DQ[61]	DC37	SSTL	I/O
DDR1_DQ[62]	DA39	SSTL	I/O
DDR1_DQ[63]	DF40	SSTL	I/O
DDR1_DQS_DN[00]	CT4	SSTL	I/O
DDR1_DQS_DN[01]	DC9	SSTL	I/O
DDR1_DQS_DN[02]	CV8	SSTL	I/O
DDR1_DQS_DN[03]	CR15	SSTL	I/O
DDR1_DQS_DN[04]	CT32	SSTL	I/O
DDR1_DQS_DN[05]	CY34	SSTL	I/O
DDR1_DQS_DN[06]	CR39	SSTL	I/O
DDR1_DQS_DN[07]	DE39	SSTL	I/O
DDR1_DQS_DN[08]	DE15	SSTL	I/O
DDR1_DQS_DP[00]	CR3	SSTL	I/O
DDR1_DQS_DP[01]	DE9	SSTL	I/O
DDR1_DQS_DP[02]	CU9	SSTL	I/O
DDR1_DQS_DP[03]	CU15	SSTL	I/O
DDR1_DQS_DP[04]	CP32	SSTL	I/O
DDR1_DQS_DP[05]	DB34	SSTL	I/O
DDR1_DQS_DP[06]	CU39	SSTL	I/O
DDR1_DQS_DP[07]	DC39	SSTL	I/O
DDR1_DQS_DP[08]	DC15	SSTL	I/O
DDR1_ECC[0]	DE13	SSTL	I/O
DDR1_ECC[1]	DF14	SSTL	I/O
DDR1_ECC[2]	DD16	SSTL	I/O

Table 8-1. Land Name (Sheet 7 of 45)

Land Name	Land No.	Buffer Type	Direction
DDR1_ECC[3]	DB16	SSTL	I/O
DDR1_ECC[4]	DA13	SSTL	I/O
DDR1_ECC[5]	DC13	SSTL	I/O
DDR1_ECC[6]	DA15	SSTL	I/O
DDR1_ECC[7]	DF16	SSTL	I/O
DDR1_MA[00]	DC23	SSTL	O
DDR1_MA[01]	DE23	SSTL	O
DDR1_MA[02]	DF24	SSTL	O
DDR1_MA[03]	DA23	SSTL	O
DDR1_MA[04]	DB22	SSTL	O
DDR1_MA[05]	DF22	SSTL	O
DDR1_MA[06]	DE21	SSTL	O
DDR1_MA[07]	DF20	SSTL	O
DDR1_MA[08]	DB20	SSTL	O
DDR1_MA[09]	DA19	SSTL	O
DDR1_MA[10]	DF26	SSTL	O
DDR1_MA[11]	DE19	SSTL	O
DDR1_MA[12]	DC19	SSTL	O
DDR1_MA[13]	DB30	SSTL	O
DDR1_MA[14]	DB18	SSTL	O
DDR1_MA[15]	DC17	SSTL	O
DDR1_ODT[0]	CT22	SSTL	O
DDR1_ODT[1]	DA25	SSTL	O
DDR1_ODT[2]	CY26	SSTL	O
DDR1_ODT[3]	CV26	SSTL	O
DDR1_RAS_N	DB28	SSTL	O
DDR1_WE_N	CV28	SSTL	O
DDR2_BA[0]	R17	SSTL	O
DDR2_BA[1]	L17	SSTL	O
DDR2_BA[2]	P24	SSTL	O
DDR2_CAS_N	T16	SSTL	O
DDR2_CKE[0]	AA25	SSTL	O
DDR2_CKE[1]	T26	SSTL	O
DDR2_CKE[2]	U27	SSTL	O
DDR2_CKE[3]	AD24	SSTL	O
DDR2_CLK_DN[0]	Y24	SSTL	O
DDR2_CLK_DN[1]	Y22	SSTL	O
DDR2_CLK_DN[2]	W21	SSTL	O
DDR2_CLK_DN[3]	W23	SSTL	O
DDR2_CLK_DP[0]	AB24	SSTL	O
DDR2_CLK_DP[1]	AB22	SSTL	O
DDR2_CLK_DP[2]	AA21	SSTL	O
DDR2_CLK_DP[3]	AA23	SSTL	O
DDR2_CS_N[0]	AB20	SSTL	O
DDR2_CS_N[1]	AE19	SSTL	O

Table 8-1. Land Name (Sheet 8 of 45)

Land Name	Land No.	Buffer Type	Direction
DDR2_CS_N[4]	AA19	SSTL	O
DDR2_CS_N[5]	P18	SSTL	O
DDR2_DQ[00]	T40	SSTL	I/O
DDR2_DQ[01]	V40	SSTL	I/O
DDR2_DQ[02]	P36	SSTL	I/O
DDR2_DQ[03]	T36	SSTL	I/O
DDR2_DQ[04]	R41	SSTL	I/O
DDR2_DQ[05]	U41	SSTL	I/O
DDR2_DQ[06]	R37	SSTL	I/O
DDR2_DQ[07]	U37	SSTL	I/O
DDR2_DQ[08]	AE41	SSTL	I/O
DDR2_DQ[09]	AD40	SSTL	I/O
DDR2_DQ[10]	AA37	SSTL	I/O
DDR2_DQ[11]	AC37	SSTL	I/O
DDR2_DQ[12]	AC41	SSTL	I/O
DDR2_DQ[13]	AA41	SSTL	I/O
DDR2_DQ[14]	AF38	SSTL	I/O
DDR2_DQ[15]	AE37	SSTL	I/O
DDR2_DQ[16]	U33	SSTL	I/O
DDR2_DQ[17]	R33	SSTL	I/O
DDR2_DQ[18]	W29	SSTL	I/O
DDR2_DQ[19]	U29	SSTL	I/O
DDR2_DQ[20]	T34	SSTL	I/O
DDR2_DQ[21]	P34	SSTL	I/O
DDR2_DQ[22]	V30	SSTL	I/O
DDR2_DQ[23]	T30	SSTL	I/O
DDR2_DQ[24]	AC35	SSTL	I/O
DDR2_DQ[25]	AE35	SSTL	I/O
DDR2_DQ[26]	AE33	SSTL	I/O
DDR2_DQ[27]	AF32	SSTL	I/O
DDR2_DQ[28]	AA35	SSTL	I/O
DDR2_DQ[29]	W35	SSTL	I/O
DDR2_DQ[30]	AB32	SSTL	I/O
DDR2_DQ[31]	AD32	SSTL	I/O
DDR2_DQ[32]	AC13	SSTL	I/O
DDR2_DQ[33]	AE13	SSTL	I/O
DDR2_DQ[34]	AG11	SSTL	I/O
DDR2_DQ[35]	AF10	SSTL	I/O
DDR2_DQ[36]	AD14	SSTL	I/O
DDR2_DQ[37]	AA13	SSTL	I/O
DDR2_DQ[38]	AB10	SSTL	I/O
DDR2_DQ[39]	AD10	SSTL	I/O
DDR2_DQ[40]	V6	SSTL	I/O
DDR2_DQ[41]	Y6	SSTL	I/O
DDR2_DQ[42]	AF8	SSTL	I/O

Table 8-1. Land Name (Sheet 9 of 45)

Land Name	Land No.	Buffer Type	Direction
DDR2_DQ[43]	AG7	SSTL	I/O
DDR2_DQ[44]	U7	SSTL	I/O
DDR2_DQ[45]	W7	SSTL	I/O
DDR2_DQ[46]	AD8	SSTL	I/O
DDR2_DQ[47]	AE7	SSTL	I/O
DDR2_DQ[48]	R13	SSTL	I/O
DDR2_DQ[49]	U13	SSTL	I/O
DDR2_DQ[50]	T10	SSTL	I/O
DDR2_DQ[51]	V10	SSTL	I/O
DDR2_DQ[52]	T14	SSTL	I/O
DDR2_DQ[53]	V14	SSTL	I/O
DDR2_DQ[54]	R9	SSTL	I/O
DDR2_DQ[55]	U9	SSTL	I/O
DDR2_DQ[56]	W3	SSTL	I/O
DDR2_DQ[57]	Y4	SSTL	I/O
DDR2_DQ[58]	AF4	SSTL	I/O
DDR2_DQ[59]	AE5	SSTL	I/O
DDR2_DQ[60]	U3	SSTL	I/O
DDR2_DQ[61]	V4	SSTL	I/O
DDR2_DQ[62]	AF2	SSTL	I/O
DDR2_DQ[63]	AE3	SSTL	I/O
DDR2_DQS_DN[00]	T38	SSTL	I/O
DDR2_DQS_DN[01]	AD38	SSTL	I/O
DDR2_DQS_DN[02]	W31	SSTL	I/O
DDR2_DQS_DN[03]	AA33	SSTL	I/O
DDR2_DQS_DN[04]	AC11	SSTL	I/O
DDR2_DQS_DN[05]	AB8	SSTL	I/O
DDR2_DQS_DN[06]	U11	SSTL	I/O
DDR2_DQS_DN[07]	AC3	SSTL	I/O
DDR2_DQS_DN[08]	AB28	SSTL	I/O
DDR2_DQS_DP[00]	V38	SSTL	I/O
DDR2_DQS_DP[01]	AB38	SSTL	I/O
DDR2_DQS_DP[02]	U31	SSTL	I/O
DDR2_DQS_DP[03]	AC33	SSTL	I/O
DDR2_DQS_DP[04]	AE11	SSTL	I/O
DDR2_DQS_DP[05]	AC7	SSTL	I/O
DDR2_DQS_DP[06]	W11	SSTL	I/O
DDR2_DQS_DP[07]	AB4	SSTL	I/O
DDR2_DQS_DP[08]	AC27	SSTL	I/O
DDR2_ECC[0]	AF30	SSTL	I/O
DDR2_ECC[1]	AF28	SSTL	I/O
DDR2_ECC[2]	Y26	SSTL	I/O
DDR2_ECC[3]	AB26	SSTL	I/O
DDR2_ECC[4]	AB30	SSTL	I/O
DDR2_ECC[5]	AD30	SSTL	I/O

Table 8-1. Land Name (Sheet 10 of 45)

Land Name	Land No.	Buffer Type	Direction
DDR2_ECC[6]	W27	SSTL	I/O
DDR2_ECC[7]	AA27	SSTL	I/O
DDR2_MA[00]	AB18	SSTL	O
DDR2_MA[01]	R19	SSTL	O
DDR2_MA[02]	U19	SSTL	O
DDR2_MA[03]	T20	SSTL	O
DDR2_MA[04]	P20	SSTL	O
DDR2_MA[05]	U21	SSTL	O
DDR2_MA[06]	R21	SSTL	O
DDR2_MA[07]	P22	SSTL	O
DDR2_MA[08]	T22	SSTL	O
DDR2_MA[09]	R23	SSTL	O
DDR2_MA[10]	T18	SSTL	O
DDR2_MA[11]	U23	SSTL	O
DDR2_MA[12]	T24	SSTL	O
DDR2_MA[13]	R15	SSTL	O
DDR2_MA[14]	W25	SSTL	O
DDR2_MA[15]	U25	SSTL	O
DDR2_ODT[0]	Y20	SSTL	O
DDR2_ODT[1]	W19	SSTL	O
DDR2_ODT[2]	AD18	SSTL	O
DDR2_ODT[3]	Y18	SSTL	O
DDR2_RAS_N	U17	SSTL	O
DDR2_WE_N	P16	SSTL	O
DDR23_RCOMP[0]	U15	Analog	I
DDR23_RCOMP[1]	AC15	Analog	I
DDR23_RCOMP[2]	Y14	Analog	I
DDR3_BA[0]	A17	SSTL	O
DDR3_BA[1]	E19	SSTL	O
DDR3_BA[2]	B24	SSTL	O
DDR3_CAS_N	B14	SSTL	O
DDR3_CKE[0]	K24	SSTL	O
DDR3_CKE[1]	M24	SSTL	O
DDR3_CKE[2]	J25	SSTL	O
DDR3_CKE[3]	N25	SSTL	O
DDR3_CLK_DN[0]	J23	SSTL	O
DDR3_CLK_DN[1]	J21	SSTL	O
DDR3_CLK_DN[2]	M20	SSTL	O
DDR3_CLK_DN[3]	K22	SSTL	O
DDR3_CLK_DP[0]	L23	SSTL	O
DDR3_CLK_DP[1]	L21	SSTL	O
DDR3_CLK_DP[2]	K20	SSTL	O
DDR3_CLK_DP[3]	M22	SSTL	O
DDR3_CS_N[0]	G19	SSTL	O
DDR3_CS_N[1]	J19	SSTL	O

Table 8-1. Land Name (Sheet 11 of 45)

Land Name	Land No.	Buffer Type	Direction
DDR3_CS_N[4]	K18	SSTL	O
DDR3_CS_N[5]	G17	SSTL	O
DDR3_DQ[00]	B40	SSTL	I/O
DDR3_DQ[01]	A39	SSTL	I/O
DDR3_DQ[02]	C37	SSTL	I/O
DDR3_DQ[03]	E37	SSTL	I/O
DDR3_DQ[04]	F40	SSTL	I/O
DDR3_DQ[05]	D40	SSTL	I/O
DDR3_DQ[06]	F38	SSTL	I/O
DDR3_DQ[07]	A37	SSTL	I/O
DDR3_DQ[08]	N39	SSTL	I/O
DDR3_DQ[09]	L39	SSTL	I/O
DDR3_DQ[10]	L35	SSTL	I/O
DDR3_DQ[11]	J35	SSTL	I/O
DDR3_DQ[12]	M40	SSTL	I/O
DDR3_DQ[13]	K40	SSTL	I/O
DDR3_DQ[14]	K36	SSTL	I/O
DDR3_DQ[15]	H36	SSTL	I/O
DDR3_DQ[16]	A35	SSTL	I/O
DDR3_DQ[17]	F34	SSTL	I/O
DDR3_DQ[18]	D32	SSTL	I/O
DDR3_DQ[19]	F32	SSTL	I/O
DDR3_DQ[20]	E35	SSTL	I/O
DDR3_DQ[21]	C35	SSTL	I/O
DDR3_DQ[22]	A33	SSTL	I/O
DDR3_DQ[23]	B32	SSTL	I/O
DDR3_DQ[24]	M32	SSTL	I/O
DDR3_DQ[25]	L31	SSTL	I/O
DDR3_DQ[26]	M28	SSTL	I/O
DDR3_DQ[27]	L27	SSTL	I/O
DDR3_DQ[28]	L33	SSTL	I/O
DDR3_DQ[29]	K32	SSTL	I/O
DDR3_DQ[30]	N27	SSTL	I/O
DDR3_DQ[31]	M26	SSTL	I/O
DDR3_DQ[32]	D12	SSTL	I/O
DDR3_DQ[33]	A11	SSTL	I/O
DDR3_DQ[34]	C9	SSTL	I/O
DDR3_DQ[35]	E9	SSTL	I/O
DDR3_DQ[36]	F12	SSTL	I/O
DDR3_DQ[37]	B12	SSTL	I/O
DDR3_DQ[38]	F10	SSTL	I/O
DDR3_DQ[39]	A9	SSTL	I/O
DDR3_DQ[40]	J13	SSTL	I/O
DDR3_DQ[41]	L13	SSTL	I/O
DDR3_DQ[42]	J9	SSTL	I/O

Table 8-1. Land Name (Sheet 12 of 45)

Land Name	Land No.	Buffer Type	Direction
DDR3_DQ[43]	L9	SSTL	I/O
DDR3_DQ[44]	K14	SSTL	I/O
DDR3_DQ[45]	M14	SSTL	I/O
DDR3_DQ[46]	K10	SSTL	I/O
DDR3_DQ[47]	M10	SSTL	I/O
DDR3_DQ[48]	E7	SSTL	I/O
DDR3_DQ[49]	F6	SSTL	I/O
DDR3_DQ[50]	N7	SSTL	I/O
DDR3_DQ[51]	P6	SSTL	I/O
DDR3_DQ[52]	C7	SSTL	I/O
DDR3_DQ[53]	D6	SSTL	I/O
DDR3_DQ[54]	L7	SSTL	I/O
DDR3_DQ[55]	M6	SSTL	I/O
DDR3_DQ[56]	G3	SSTL	I/O
DDR3_DQ[57]	H2	SSTL	I/O
DDR3_DQ[58]	N3	SSTL	I/O
DDR3_DQ[59]	P4	SSTL	I/O
DDR3_DQ[60]	F4	SSTL	I/O
DDR3_DQ[61]	H4	SSTL	I/O
DDR3_DQ[62]	L1	SSTL	I/O
DDR3_DQ[63]	M2	SSTL	I/O
DDR3_DQS_DN[00]	B38	SSTL	I/O
DDR3_DQS_DN[01]	L37	SSTL	I/O
DDR3_DQS_DN[02]	G33	SSTL	I/O
DDR3_DQS_DN[03]	P28	SSTL	I/O
DDR3_DQS_DN[04]	B10	SSTL	I/O
DDR3_DQS_DN[05]	L11	SSTL	I/O
DDR3_DQS_DN[06]	J7	SSTL	I/O
DDR3_DQS_DN[07]	L3	SSTL	I/O
DDR3_DQS_DN[08]	G27	SSTL	I/O
DDR3_DQS_DP[00]	D38	SSTL	I/O
DDR3_DQS_DP[01]	J37	SSTL	I/O
DDR3_DQS_DP[02]	E33	SSTL	I/O
DDR3_DQS_DP[03]	N29	SSTL	I/O
DDR3_DQS_DP[04]	D10	SSTL	I/O
DDR3_DQS_DP[05]	N11	SSTL	I/O
DDR3_DQS_DP[06]	K6	SSTL	I/O
DDR3_DQS_DP[07]	M4	SSTL	I/O
DDR3_DQS_DP[08]	E27	SSTL	I/O
DDR3_ECC[0]	G29	SSTL	I/O
DDR3_ECC[1]	J29	SSTL	I/O
DDR3_ECC[2]	E25	SSTL	I/O
DDR3_ECC[3]	C25	SSTL	I/O
DDR3_ECC[4]	F30	SSTL	I/O
DDR3_ECC[5]	H30	SSTL	I/O

Table 8-1. Land Name (Sheet 13 of 45)

Land Name	Land No.	Buffer Type	Direction
DDR3_ECC[6]	F26	SSTL	I/O
DDR3_ECC[7]	H26	SSTL	I/O
DDR3_MA[00]	A19	SSTL	O
DDR3_MA[01]	E21	SSTL	O
DDR3_MA[02]	F20	SSTL	O
DDR3_MA[03]	B20	SSTL	O
DDR3_MA[04]	D20	SSTL	O
DDR3_MA[05]	A21	SSTL	O
DDR3_MA[06]	F22	SSTL	O
DDR3_MA[07]	B22	SSTL	O
DDR3_MA[08]	D22	SSTL	O
DDR3_MA[09]	G23	SSTL	O
DDR3_MA[10]	D18	SSTL	O
DDR3_MA[11]	A23	SSTL	O
DDR3_MA[12]	E23	SSTL	O
DDR3_MA[13]	A13	SSTL	O
DDR3_MA[14]	D24	SSTL	O
DDR3_MA[15]	F24	SSTL	O
DDR3_ODT[0]	L19	SSTL	O
DDR3_ODT[1]	F18	SSTL	O
DDR3_ODT[2]	E17	SSTL	O
DDR3_ODT[3]	J17	SSTL	O
DDR3_RAS_N	B16	SSTL	O
DDR3_WE_N	A15	SSTL	O
DMI_RX_DN[0]	E47	PCIEX	I
DMI_RX_DN[1]	D48	PCIEX	I
DMI_RX_DN[2]	E49	PCIEX	I
DMI_RX_DN[3]	D50	PCIEX	I
DMI_RX_DP[0]	C47	PCIEX	I
DMI_RX_DP[1]	B48	PCIEX	I
DMI_RX_DP[2]	C49	PCIEX	I
DMI_RX_DP[3]	B50	PCIEX	I
DMI_TX_DN[0]	D42	PCIEX	O
DMI_TX_DN[1]	E43	PCIEX	O
DMI_TX_DN[2]	D44	PCIEX	O
DMI_TX_DN[3]	E45	PCIEX	O
DMI_TX_DP[0]	B42	PCIEX	O
DMI_TX_DP[1]	C43	PCIEX	O
DMI_TX_DP[2]	B44	PCIEX	O
DMI_TX_DP[3]	C45	PCIEX	O
DRAM_PWR_OK_C01	CW17	CMOS1.5v	I
DRAM_PWR_OK_C23	L15	CMOS1.5v	I
EAR_N	CH56	ODCMOS	I/O
MEM_HOT_C01_N	CB22	ODCMOS	I/O
MEM_HOT_C23_N	E13	ODCMOS	I/O

Table 8-1. Land Name (Sheet 14 of 45)

Land Name	Land No.	Buffer Type	Direction
PE_RBIAS	AH52	PCIEX3	I/O
PE_RBIAS_SENSE	AF52	PCIEX3	I
PE_VREF_CAP	AJ43	PCIEX3	I/O
PE1A_RX_DN[0]	E51	PCIEX3	I
PE1A_RX_DN[1]	F52	PCIEX3	I
PE1A_RX_DN[2]	F54	PCIEX3	I
PE1A_RX_DN[3]	G55	PCIEX3	I
PE1A_RX_DP[0]	C51	PCIEX3	I
PE1A_RX_DP[1]	D52	PCIEX3	I
PE1A_RX_DP[2]	D54	PCIEX3	I
PE1A_RX_DP[3]	E55	PCIEX3	I
PE1A_TX_DN[0]	K42	PCIEX3	O
PE1A_TX_DN[1]	L43	PCIEX3	O
PE1A_TX_DN[2]	K44	PCIEX3	O
PE1A_TX_DN[3]	L45	PCIEX3	O
PE1A_TX_DP[0]	H42	PCIEX3	O
PE1A_TX_DP[1]	J43	PCIEX3	O
PE1A_TX_DP[2]	H44	PCIEX3	O
PE1A_TX_DP[3]	J45	PCIEX3	O
PE1B_RX_DN[4]	L53	PCIEX3	I
PE1B_RX_DN[5]	M54	PCIEX3	I
PE1B_RX_DN[6]	L57	PCIEX3	I
PE1B_RX_DN[7]	M56	PCIEX3	I
PE1B_RX_DP[4]	J53	PCIEX3	I
PE1B_RX_DP[5]	K54	PCIEX3	I
PE1B_RX_DP[6]	J57	PCIEX3	I
PE1B_RX_DP[7]	K56	PCIEX3	I
PE1B_TX_DN[4]	K46	PCIEX3	O
PE1B_TX_DN[5]	L47	PCIEX3	O
PE1B_TX_DN[6]	K48	PCIEX3	O
PE1B_TX_DN[7]	L49	PCIEX3	O
PE1B_TX_DP[4]	H46	PCIEX3	O
PE1B_TX_DP[5]	J47	PCIEX3	O
PE1B_TX_DP[6]	H48	PCIEX3	O
PE1B_TX_DP[7]	J49	PCIEX3	O
PE2A_RX_DN[0]	N55	PCIEX3	I
PE2A_RX_DN[1]	V54	PCIEX3	I
PE2A_RX_DN[2]	V56	PCIEX3	I
PE2A_RX_DN[3]	W55	PCIEX3	I
PE2A_RX_DP[0]	L55	PCIEX3	I
PE2A_RX_DP[1]	T54	PCIEX3	I
PE2A_RX_DP[2]	T56	PCIEX3	I
PE2A_RX_DP[3]	U55	PCIEX3	I
PE2A_TX_DN[0]	AR49	PCIEX3	O
PE2A_TX_DN[1]	AP50	PCIEX3	O

Table 8-1. Land Name (Sheet 15 of 45)

Land Name	Land No.	Buffer Type	Direction
PE2A_TX_DN[2]	AR51	PCIEX3	O
PE2A_TX_DN[3]	AP52	PCIEX3	O
PE2A_TX_DP[0]	AN49	PCIEX3	O
PE2A_TX_DP[1]	AM50	PCIEX3	O
PE2A_TX_DP[2]	AN51	PCIEX3	O
PE2A_TX_DP[3]	AM52	PCIEX3	O
PE2B_RX_DN[4]	AD54	PCIEX3	I
PE2B_RX_DN[5]	AD56	PCIEX3	I
PE2B_RX_DN[6]	AE55	PCIEX3	I
PE2B_RX_DN[7]	AF58	PCIEX3	I
PE2B_RX_DP[4]	AB54	PCIEX3	I
PE2B_RX_DP[5]	AB56	PCIEX3	I
PE2B_RX_DP[6]	AC55	PCIEX3	I
PE2B_RX_DP[7]	AE57	PCIEX3	I
PE2B_TX_DN[4]	AJ53	PCIEX3	O
PE2B_TX_DN[5]	AK54	PCIEX3	O
PE2B_TX_DN[6]	AR53	PCIEX3	O
PE2B_TX_DN[7]	AT54	PCIEX3	O
PE2B_TX_DP[4]	AG53	PCIEX3	O
PE2B_TX_DP[5]	AH54	PCIEX3	O
PE2B_TX_DP[6]	AN53	PCIEX3	O
PE2B_TX_DP[7]	AP54	PCIEX3	O
PE2C_RX_DN[10]	AL57	PCIEX3	I
PE2C_RX_DN[11]	AU57	PCIEX3	I
PE2C_RX_DN[8]	AK56	PCIEX3	I
PE2C_RX_DN[9]	AM58	PCIEX3	I
PE2C_RX_DP[10]	AJ57	PCIEX3	I
PE2C_RX_DP[11]	AR57	PCIEX3	I
PE2C_RX_DP[8]	AH56	PCIEX3	I
PE2C_RX_DP[9]	AK58	PCIEX3	I
PE2C_TX_DN[10]	BB54	PCIEX3	O
PE2C_TX_DN[11]	BA51	PCIEX3	O
PE2C_TX_DN[8]	AY52	PCIEX3	O
PE2C_TX_DN[9]	BA53	PCIEX3	O
PE2C_TX_DP[10]	AY54	PCIEX3	O
PE2C_TX_DP[11]	AW51	PCIEX3	O
PE2C_TX_DP[8]	AV52	PCIEX3	O
PE2C_TX_DP[9]	AW53	PCIEX3	O
PE2D_RX_DN[12]	AV58	PCIEX3	I
PE2D_RX_DN[13]	AT56	PCIEX3	I
PE2D_RX_DN[14]	BA57	PCIEX3	I
PE2D_RX_DN[15]	BB56	PCIEX3	I
PE2D_RX_DP[12]	AT58	PCIEX3	I
PE2D_RX_DP[13]	AP56	PCIEX3	I
PE2D_RX_DP[14]	AY58	PCIEX3	I

Table 8-1. Land Name (Sheet 16 of 45)

Land Name	Land No.	Buffer Type	Direction
PE2D_RX_DP[15]	AY56	PCIEX3	I
PE2D_TX_DN[12]	AY50	PCIEX3	O
PE2D_TX_DN[13]	BA49	PCIEX3	O
PE2D_TX_DN[14]	AY48	PCIEX3	O
PE2D_TX_DN[15]	BA47	PCIEX3	O
PE2D_TX_DP[12]	AV50	PCIEX3	O
PE2D_TX_DP[13]	AW49	PCIEX3	O
PE2D_TX_DP[14]	AV48	PCIEX3	O
PE2D_TX_DP[15]	AW47	PCIEX3	O
PE3A_RX_DN[0]	AH44	PCIEX3	I
PE3A_RX_DN[1]	AJ45	PCIEX3	I
PE3A_RX_DN[2]	AH46	PCIEX3	I
PE3A_RX_DN[3]	AC49	PCIEX3	I
PE3A_RX_DP[0]	AF44	PCIEX3	I
PE3A_RX_DP[1]	AG45	PCIEX3	I
PE3A_RX_DP[2]	AF46	PCIEX3	I
PE3A_RX_DP[3]	AA49	PCIEX3	I
PE3A_TX_DN[0]	K50	PCIEX3	O
PE3A_TX_DN[1]	L51	PCIEX3	O
PE3A_TX_DN[2]	U47	PCIEX3	O
PE3A_TX_DN[3]	T48	PCIEX3	O
PE3A_TX_DP[0]	H50	PCIEX3	O
PE3A_TX_DP[1]	J51	PCIEX3	O
PE3A_TX_DP[2]	R47	PCIEX3	O
PE3A_TX_DP[3]	P48	PCIEX3	O
PE3B_RX_DN[4]	AB50	PCIEX3	I
PE3B_RX_DN[5]	AB52	PCIEX3	I
PE3B_RX_DN[6]	AC53	PCIEX3	I
PE3B_RX_DN[7]	AC51	PCIEX3	I
PE3B_RX_DP[4]	Y50	PCIEX3	I
PE3B_RX_DP[5]	Y52	PCIEX3	I
PE3B_RX_DP[6]	AA53	PCIEX3	I
PE3B_RX_DP[7]	AA51	PCIEX3	I
PE3B_TX_DN[4]	T52	PCIEX3	O
PE3B_TX_DN[5]	U51	PCIEX3	O
PE3B_TX_DN[6]	T50	PCIEX3	O
PE3B_TX_DN[7]	U49	PCIEX3	O
PE3B_TX_DP[4]	P52	PCIEX3	O
PE3B_TX_DP[5]	R51	PCIEX3	O
PE3B_TX_DP[6]	P50	PCIEX3	O
PE3B_TX_DP[7]	R49	PCIEX3	O
PE3C_RX_DN[10]	AH50	PCIEX3	I
PE3C_RX_DN[11]	AJ49	PCIEX3	I
PE3C_RX_DN[8]	AH48	PCIEX3	I
PE3C_RX_DN[9]	AJ51	PCIEX3	I

Table 8-1. Land Name (Sheet 17 of 45)

Land Name	Land No.	Buffer Type	Direction
PE3C_RX_DP[10]	AF50	PCIEX3	I
PE3C_RX_DP[11]	AG49	PCIEX3	I
PE3C_RX_DP[8]	AF48	PCIEX3	I
PE3C_RX_DP[9]	AG51	PCIEX3	I
PE3C_TX_DN[10]	U45	PCIEX3	O
PE3C_TX_DN[11]	AB46	PCIEX3	O
PE3C_TX_DN[8]	T46	PCIEX3	O
PE3C_TX_DN[9]	AC47	PCIEX3	O
PE3C_TX_DP[10]	R45	PCIEX3	O
PE3C_TX_DP[11]	Y46	PCIEX3	O
PE3C_TX_DP[8]	P46	PCIEX3	O
PE3C_TX_DP[9]	AA47	PCIEX3	O
PE3D_RX_DN[12]	AJ47	PCIEX3	I
PE3D_RX_DN[13]	AR47	PCIEX3	I
PE3D_RX_DN[14]	AP46	PCIEX3	I
PE3D_RX_DN[15]	AR45	PCIEX3	I
PE3D_RX_DP[12]	AG47	PCIEX3	I
PE3D_RX_DP[13]	AN47	PCIEX3	I
PE3D_RX_DP[14]	AM46	PCIEX3	I
PE3D_RX_DP[15]	AN45	PCIEX3	I
PE3D_TX_DN[12]	AC45	PCIEX3	O
PE3D_TX_DN[13]	AB44	PCIEX3	O
PE3D_TX_DN[14]	AA43	PCIEX3	O
PE3D_TX_DN[15]	P44	PCIEX3	O
PE3D_TX_DP[12]	AA45	PCIEX3	O
PE3D_TX_DP[13]	Y44	PCIEX3	O
PE3D_TX_DP[14]	AC43	PCIEX3	O
PE3D_TX_DP[15]	T44	PCIEX3	O
PECI	BJ47	PECI	I/O
PMSYNC	K52	CMOS	I
PRDY_N	R53	CMOS	O
PREQ_N	U53	CMOS	I/O
PROC_SEL_N	AH42		O
PROCHOT_N	BD52	ODCMOS	I/O
PWRGOOD	BJ53	CMOS	I
RESET_N	CK44	CMOS	I
RSVD	AK52		
RSVD	A53		
RSVD	AA15		
RSVD	AA17		
RSVD	AA7		
RSVD	AB12		
RSVD	AB16		
RSVD	AB34		
RSVD	AB40		

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Land Name	Land No.	Buffer Type	Direction
RSVD	AB48		
RSVD	AC29		
RSVD	AC39		
RSVD	AC5		
RSVD	AD12		
RSVD	AD16		
RSVD	AD20		
RSVD	AD22		
RSVD	AD28		
RSVD	AD4		
RSVD	AE21		
RSVD	AE23		
RSVD	AE25		
RSVD	AL47		
RSVD	AL55		
RSVD	AM44		
RSVD	AP48		
RSVD	AR55		
RSVD	AU55		
RSVD	AV46		
RSVD	AY46		
RSVD	B18		
RSVD	B34		
RSVD	B46		
RSVD	BC47		
RSVD	BC51		
RSVD	BD44		
RSVD	BD46		
RSVD	BD50		
RSVD	BD58		
RSVD	BE43		
RSVD	BE45		
RSVD	BE47		
RSVD	BE53		
RSVD	BE55		
RSVD	BE57		
RSVD	BF46		
RSVD	BF50		
RSVD	BF52		
RSVD	BF54		
RSVD	BF56		
RSVD	BF58		
RSVD	BG43		
RSVD	BG45		
RSVD	BG49		

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Land Name	Land No.	Buffer Type	Direction
RSVD	BG51		
RSVD	BG53		
RSVD	BG55		
RSVD	BG57		
RSVD	BH44		
RSVD	BH46		
RSVD	BH50		
RSVD	BH52		
RSVD	BH54		
RSVD	BH56		
RSVD	BJ43		
RSVD	BJ45		
RSVD	BJ49		
RSVD	BJ51		
RSVD	BK44		
RSVD	BK58		
RSVD	BL43		
RSVD	BL45		
RSVD	BL53		
RSVD	BL55		
RSVD	BL57		
RSVD	BM44		
RSVD	BM46		
RSVD	BM48		
RSVD	BM50		
RSVD	BM52		
RSVD	BM54		
RSVD	BM56		
RSVD	BM58		
RSVD	BN47		
RSVD	BN49		
RSVD	BN51		
RSVD	BN53		
RSVD	BN55		
RSVD	BN57		
RSVD	BP44		
RSVD	BP46		
RSVD	BP48		
RSVD	BP50		
RSVD	BP52		
RSVD	BP54		
RSVD	BP56		
RSVD	BR43		
RSVD	BR47		
RSVD	BR49		

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Land Name	Land No.	Buffer Type	Direction
RSVD	BR51		
RSVD	BT44		
RSVD	BT58		
RSVD	BU43		
RSVD	BU53		
RSVD	BU55		
RSVD	BU57		
RSVD	BV46		
RSVD	BV48		
RSVD	BV50		
RSVD	BV52		
RSVD	BV54		
RSVD	BV56		
RSVD	BV58		
RSVD	BW45		
RSVD	BW47		
RSVD	BW49		
RSVD	BW51		
RSVD	BW53		
RSVD	BW55		
RSVD	BW57		
RSVD	BY46		
RSVD	BY48		
RSVD	BY50		
RSVD	BY52		
RSVD	BY54		
RSVD	BY56		
RSVD	C53		
RSVD	CA45		
RSVD	CA47		
RSVD	CA49		
RSVD	CA51		
RSVD	CB10		
RSVD	CB24		
RSVD	CB26		
RSVD	CB28		
RSVD	CB32		
RSVD	CB54		
RSVD	CC11		
RSVD	CC21		
RSVD	CC23		
RSVD	CC25		
RSVD	CC27		
RSVD	CC39		
RSVD	CC5		

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Land Name	Land No.	Buffer Type	Direction
RSVD	CC55		
RSVD	CD16		
RSVD	CD32		
RSVD	CD4		
RSVD	CD44		
RSVD	CD46		
RSVD	CD48		
RSVD	CD50		
RSVD	CD52		
RSVD	CD54		
RSVD	CD56		
RSVD	CE19		
RSVD	CE39		
RSVD	CE43		
RSVD	CE45		
RSVD	CE47		
RSVD	CE49		
RSVD	CE51		
RSVD	CE55		
RSVD	CE7		
RSVD	CF16		
RSVD	CF20		
RSVD	CF44		
RSVD	CF46		
RSVD	CF48		
RSVD	CF50		
RSVD	CF52		
RSVD	CF54		
RSVD	CF56		
RSVD	CF8		
RSVD	CG11		
RSVD	CG45		
RSVD	CG47		
RSVD	CG49		
RSVD	CG51		
RSVD	CH32		
RSVD	CJ13		
RSVD	CJ39		
RSVD	CJ53		
RSVD	CJ55		
RSVD	CK28		
RSVD	CK32		
RSVD	CK46		
RSVD	CK48		
RSVD	CK50		

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Land Name	Land No.	Buffer Type	Direction
RSVD	CK52		
RSVD	CK54		
RSVD	CK56		
RSVD	CL13		
RSVD	CL27		
RSVD	CL39		
RSVD	CL45		
RSVD	CL47		
RSVD	CL49		
RSVD	CL51		
RSVD	CL53		
RSVD	CL55		
RSVD	CM26		
RSVD	CM46		
RSVD	CM48		
RSVD	CM50		
RSVD	CM52		
RSVD	CM54		
RSVD	CM56		
RSVD	CN45		
RSVD	CN47		
RSVD	CN49		
RSVD	CN51		
RSVD	CP14		
RSVD	CP38		
RSVD	CP54		
RSVD	CP58		
RSVD	CP8		
RSVD	CR1		
RSVD	CR19		
RSVD	CR21		
RSVD	CR23		
RSVD	CR27		
RSVD	CR31		
RSVD	CR53		
RSVD	CR55		
RSVD	CR57		
RSVD	CT14		
RSVD	CT18		
RSVD	CT2		
RSVD	CT26		
RSVD	CT38		
RSVD	CT44		
RSVD	CT46		
RSVD	CT48		

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Land Name	Land No.	Buffer Type	Direction
RSVD	CT50		
RSVD	CT52		
RSVD	CT56		
RSVD	CT58		
RSVD	CT8		
RSVD	CU21		
RSVD	CU27		
RSVD	CU31		
RSVD	CU43		
RSVD	CU45		
RSVD	CU47		
RSVD	CU49		
RSVD	CU53		
RSVD	CU55		
RSVD	CU57		
RSVD	CV44		
RSVD	CV46		
RSVD	CV48		
RSVD	CV50		
RSVD	CV52		
RSVD	CV56		
RSVD	CW43		
RSVD	CW45		
RSVD	CW47		
RSVD	CW49		
RSVD	CY14		
RSVD	CY28		
RSVD	CY38		
RSVD	CY46		
RSVD	CY48		
RSVD	CY54		
RSVD	CY56		
RSVD	CY58		
RSVD	D14		
RSVD	D16		
RSVD	D34		
RSVD	D46		
RSVD	D56		
RSVD	DA27		
RSVD	DA29		
RSVD	DA53		
RSVD	DA55		
RSVD	DA57		
RSVD	DB14		
RSVD	DB38		

Table 8-1. Land Name (Sheet 24 of 45)

Land Name	Land No.	Buffer Type	Direction
RSVD	DB42		
RSVD	DB44		
RSVD	DB46		
RSVD	DB48		
RSVD	DB50		
RSVD	DB52		
RSVD	DB54		
RSVD	DB56		
RSVD	DB8		
RSVD	DC33		
RSVD	DC43		
RSVD	DC45		
RSVD	DC47		
RSVD	DC49		
RSVD	DC51		
RSVD	DC53		
RSVD	DC55		
RSVD	DD42		
RSVD	DD44		
RSVD	DD46		
RSVD	DD48		
RSVD	DD50		
RSVD	DD52		
RSVD	DD54		
RSVD	DD8		
RSVD	DE25		
RSVD	DE33		
RSVD	DE43		
RSVD	DE45		
RSVD	DE47		
RSVD	DE49		
RSVD	DE51		
RSVD	DE55		
RSVD	E11		
RSVD	E15		
RSVD	E39		
RSVD	E53		
RSVD	E57		
RSVD	F14		
RSVD	F16		
RSVD	F28		
RSVD	F46		
RSVD	F56		
RSVD	F58		
RSVD	G11		

Table 8-1. Land Name (Sheet 25 of 45)

Land Name	Land No.	Buffer Type	Direction
RSVD	G15		
RSVD	G21		
RSVD	G39		
RSVD	G7		
RSVD	H28		
RSVD	H56		
RSVD	H58		
RSVD	H6		
RSVD	J15		
RSVD	J3		
RSVD	K12		
RSVD	K16		
RSVD	K38		
RSVD	K4		
RSVD	K58		
RSVD	M12		
RSVD	M16		
RSVD	M18		
RSVD	M30		
RSVD	M38		
RSVD	M48		
RSVD	N31		
RSVD	R25		
RSVD	R27		
RSVD	T12		
RSVD	T32		
RSVD	U39		
RSVD	V12		
RSVD	V32		
RSVD	V52		
RSVD	W15		
RSVD	W17		
RSVD	W39		
RSVD	Y16		
RSVD	Y34		
RSVD	Y48		
RSVD	Y8		
SKTOCC_N	BU49		O
SVIDALERT_N	CR43	CMOS	I
SVIDCLK	CB44	ODCMOS	O
SVIDDATA	BR45	ODCMOS	I/O
TCK	BY44	CMOS	I
TDI	BW43	CMOS	I
TDO	CA43	ODCMOS	O
TEST0	DB4		O

Table 8-1. Land Name (Sheet 26 of 45)

Land Name	Land No.	Buffer Type	Direction
TEST1	CW1		O
TEST2	F2		O
TEST3	D4		O
TEST4	BA55		I
TESTHI_AT50	AT50	CMOS	I
TESTHI_BF48	BF48	Open Drain	I/O
TESTHI_BH48	BH48	Open Drain	I/O
THERMTRIP_N	BL47	ODCMOS	O
TMS	BV44	CMOS	I
TRST_N	CT54	CMOS	I
VCC	AG19	PWR	
VCC	AG25	PWR	
VCC	AG27	PWR	
VCC	AG29	PWR	
VCC	AG31	PWR	
VCC	AG33	PWR	
VCC	AG35	PWR	
VCC	AG37	PWR	
VCC	AG39	PWR	
VCC	AG41	PWR	
VCC	AL1	PWR	
VCC	AL11	PWR	
VCC	AL13	PWR	
VCC	AL15	PWR	
VCC	AL17	PWR	
VCC	AL3	PWR	
VCC	AL5	PWR	
VCC	AL7	PWR	
VCC	AL9	PWR	
VCC	AM10	PWR	
VCC	AM12	PWR	
VCC	AM14	PWR	
VCC	AM16	PWR	
VCC	AM2	PWR	
VCC	AM4	PWR	
VCC	AM6	PWR	
VCC	AM8	PWR	
VCC	AN1	PWR	
VCC	AN11	PWR	
VCC	AN13	PWR	
VCC	AN15	PWR	
VCC	AN17	PWR	
VCC	AN3	PWR	
VCC	AN5	PWR	
VCC	AN7	PWR	

Table 8-1. Land Name (Sheet 27 of 45)

Land Name	Land No.	Buffer Type	Direction
VCC	AN9	PWR	
VCC	AP10	PWR	
VCC	AP12	PWR	
VCC	AP14	PWR	
VCC	AP16	PWR	
VCC	AP2	PWR	
VCC	AP4	PWR	
VCC	AP6	PWR	
VCC	AP8	PWR	
VCC	AU1	PWR	
VCC	AU11	PWR	
VCC	AU13	PWR	
VCC	AU15	PWR	
VCC	AU17	PWR	
VCC	AU3	PWR	
VCC	AU5	PWR	
VCC	AU7	PWR	
VCC	AU9	PWR	
VCC	AV10	PWR	
VCC	AV12	PWR	
VCC	AV14	PWR	
VCC	AV16	PWR	
VCC	AV2	PWR	
VCC	AV4	PWR	
VCC	AV6	PWR	
VCC	AV8	PWR	
VCC	AW1	PWR	
VCC	AW11	PWR	
VCC	AW13	PWR	
VCC	AW15	PWR	
VCC	AW17	PWR	
VCC	AW3	PWR	
VCC	AW5	PWR	
VCC	AW7	PWR	
VCC	AW9	PWR	
VCC	AY10	PWR	
VCC	AY12	PWR	
VCC	AY14	PWR	
VCC	AY16	PWR	
VCC	AY2	PWR	
VCC	AY4	PWR	
VCC	AY6	PWR	
VCC	AY8	PWR	
VCC	BA1	PWR	
VCC	BA11	PWR	

Table 8-1. Land Name (Sheet 28 of 45)

Land Name	Land No.	Buffer Type	Direction
VCC	BA13	PWR	
VCC	BA15	PWR	
VCC	BA17	PWR	
VCC	BA3	PWR	
VCC	BA5	PWR	
VCC	BA7	PWR	
VCC	BA9	PWR	
VCC	BB10	PWR	
VCC	BB12	PWR	
VCC	BB14	PWR	
VCC	BB16	PWR	
VCC	BB2	PWR	
VCC	BB4	PWR	
VCC	BB6	PWR	
VCC	BB8	PWR	
VCC	BE1	PWR	
VCC	BE11	PWR	
VCC	BE13	PWR	
VCC	BE15	PWR	
VCC	BE17	PWR	
VCC	BE3	PWR	
VCC	BE5	PWR	
VCC	BE7	PWR	
VCC	BE9	PWR	
VCC	BF10	PWR	
VCC	BF12	PWR	
VCC	BF14	PWR	
VCC	BF16	PWR	
VCC	BF2	PWR	
VCC	BF4	PWR	
VCC	BF6	PWR	
VCC	BF8	PWR	
VCC	BG1	PWR	
VCC	BG11	PWR	
VCC	BG13	PWR	
VCC	BG15	PWR	
VCC	BG17	PWR	
VCC	BG3	PWR	
VCC	BG5	PWR	
VCC	BG7	PWR	
VCC	BG9	PWR	
VCC	BH10	PWR	
VCC	BH12	PWR	
VCC	BH14	PWR	
VCC	BH16	PWR	

Table 8-1. Land Name (Sheet 29 of 45)

Land Name	Land No.	Buffer Type	Direction
VCC	BH2	PWR	
VCC	BH4	PWR	
VCC	BH6	PWR	
VCC	BH8	PWR	
VCC	BJ1	PWR	
VCC	BJ11	PWR	
VCC	BJ13	PWR	
VCC	BJ15	PWR	
VCC	BJ17	PWR	
VCC	BJ3	PWR	
VCC	BJ5	PWR	
VCC	BJ7	PWR	
VCC	BJ9	PWR	
VCC	BK10	PWR	
VCC	BK12	PWR	
VCC	BK14	PWR	
VCC	BK16	PWR	
VCC	BK2	PWR	
VCC	BK4	PWR	
VCC	BK6	PWR	
VCC	BK8	PWR	
VCC	BN1	PWR	
VCC	BN11	PWR	
VCC	BN13	PWR	
VCC	BN15	PWR	
VCC	BN17	PWR	
VCC	BN3	PWR	
VCC	BN5	PWR	
VCC	BN7	PWR	
VCC	BN9	PWR	
VCC	BP10	PWR	
VCC	BP12	PWR	
VCC	BP14	PWR	
VCC	BP16	PWR	
VCC	BP2	PWR	
VCC	BP4	PWR	
VCC	BP6	PWR	
VCC	BP8	PWR	
VCC	BR1	PWR	
VCC	BR11	PWR	
VCC	BR13	PWR	
VCC	BR15	PWR	
VCC	BR17	PWR	
VCC	BR3	PWR	
VCC	BR5	PWR	

Table 8-1. Land Name (Sheet 30 of 45)

Land Name	Land No.	Buffer Type	Direction
VCC	BR7	PWR	
VCC	BR9	PWR	
VCC	BT10	PWR	
VCC	BT12	PWR	
VCC	BT14	PWR	
VCC	BT16	PWR	
VCC	BT2	PWR	
VCC	BT4	PWR	
VCC	BT6	PWR	
VCC	BT8	PWR	
VCC	BU1	PWR	
VCC	BU11	PWR	
VCC	BU13	PWR	
VCC	BU15	PWR	
VCC	BU17	PWR	
VCC	BU3	PWR	
VCC	BU5	PWR	
VCC	BU7	PWR	
VCC	BU9	PWR	
VCC	BV10	PWR	
VCC	BV12	PWR	
VCC	BV14	PWR	
VCC	BV16	PWR	
VCC	BV2	PWR	
VCC	BV4	PWR	
VCC	BV6	PWR	
VCC	BV8	PWR	
VCC	BY18	PWR	
VCC	BY26	PWR	
VCC	BY28	PWR	
VCC	BY30	PWR	
VCC	BY32	PWR	
VCC	BY34	PWR	
VCC	BY36	PWR	
VCC	BY38	PWR	
VCC	BY40	PWR	
VCC	CA25	PWR	
VCC	CA29	PWR	
VCC_SENSE	BW3		O
VCCD_01	CD20	PWR	
VCCD_01	CD22	PWR	
VCCD_01	CD24	PWR	
VCCD_01	CD26	PWR	
VCCD_01	CD28	PWR	
VCCD_01	CJ19	PWR	

Table 8-1. Land Name (Sheet 31 of 45)

Land Name	Land No.	Buffer Type	Direction
VCCD_01	CJ21	PWR	
VCCD_01	CJ23	PWR	
VCCD_01	CJ25	PWR	
VCCD_01	CJ27	PWR	
VCCD_01	CP20	PWR	
VCCD_01	CP22	PWR	
VCCD_01	CP24	PWR	
VCCD_01	CP26	PWR	
VCCD_01	CP28	PWR	
VCCD_01	CW19	PWR	
VCCD_01	CW21	PWR	
VCCD_01	CW23	PWR	
VCCD_01	CW25	PWR	
VCCD_01	CW27	PWR	
VCCD_01	DD18	PWR	
VCCD_01	DD20	PWR	
VCCD_01	DD22	PWR	
VCCD_01	DD24	PWR	
VCCD_01	DD26	PWR	
VCCD_23	AC17	PWR	
VCCD_23	AC19	PWR	
VCCD_23	AC21	PWR	
VCCD_23	AC23	PWR	
VCCD_23	AC25	PWR	
VCCD_23	C15	PWR	
VCCD_23	C17	PWR	
VCCD_23	C19	PWR	
VCCD_23	C21	PWR	
VCCD_23	C23	PWR	
VCCD_23	G13	PWR	
VCCD_23	H16	PWR	
VCCD_23	H18	PWR	
VCCD_23	H20	PWR	
VCCD_23	H22	PWR	
VCCD_23	H24	PWR	
VCCD_23	N15	PWR	
VCCD_23	N17	PWR	
VCCD_23	N19	PWR	
VCCD_23	N21	PWR	
VCCD_23	N23	PWR	
VCCD_23	V16	PWR	
VCCD_23	V18	PWR	
VCCD_23	V20	PWR	
VCCD_23	V22	PWR	
VCCD_23	V24	PWR	

Table 8-1. Land Name (Sheet 32 of 45)

Land Name	Land No.	Buffer Type	Direction
VCCPLL	BY14	PWR	
VCCPLL	CA13	PWR	
VCCPLL	CA15	PWR	
VSA	AE15	PWR	
VSA	AE17	PWR	
VSA	AF18	PWR	
VSA	AG15	PWR	
VSA	AG17	PWR	
VSA	AH10	PWR	
VSA	AH12	PWR	
VSA	AH14	PWR	
VSA	AH16	PWR	
VSA	AH2	PWR	
VSA	AH4	PWR	
VSA	AH6	PWR	
VSA	AH8	PWR	
VSA	AJ1	PWR	
VSA	AJ11	PWR	
VSA	AJ13	PWR	
VSA	AJ3	PWR	
VSA	AJ5	PWR	
VSA	AJ7	PWR	
VSA	AJ9	PWR	
VSA	B54	PWR	
VSA	G43	PWR	
VSA	G49	PWR	
VSA	N45	PWR	
VSA	N51	PWR	
VSA_SENSE	AG13		O
VSS	A41	GND	
VSS	A43	GND	
VSS	A45	GND	
VSS	A47	GND	
VSS	A49	GND	
VSS	A5	GND	
VSS	A51	GND	
VSS	A7	GND	
VSS	AA11	GND	
VSS	AA29	GND	
VSS	AA3	GND	
VSS	AA31	GND	
VSS	AA39	GND	
VSS	AA5	GND	
VSS	AA55	GND	
VSS	AA9	GND	

Table 8-1. Land Name (Sheet 33 of 45)

Land Name	Land No.	Buffer Type	Direction
VSS	AB14	GND	
VSS	AB36	GND	
VSS	AB42	GND	
VSS	AB6	GND	
VSS	AC31	GND	
VSS	AC9	GND	
VSS	AD26	GND	
VSS	AD34	GND	
VSS	AD36	GND	
VSS	AD42	GND	
VSS	AD44	GND	
VSS	AD46	GND	
VSS	AD48	GND	
VSS	AD50	GND	
VSS	AD52	GND	
VSS	AD6	GND	
VSS	AE29	GND	
VSS	AE31	GND	
VSS	AE39	GND	
VSS	AE43	GND	
VSS	AE47	GND	
VSS	AE49	GND	
VSS	AE51	GND	
VSS	AE9	GND	
VSS	AF12	GND	
VSS	AF16	GND	
VSS	AF20	GND	
VSS	AF26	GND	
VSS	AF34	GND	
VSS	AF36	GND	
VSS	AF40	GND	
VSS	AF42	GND	
VSS	AF54	GND	
VSS	AF56	GND	
VSS	AF6	GND	
VSS	AG1	GND	
VSS	AG3	GND	
VSS	AG43	GND	
VSS	AG5	GND	
VSS	AG55	GND	
VSS	AG57	GND	
VSS	AG9	GND	
VSS	AH58	GND	
VSS	AJ15	GND	
VSS	AJ17	GND	

Table 8-1. Land Name (Sheet 34 of 45)

Land Name	Land No.	Buffer Type	Direction
VSS	AK10	GND	
VSS	AK12	GND	
VSS	AK14	GND	
VSS	AK16	GND	
VSS	AK2	GND	
VSS	AK4	GND	
VSS	AK42	GND	
VSS	AK44	GND	
VSS	AK46	GND	
VSS	AK48	GND	
VSS	AK50	GND	
VSS	AK6	GND	
VSS	AK8	GND	
VSS	AL43	GND	
VSS	AL45	GND	
VSS	AL49	GND	
VSS	AL51	GND	
VSS	AL53	GND	
VSS	AM56	GND	
VSS	AN55	GND	
VSS	AN57	GND	
VSS	AP42	GND	
VSS	AP44	GND	
VSS	AP58	GND	
VSS	AR1	GND	
VSS	AR11	GND	
VSS	AR13	GND	
VSS	AR15	GND	
VSS	AR17	GND	
VSS	AR3	GND	
VSS	AR5	GND	
VSS	AR7	GND	
VSS	AR9	GND	
VSS	AT10	GND	
VSS	AT12	GND	
VSS	AT14	GND	
VSS	AT16	GND	
VSS	AT2	GND	
VSS	AT4	GND	
VSS	AT46	GND	
VSS	AT52	GND	
VSS	AT6	GND	
VSS	AT8	GND	
VSS	AU45	GND	
VSS	AU47	GND	

Table 8-1. Land Name (Sheet 35 of 45)

Land Name	Land No.	Buffer Type	Direction
VSS	AU49	GND	
VSS	AU51	GND	
VSS	AV42	GND	
VSS	AV54	GND	
VSS	AV56	GND	
VSS	AW55	GND	
VSS	AW57	GND	
VSS	B36	GND	
VSS	B52	GND	
VSS	B6	GND	
VSS	B8	GND	
VSS	BB42	GND	
VSS	BB46	GND	
VSS	BB48	GND	
VSS	BB50	GND	
VSS	BB52	GND	
VSS	BB58	GND	
VSS	BC1	GND	
VSS	BC11	GND	
VSS	BC13	GND	
VSS	BC15	GND	
VSS	BC17	GND	
VSS	BC3	GND	
VSS	BC43	GND	
VSS	BC45	GND	
VSS	BC49	GND	
VSS	BC5	GND	
VSS	BC53	GND	
VSS	BC55	GND	
VSS	BC57	GND	
VSS	BC7	GND	
VSS	BC9	GND	
VSS	BD10	GND	
VSS	BD12	GND	
VSS	BD14	GND	
VSS	BD16	GND	
VSS	BD2	GND	
VSS	BD4	GND	
VSS	BD54	GND	
VSS	BD56	GND	
VSS	BD6	GND	
VSS	BD8	GND	
VSS	BE49	GND	
VSS	BE51	GND	
VSS	BF42	GND	

Table 8-1. Land Name (Sheet 36 of 45)

Land Name	Land No.	Buffer Type	Direction
VSS	BF44	GND	
VSS	BG47	GND	
VSS	BH58	GND	
VSS	BJ55	GND	
VSS	BJ57	GND	
VSS	BK42	GND	
VSS	BK46	GND	
VSS	BK48	GND	
VSS	BK50	GND	
VSS	BK52	GND	
VSS	BK54	GND	
VSS	BL1	GND	
VSS	BL11	GND	
VSS	BL13	GND	
VSS	BL15	GND	
VSS	BL17	GND	
VSS	BL3	GND	
VSS	BL49	GND	
VSS	BL5	GND	
VSS	BL7	GND	
VSS	BL9	GND	
VSS	BM10	GND	
VSS	BM12	GND	
VSS	BM14	GND	
VSS	BM16	GND	
VSS	BM2	GND	
VSS	BM4	GND	
VSS	BM6	GND	
VSS	BM8	GND	
VSS	BN43	GND	
VSS	BN45	GND	
VSS	BP58	GND	
VSS	BR53	GND	
VSS	BR57	GND	
VSS	BT46	GND	
VSS	BT48	GND	
VSS	BT50	GND	
VSS	BT52	GND	
VSS	BT54	GND	
VSS	BT56	GND	
VSS	BU45	GND	
VSS	BU51	GND	
VSS	BW1	GND	
VSS	BW11	GND	
VSS	BW13	GND	

Table 8-1. Land Name (Sheet 37 of 45)

Land Name	Land No.	Buffer Type	Direction
VSS	BW15	GND	
VSS	BW17	GND	
VSS	BW5	GND	
VSS	BW7	GND	
VSS	BY24	GND	
VSS	BY4	GND	
VSS	BY42	GND	
VSS	BY58	GND	
VSS	BY8	GND	
VSS	C11	GND	
VSS	C13	GND	
VSS	C3	GND	
VSS	C33	GND	
VSS	C39	GND	
VSS	C41	GND	
VSS	C5	GND	
VSS	C55	GND	
VSS	CA11	GND	
VSS	CA19	GND	
VSS	CA27	GND	
VSS	CA31	GND	
VSS	CA33	GND	
VSS	CA35	GND	
VSS	CA37	GND	
VSS	CA39	GND	
VSS	CA41	GND	
VSS	CA5	GND	
VSS	CA55	GND	
VSS	CA57	GND	
VSS	CB16	GND	
VSS	CB36	GND	
VSS	CB46	GND	
VSS	CB48	GND	
VSS	CB50	GND	
VSS	CB52	GND	
VSS	CB56	GND	
VSS	CB6	GND	
VSS	CB8	GND	
VSS	CC13	GND	
VSS	CC29	GND	
VSS	CC3	GND	
VSS	CC43	GND	
VSS	CC47	GND	
VSS	CC49	GND	
VSS	CC9	GND	

Table 8-1. Land Name (Sheet 38 of 45)

Land Name	Land No.	Buffer Type	Direction
VSS	CD18	GND	
VSS	CD36	GND	
VSS	CD6	GND	
VSS	CE13	GND	
VSS	CE5	GND	
VSS	CE9	GND	
VSS	CF12	GND	
VSS	CF14	GND	
VSS	CF30	GND	
VSS	CF32	GND	
VSS	CF34	GND	
VSS	CF36	GND	
VSS	CF38	GND	
VSS	CF40	GND	
VSS	CF42	GND	
VSS	CF6	GND	
VSS	CG15	GND	
VSS	CG31	GND	
VSS	CG33	GND	
VSS	CG35	GND	
VSS	CG37	GND	
VSS	CG39	GND	
VSS	CG41	GND	
VSS	CG43	GND	
VSS	CG53	GND	
VSS	CG9	GND	
VSS	CH12	GND	
VSS	CH16	GND	
VSS	CH36	GND	
VSS	CH44	GND	
VSS	CH46	GND	
VSS	CH48	GND	
VSS	CH50	GND	
VSS	CH52	GND	
VSS	CH54	GND	
VSS	CH6	GND	
VSS	CJ11	GND	
VSS	CJ17	GND	
VSS	CJ29	GND	
VSS	CJ3	GND	
VSS	CJ43	GND	
VSS	CJ45	GND	
VSS	CJ47	GND	
VSS	CJ51	GND	
VSS	CJ9	GND	

Table 8-1. Land Name (Sheet 39 of 45)

Land Name	Land No.	Buffer Type	Direction
VSS	CK10	GND	
VSS	CK36	GND	
VSS	CK4	GND	
VSS	CK6	GND	
VSS	CL17	GND	
VSS	CL43	GND	
VSS	CL5	GND	
VSS	CM10	GND	
VSS	CM14	GND	
VSS	CM30	GND	
VSS	CM32	GND	
VSS	CM34	GND	
VSS	CM36	GND	
VSS	CM38	GND	
VSS	CM40	GND	
VSS	CM42	GND	
VSS	CM6	GND	
VSS	CM8	GND	
VSS	CN11	GND	
VSS	CN13	GND	
VSS	CN15	GND	
VSS	CN17	GND	
VSS	CN3	GND	
VSS	CN31	GND	
VSS	CN33	GND	
VSS	CN35	GND	
VSS	CN37	GND	
VSS	CN39	GND	
VSS	CN5	GND	
VSS	CN53	GND	
VSS	CN55	GND	
VSS	CN57	GND	
VSS	CN7	GND	
VSS	CN9	GND	
VSS	CP12	GND	
VSS	CP16	GND	
VSS	CP36	GND	
VSS	CP40	GND	
VSS	CP42	GND	
VSS	CP44	GND	
VSS	CP46	GND	
VSS	CP48	GND	
VSS	CP50	GND	
VSS	CP52	GND	
VSS	CP56	GND	

Table 8-1. Land Name (Sheet 40 of 45)

Land Name	Land No.	Buffer Type	Direction
VSS	CR11	GND	
VSS	CR35	GND	
VSS	CR47	GND	
VSS	CR49	GND	
VSS	CR5	GND	
VSS	CR9	GND	
VSS	CT28	GND	
VSS	CT42	GND	
VSS	CU1	GND	
VSS	CU11	GND	
VSS	CU3	GND	
VSS	CU35	GND	
VSS	CU5	GND	
VSS	CV14	GND	
VSS	CV18	GND	
VSS	CV30	GND	
VSS	CV32	GND	
VSS	CV34	GND	
VSS	CV38	GND	
VSS	CV42	GND	
VSS	CV54	GND	
VSS	CV58	GND	
VSS	CV6	GND	
VSS	CW11	GND	
VSS	CW13	GND	
VSS	CW15	GND	
VSS	CW29	GND	
VSS	CW31	GND	
VSS	CW33	GND	
VSS	CW35	GND	
VSS	CW37	GND	
VSS	CW39	GND	
VSS	CW5	GND	
VSS	CW51	GND	
VSS	CW53	GND	
VSS	CW55	GND	
VSS	CW57	GND	
VSS	CW7	GND	
VSS	CY10	GND	
VSS	CY12	GND	
VSS	CY16	GND	
VSS	CY2	GND	
VSS	CY36	GND	
VSS	CY40	GND	
VSS	CY44	GND	

Table 8-1. Land Name (Sheet 41 of 45)

Land Name	Land No.	Buffer Type	Direction
VSS	CY50	GND	
VSS	CY52	GND	
VSS	CY8	GND	
VSS	D2	GND	
VSS	D26	GND	
VSS	D36	GND	
VSS	D8	GND	
VSS	DA11	GND	
VSS	DA3	GND	
VSS	DA41	GND	
VSS	DA43	GND	
VSS	DA45	GND	
VSS	DA47	GND	
VSS	DA5	GND	
VSS	DA51	GND	
VSS	DA9	GND	
VSS	DB12	GND	
VSS	DB2	GND	
VSS	DB32	GND	
VSS	DB36	GND	
VSS	DB58	GND	
VSS	DC3	GND	
VSS	DC41	GND	
VSS	DC5	GND	
VSS	DD10	GND	
VSS	DD12	GND	
VSS	DD14	GND	
VSS	DD34	GND	
VSS	DD36	GND	
VSS	DD38	GND	
VSS	DD6	GND	
VSS	DE17	GND	
VSS	DE41	GND	
VSS	DE53	GND	
VSS	DE7	GND	
VSS	DF12	GND	
VSS	DF36	GND	
VSS	DF42	GND	
VSS	DF44	GND	
VSS	DF46	GND	
VSS	DF48	GND	
VSS	DF50	GND	
VSS	DF52	GND	
VSS	DF8	GND	
VSS	E1	GND	

Table 8-1. Land Name (Sheet 42 of 45)

Land Name	Land No.	Buffer Type	Direction
VSS	E29	GND	
VSS	E3	GND	
VSS	E31	GND	
VSS	E41	GND	
VSS	E5	GND	
VSS	F36	GND	
VSS	F42	GND	
VSS	F44	GND	
VSS	F48	GND	
VSS	F50	GND	
VSS	F8	GND	
VSS	G1	GND	
VSS	G25	GND	
VSS	G31	GND	
VSS	G35	GND	
VSS	G37	GND	
VSS	G41	GND	
VSS	G45	GND	
VSS	G47	GND	
VSS	G5	GND	
VSS	G51	GND	
VSS	G53	GND	
VSS	G57	GND	
VSS	G9	GND	
VSS	H10	GND	
VSS	H12	GND	
VSS	H14	GND	
VSS	H32	GND	
VSS	H34	GND	
VSS	H38	GND	
VSS	H40	GND	
VSS	H52	GND	
VSS	H54	GND	
VSS	H8	GND	
VSS	J11	GND	
VSS	J27	GND	
VSS	J31	GND	
VSS	J33	GND	
VSS	J39	GND	
VSS	J41	GND	
VSS	J5	GND	
VSS	J55	GND	
VSS	K2	GND	
VSS	K26	GND	
VSS	K28	GND	

Table 8-1. Land Name (Sheet 43 of 45)

Land Name	Land No.	Buffer Type	Direction
VSS	K30	GND	
VSS	K34	GND	
VSS	K8	GND	
VSS	L25	GND	
VSS	L29	GND	
VSS	L41	GND	
VSS	L5	GND	
VSS	M34	GND	
VSS	M36	GND	
VSS	M42	GND	
VSS	M44	GND	
VSS	M46	GND	
VSS	M50	GND	
VSS	M52	GND	
VSS	M8	GND	
VSS	N13	GND	
VSS	N33	GND	
VSS	N35	GND	
VSS	N37	GND	
VSS	N41	GND	
VSS	N43	GND	
VSS	N47	GND	
VSS	N49	GND	
VSS	N5	GND	
VSS	N53	GND	
VSS	N9	GND	
VSS	P10	GND	
VSS	P12	GND	
VSS	P14	GND	
VSS	P26	GND	
VSS	P30	GND	
VSS	P32	GND	
VSS	P38	GND	
VSS	P40	GND	
VSS	P54	GND	
VSS	P56	GND	
VSS	P8	GND	
VSS	R11	GND	
VSS	R29	GND	
VSS	R3	GND	
VSS	R31	GND	
VSS	R35	GND	
VSS	R39	GND	
VSS	R5	GND	
VSS	R55	GND	

Table 8-1. Land Name (Sheet 44 of 45)

Land Name	Land No.	Buffer Type	Direction
VSS	R7	GND	
VSS	T28	GND	
VSS	T4	GND	
VSS	T42	GND	
VSS	T6	GND	
VSS	T8	GND	
VSS	U35	GND	
VSS	U5	GND	
VSS	V26	GND	
VSS	V28	GND	
VSS	V34	GND	
VSS	V36	GND	
VSS	V42	GND	
VSS	V44	GND	
VSS	V46	GND	
VSS	V48	GND	
VSS	V50	GND	
VSS	V8	GND	
VSS	W13	GND	
VSS	W33	GND	
VSS	W37	GND	
VSS	W41	GND	
VSS	W43	GND	
VSS	W45	GND	
VSS	W47	GND	
VSS	W5	GND	
VSS	W51	GND	
VSS	W53	GND	
VSS	W9	GND	
VSS	Y10	GND	
VSS	Y12	GND	
VSS	Y28	GND	
VSS	Y30	GND	
VSS	Y32	GND	
VSS	Y36	GND	
VSS	Y38	GND	
VSS	Y40	GND	
VSS	Y42	GND	
VSS	Y56	GND	
VSS_VCC_SENSE	BY2		O
VSS_VSA_SENSE	AF14		O
VSS_VTTD_SENSE	BT42		O
VTTA	AE45	PWR	
VTTA	AE53	PWR	
VTTA	AM48	PWR	

Table 8-1. Land Name (Sheet 45 of 45)

Land Name	Land No.	Buffer Type	Direction
VTTA	AM54	PWR	
VTTA	AU53	PWR	
VTTA	CA53	PWR	
VTTA	CC45	PWR	
VTTA	CG55	PWR	
VTTA	CJ49	PWR	
VTTA	CR45	PWR	
VTTA	CR51	PWR	
VTTA	DA49	PWR	
VTTA	W49	PWR	
VTTA	Y54	PWR	
VTTD	AF22	PWR	
VTTD	AF24	PWR	
VTTD	AG21	PWR	
VTTD	AG23	PWR	
VTTD	AM42	PWR	
VTTD	AT42	PWR	
VTTD	AY42	PWR	
VTTD	BD42	PWR	
VTTD	BH42	PWR	
VTTD	BK56	PWR	
VTTD	BL51	PWR	
VTTD	BM42	PWR	
VTTD	BR55	PWR	
VTTD	BU47	PWR	
VTTD	BV42	PWR	
VTTD	BY20	PWR	
VTTD	BY22	PWR	
VTTD	CA21	PWR	
VTTD	CA23	PWR	
VTTD_SENSE	BP42		O

Table 8-2. Land Number (Sheet 1 of 45)

Land No.	Land Name	Buffer Type	Direction
A11	DDR3_DQ[33]	SSTL	I/O
A13	DDR3_MA[13]	SSTL	O
A15	DDR3_WE_N	SSTL	O
A17	DDR3_BA[0]	SSTL	O
A19	DDR3_MA[00]	SSTL	O
A21	DDR3_MA[05]	SSTL	O
A23	DDR3_MA[11]	SSTL	O
A33	DDR3_DQ[22]	SSTL	I/O
A35	DDR3_DQ[16]	SSTL	I/O
A37	DDR3_DQ[07]	SSTL	I/O
A39	DDR3_DQ[01]	SSTL	I/O
A41	VSS	GND	
A43	VSS	GND	
A45	VSS	GND	
A47	VSS	GND	
A49	VSS	GND	
A5	VSS	GND	
A51	VSS	GND	
A53	RSVD		
A7	VSS	GND	
A9	DDR3_DQ[39]	SSTL	I/O
AA11	VSS	GND	
AA13	DDR2_DQ[37]	SSTL	I/O
AA15	RSVD		
AA17	RSVD		
AA19	DDR2_CS_N[4]	SSTL	O
AA21	DDR2_CLK_DP[2]	SSTL	O
AA23	DDR2_CLK_DP[3]	SSTL	O
AA25	DDR2_CKE[0]	SSTL	O
AA27	DDR2_ECC[7]	SSTL	I/O
AA29	VSS	GND	
AA3	VSS	GND	
AA31	VSS	GND	
AA33	DDR2_DQS_DN[03]	SSTL	I/O
AA35	DDR2_DQ[28]	SSTL	I/O
AA37	DDR2_DQ[10]	SSTL	I/O
AA39	VSS	GND	
AA41	DDR2_DQ[13]	SSTL	I/O
AA43	PE3D_TX_DN[14]	PCIEX3	O
AA45	PE3D_TX_DP[12]	PCIEX3	O
AA47	PE3C_TX_DP[9]	PCIEX3	O
AA49	PE3A_RX_DP[3]	PCIEX3	I
AA5	VSS	GND	
AA51	PE3B_RX_DP[7]	PCIEX3	I
AA53	PE3B_RX_DP[6]	PCIEX3	I

Table 8-2. Land Number (Sheet 2 of 45)

Land No.	Land Name	Buffer Type	Direction
AA55	VSS	GND	
AA7	RSVD		
AA9	VSS	GND	
AB10	DDR2_DQ[38]	SSTL	I/O
AB12	RSVD		
AB14	VSS	GND	
AB16	RSVD		
AB18	DDR2_MA[00]	SSTL	O
AB20	DDR2_CS_N[0]	SSTL	O
AB22	DDR2_CLK_DP[1]	SSTL	O
AB24	DDR2_CLK_DP[0]	SSTL	O
AB26	DDR2_ECC[3]	SSTL	I/O
AB28	DDR2_DQS_DN[08]	SSTL	I/O
AB30	DDR2_ECC[4]	SSTL	I/O
AB32	DDR2_DQ[30]	SSTL	I/O
AB34	RSVD		
AB36	VSS	GND	
AB38	DDR2_DQS_DP[01]	SSTL	I/O
AB4	DDR2_DQS_DP[07]	SSTL	I/O
AB40	RSVD		
AB42	VSS	GND	
AB44	PE3D_TX_DN[13]	PCIEX3	O
AB46	PE3C_TX_DN[11]	PCIEX3	O
AB48	RSVD		
AB50	PE3B_RX_DN[4]	PCIEX3	I
AB52	PE3B_RX_DN[5]	PCIEX3	I
AB54	PE2B_RX_DP[4]	PCIEX3	I
AB56	PE2B_RX_DP[5]	PCIEX3	I
AB6	VSS	GND	
AB8	DDR2_DQS_DN[05]	SSTL	I/O
AC11	DDR2_DQS_DN[04]	SSTL	I/O
AC13	DDR2_DQ[32]	SSTL	I/O
AC15	DDR23_RCOMP[1]	Analog	I
AC17	VCCD_23	PWR	
AC19	VCCD_23	PWR	
AC21	VCCD_23	PWR	
AC23	VCCD_23	PWR	
AC25	VCCD_23	PWR	
AC27	DDR2_DQS_DP[08]	SSTL	I/O
AC29	RSVD		
AC3	DDR2_DQS_DN[07]	SSTL	I/O
AC31	VSS	GND	
AC33	DDR2_DQS_DP[03]	SSTL	I/O
AC35	DDR2_DQ[24]	SSTL	I/O
AC37	DDR2_DQ[11]	SSTL	I/O

Table 8-2. Land Number (Sheet 3 of 45)

Land No.	Land Name	Buffer Type	Direction
AC39	RSVD		
AC41	DDR2_DQ[12]	SSTL	I/O
AC43	PE3D_TX_DP[14]	PCIEX3	O
AC45	PE3D_TX_DN[12]	PCIEX3	O
AC47	PE3C_TX_DN[9]	PCIEX3	O
AC49	PE3A_RX_DN[3]	PCIEX3	I
AC5	RSVD		
AC51	PE3B_RX_DN[7]	PCIEX3	I
AC53	PE3B_RX_DN[6]	PCIEX3	I
AC55	PE2B_RX_DP[6]	PCIEX3	I
AC7	DDR2_DQS_DP[05]	SSTL	I/O
AC9	VSS	GND	
AD10	DDR2_DQ[39]	SSTL	I/O
AD12	RSVD		
AD14	DDR2_DQ[36]	SSTL	I/O
AD16	RSVD		
AD18	DDR2_ODT[2]	SSTL	O
AD20	RSVD		
AD22	RSVD		
AD24	DDR2_CKE[3]	SSTL	O
AD26	VSS	GND	
AD28	RSVD		
AD30	DDR2_ECC[5]	SSTL	I/O
AD32	DDR2_DQ[31]	SSTL	I/O
AD34	VSS	GND	
AD36	VSS	GND	
AD38	DDR2_DQS_DN[01]	SSTL	I/O
AD4	RSVD		
AD40	DDR2_DQ[09]	SSTL	I/O
AD42	VSS	GND	
AD44	VSS	GND	
AD46	VSS	GND	
AD48	VSS	GND	
AD50	VSS	GND	
AD52	VSS	GND	
AD54	PE2B_RX_DN[4]	PCIEX3	I
AD56	PE2B_RX_DN[5]	PCIEX3	I
AD6	VSS	GND	
AD8	DDR2_DQ[46]	SSTL	I/O
AE11	DDR2_DQS_DP[04]	SSTL	I/O
AE13	DDR2_DQ[33]	SSTL	I/O
AE15	VSA	PWR	
AE17	VSA	PWR	
AE19	DDR2_CS_N[1]	SSTL	O
AE21	RSVD		

Table 8-2. Land Number (Sheet 4 of 45)

Land No.	Land Name	Buffer Type	Direction
AE23	RSVD		
AE25	RSVD		
AE27	DDR_RESET_C23_N	CMOS1.5v	O
AE29	VSS	GND	
AE3	DDR2_DQ[63]	SSTL	I/O
AE31	VSS	GND	
AE33	DDR2_DQ[26]	SSTL	I/O
AE35	DDR2_DQ[25]	SSTL	I/O
AE37	DDR2_DQ[15]	SSTL	I/O
AE39	VSS	GND	
AE41	DDR2_DQ[08]	SSTL	I/O
AE43	VSS	GND	
AE45	VTTA	PWR	
AE47	VSS	GND	
AE49	VSS	GND	
AE5	DDR2_DQ[59]	SSTL	I/O
AE51	VSS	GND	
AE53	VTTA	PWR	
AE55	PE2B_RX_DN[6]	PCIEX3	I
AE57	PE2B_RX_DP[7]	PCIEX3	I
AE7	DDR2_DQ[47]	SSTL	I/O
AE9	VSS	GND	
AF10	DDR2_DQ[35]	SSTL	I/O
AF12	VSS	GND	
AF14	VSS_VSA_SENSE		O
AF16	VSS	GND	
AF18	VSA	PWR	
AF2	DDR2_DQ[62]	SSTL	I/O
AF20	VSS	GND	
AF22	VTTD	PWR	
AF24	VTTD	PWR	
AF26	VSS	GND	
AF28	DDR2_ECC[1]	SSTL	I/O
AF30	DDR2_ECC[0]	SSTL	I/O
AF32	DDR2_DQ[27]	SSTL	I/O
AF34	VSS	GND	
AF36	VSS	GND	
AF38	DDR2_DQ[14]	SSTL	I/O
AF4	DDR2_DQ[58]	SSTL	I/O
AF40	VSS	GND	
AF42	VSS	GND	
AF44	PE3A_RX_DP[0]	PCIEX3	I
AF46	PE3A_RX_DP[2]	PCIEX3	I
AF48	PE3C_RX_DP[8]	PCIEX3	I
AF50	PE3C_RX_DP[10]	PCIEX3	I

Table 8-2. Land Number (Sheet 5 of 45)

Land No.	Land Name	Buffer Type	Direction
AF52	PE_RBIAS_SENSE	PCIEX3	I
AF54	VSS	GND	
AF56	VSS	GND	
AF58	PE2B_RX_DN[7]	PCIEX3	I
AF6	VSS	GND	
AF8	DDR2_DQ[42]	SSTL	I/O
AG1	VSS	GND	
AG11	DDR2_DQ[34]	SSTL	I/O
AG13	VSA_SENSE		O
AG15	VSA	PWR	
AG17	VSA	PWR	
AG19	VCC	PWR	
AG21	VTTD	PWR	
AG23	VTTD	PWR	
AG25	VCC	PWR	
AG27	VCC	PWR	
AG29	VCC	PWR	
AG3	VSS	GND	
AG31	VCC	PWR	
AG33	VCC	PWR	
AG35	VCC	PWR	
AG37	VCC	PWR	
AG39	VCC	PWR	
AG41	VCC	PWR	
AG43	VSS	GND	
AG45	PE3A_RX_DP[1]	PCIEX3	I
AG47	PE3D_RX_DP[12]	PCIEX3	I
AG49	PE3C_RX_DP[11]	PCIEX3	I
AG5	VSS	GND	
AG51	PE3C_RX_DP[9]	PCIEX3	I
AG53	PE2B_TX_DP[4]	PCIEX3	O
AG55	VSS	GND	
AG57	VSS	GND	
AG7	DDR2_DQ[43]	SSTL	I/O
AG9	VSS	GND	
AH10	VSA	PWR	
AH12	VSA	PWR	
AH14	VSA	PWR	
AH16	VSA	PWR	
AH2	VSA	PWR	
AH4	VSA	PWR	
AH42	PROC_SEL_N		O
AH44	PE3A_RX_DN[0]	PCIEX3	I
AH46	PE3A_RX_DN[2]	PCIEX3	I
AH48	PE3C_RX_DN[8]	PCIEX3	I

Table 8-2. Land Number (Sheet 6 of 45)

Land No.	Land Name	Buffer Type	Direction
AH50	PE3C_RX_DN[10]	PCIEX3	I
AH52	PE_RBIAS	PCIEX3	I/O
AH54	PE2B_TX_DP[5]	PCIEX3	O
AH56	PE2C_RX_DP[8]	PCIEX3	I
AH58	VSS	GND	
AH6	VSA	PWR	
AH8	VSA	PWR	
AJ1	VSA	PWR	
AJ11	VSA	PWR	
AJ13	VSA	PWR	
AJ15	VSS	GND	
AJ17	VSS	GND	
AJ3	VSA	PWR	
AJ43	PE_VREF_CAP	PCIEX3	I/O
AJ45	PE3A_RX_DN[1]	PCIEX3	I
AJ47	PE3D_RX_DN[12]	PCIEX3	I
AJ49	PE3C_RX_DN[11]	PCIEX3	I
AJ5	VSA	PWR	
AJ51	PE3C_RX_DN[9]	PCIEX3	I
AJ53	PE2B_TX_DN[4]	PCIEX3	O
AJ55	BCLK_SELECT[1]	CMOS	I
AJ57	PE2C_RX_DP[10]	PCIEX3	I
AJ7	VSA	PWR	
AJ9	VSA	PWR	
AK10	VSS	GND	
AK12	VSS	GND	
AK14	VSS	GND	
AK16	VSS	GND	
AK2	VSS	GND	
AK4	VSS	GND	
AK42	VSS	GND	
AK44	VSS	GND	
AK46	VSS	GND	
AK48	VSS	GND	
AK50	VSS	GND	
AK52	RSVD		
AK54	PE2B_TX_DN[5]	PCIEX3	O
AK56	PE2C_RX_DN[8]	PCIEX3	I
AK58	PE2C_RX_DP[9]	PCIEX3	I
AK6	VSS	GND	
AK8	VSS	GND	
AL1	VCC	PWR	
AL11	VCC	PWR	
AL13	VCC	PWR	
AL15	VCC	PWR	

Table 8-2. Land Number (Sheet 7 of 45)

Land No.	Land Name	Buffer Type	Direction
AL17	VCC	PWR	
AL3	VCC	PWR	
AL43	VSS	GND	
AL45	VSS	GND	
AL47	RSVD		
AL49	VSS	GND	
AL5	VCC	PWR	
AL51	VSS	GND	
AL53	VSS	GND	
AL55	RSVD		
AL57	PE2C_RX_DN[10]	PCIEX3	I
AL7	VCC	PWR	
AL9	VCC	PWR	
AM10	VCC	PWR	
AM12	VCC	PWR	
AM14	VCC	PWR	
AM16	VCC	PWR	
AM2	VCC	PWR	
AM4	VCC	PWR	
AM42	VTTD	PWR	
AM44	RSVD		
AM46	PE3D_RX_DP[14]	PCIEX3	I
AM48	VTTA	PWR	
AM50	PE2A_TX_DP[1]	PCIEX3	O
AM52	PE2A_TX_DP[3]	PCIEX3	O
AM54	VTTA	PWR	
AM56	VSS	GND	
AM58	PE2C_RX_DN[9]	PCIEX3	I
AM6	VCC	PWR	
AM8	VCC	PWR	
AN1	VCC	PWR	
AN11	VCC	PWR	
AN13	VCC	PWR	
AN15	VCC	PWR	
AN17	VCC	PWR	
AN3	VCC	PWR	
AN43	CPU_ONLY_RESET	ODCMOS	I/O
AN45	PE3D_RX_DP[15]	PCIEX3	I
AN47	PE3D_RX_DP[13]	PCIEX3	I
AN49	PE2A_TX_DP[0]	PCIEX3	O
AN5	VCC	PWR	
AN51	PE2A_TX_DP[2]	PCIEX3	O
AN53	PE2B_TX_DP[6]	PCIEX3	O
AN55	VSS	GND	
AN57	VSS	GND	

Table 8-2. Land Number (Sheet 8 of 45)

Land No.	Land Name	Buffer Type	Direction
AN7	VCC	PWR	
AN9	VCC	PWR	
AP10	VCC	PWR	
AP12	VCC	PWR	
AP14	VCC	PWR	
AP16	VCC	PWR	
AP2	VCC	PWR	
AP4	VCC	PWR	
AP42	VSS	GND	
AP44	VSS	GND	
AP46	PE3D_RX_DN[14]	PCIEX3	I
AP48	RSVD		
AP50	PE2A_TX_DN[1]	PCIEX3	O
AP52	PE2A_TX_DN[3]	PCIEX3	O
AP54	PE2B_TX_DP[7]	PCIEX3	O
AP56	PE2D_RX_DP[13]	PCIEX3	I
AP58	VSS	GND	
AP6	VCC	PWR	
AP8	VCC	PWR	
AR1	VSS	GND	
AR11	VSS	GND	
AR13	VSS	GND	
AR15	VSS	GND	
AR17	VSS	GND	
AR3	VSS	GND	
AR43	BPM_N[0]	ODCMOS	I/O
AR45	PE3D_RX_DN[15]	PCIEX3	I
AR47	PE3D_RX_DN[13]	PCIEX3	I
AR49	PE2A_TX_DN[0]	PCIEX3	O
AR5	VSS	GND	
AR51	PE2A_TX_DN[2]	PCIEX3	O
AR53	PE2B_TX_DN[6]	PCIEX3	O
AR55	RSVD		
AR57	PE2C_RX_DP[11]	PCIEX3	I
AR7	VSS	GND	
AR9	VSS	GND	
AT10	VSS	GND	
AT12	VSS	GND	
AT14	VSS	GND	
AT16	VSS	GND	
AT2	VSS	GND	
AT4	VSS	GND	
AT42	VTTD	PWR	
AT44	BPM_N[1]	ODCMOS	I/O
AT46	VSS	GND	

Table 8-2. Land Number (Sheet 9 of 45)

Land No.	Land Name	Buffer Type	Direction
AT48	BIST_ENABLE	CMOS	I
AT50	TESTHI_AT50	CMOS	I
AT52	VSS	GND	
AT54	PE2B_TX_DN[7]	PCIEX3	O
AT56	PE2D_RX_DN[13]	PCIEX3	I
AT58	PE2D_RX_DP[12]	PCIEX3	I
AT6	VSS	GND	
AT8	VSS	GND	
AU1	VCC	PWR	
AU11	VCC	PWR	
AU13	VCC	PWR	
AU15	VCC	PWR	
AU17	VCC	PWR	
AU3	VCC	PWR	
AU43	BPM_N[2]	ODCMOS	I/O
AU45	VSS	GND	
AU47	VSS	GND	
AU49	VSS	GND	
AU5	VCC	PWR	
AU51	VSS	GND	
AU53	VTTA	PWR	
AU55	RSVD		
AU57	PE2C_RX_DN[11]	PCIEX3	I
AU7	VCC	PWR	
AU9	VCC	PWR	
AV10	VCC	PWR	
AV12	VCC	PWR	
AV14	VCC	PWR	
AV16	VCC	PWR	
AV2	VCC	PWR	
AV4	VCC	PWR	
AV42	VSS	GND	
AV44	BPM_N[3]	ODCMOS	I/O
AV46	RSVD		
AV48	PE2D_TX_DP[14]	PCIEX3	O
AV50	PE2D_TX_DP[12]	PCIEX3	O
AV52	PE2C_TX_DP[8]	PCIEX3	O
AV54	VSS	GND	
AV56	VSS	GND	
AV58	PE2D_RX_DN[12]	PCIEX3	I
AV6	VCC	PWR	
AV8	VCC	PWR	
AW1	VCC	PWR	
AW11	VCC	PWR	
AW13	VCC	PWR	

Table 8-2. Land Number (Sheet 10 of 45)

Land No.	Land Name	Buffer Type	Direction
AW15	VCC	PWR	
AW17	VCC	PWR	
AW3	VCC	PWR	
AW43	BPM_N[5]	ODCMOS	I/O
AW45	BCLK1_DP	CMOS	I
AW47	PE2D_TX_DP[15]	PCIEX3	O
AW49	PE2D_TX_DP[13]	PCIEX3	O
AW5	VCC	PWR	
AW51	PE2C_TX_DP[11]	PCIEX3	O
AW53	PE2C_TX_DP[9]	PCIEX3	O
AW55	VSS	GND	
AW57	VSS	GND	
AW7	VCC	PWR	
AW9	VCC	PWR	
AY10	VCC	PWR	
AY12	VCC	PWR	
AY14	VCC	PWR	
AY16	VCC	PWR	
AY2	VCC	PWR	
AY4	VCC	PWR	
AY42	VTTD	PWR	
AY44	BPM_N[7]	ODCMOS	I/O
AY46	RSVD		
AY48	PE2D_TX_DN[14]	PCIEX3	O
AY50	PE2D_TX_DN[12]	PCIEX3	O
AY52	PE2C_TX_DN[8]	PCIEX3	O
AY54	PE2C_TX_DP[10]	PCIEX3	O
AY56	PE2D_RX_DP[15]	PCIEX3	I
AY58	PE2D_RX_DP[14]	PCIEX3	I
AY6	VCC	PWR	
AY8	VCC	PWR	
B10	DDR3_DQS_DN[04]	SSTL	I/O
B12	DDR3_DQ[37]	SSTL	I/O
B14	DDR3_CAS_N	SSTL	O
B16	DDR3_RAS_N	SSTL	O
B18	RSVD		
B20	DDR3_MA[03]	SSTL	O
B22	DDR3_MA[07]	SSTL	O
B24	DDR3_BA[2]	SSTL	O
B32	DDR3_DQ[23]	SSTL	I/O
B34	RSVD		
B36	VSS	GND	
B38	DDR3_DQS_DN[00]	SSTL	I/O
B40	DDR3_DQ[00]	SSTL	I/O
B42	DMI_TX_DP[0]	PCIEX	O

Table 8-2. Land Number (Sheet 11 of 45)

Land No.	Land Name	Buffer Type	Direction
B44	DMI_TX_DP[2]	PCIEX	O
B46	RSVD		
B48	DMI_RX_DP[1]	PCIEX	I
B50	DMI_RX_DP[3]	PCIEX	I
B52	VSS	GND	
B54	VSA	PWR	
B6	VSS	GND	
B8	VSS	GND	
BA1	VCC	PWR	
BA11	VCC	PWR	
BA13	VCC	PWR	
BA15	VCC	PWR	
BA17	VCC	PWR	
BA3	VCC	PWR	
BA43	BPM_N[6]	ODCMOS	I/O
BA45	BCLK1_DN	CMOS	I
BA47	PE2D_TX_DN[15]	PCIEX3	O
BA49	PE2D_TX_DN[13]	PCIEX3	O
BA5	VCC	PWR	
BA51	PE2C_TX_DN[11]	PCIEX3	O
BA53	PE2C_TX_DN[9]	PCIEX3	O
BA55	TEST4		I
BA57	PE2D_RX_DN[14]	PCIEX3	I
BA7	VCC	PWR	
BA9	VCC	PWR	
BB10	VCC	PWR	
BB12	VCC	PWR	
BB14	VCC	PWR	
BB16	VCC	PWR	
BB2	VCC	PWR	
BB4	VCC	PWR	
BB42	VSS	GND	
BB44	BPM_N[4]	ODCMOS	I/O
BB46	VSS	GND	
BB48	VSS	GND	
BB50	VSS	GND	
BB52	VSS	GND	
BB54	PE2C_TX_DN[10]	PCIEX3	O
BB56	PE2D_RX_DN[15]	PCIEX3	I
BB58	VSS	GND	
BB6	VCC	PWR	
BB8	VCC	PWR	
BC1	VSS	GND	
BC11	VSS	GND	
BC13	VSS	GND	

Table 8-2. Land Number (Sheet 12 of 45)

Land No.	Land Name	Buffer Type	Direction
BC15	VSS	GND	
BC17	VSS	GND	
BC3	VSS	GND	
BC43	VSS	GND	
BC45	VSS	GND	
BC47	RSVD		
BC49	VSS	GND	
BC5	VSS	GND	
BC51	RSVD		
BC53	VSS	GND	
BC55	VSS	GND	
BC57	VSS	GND	
BC7	VSS	GND	
BC9	VSS	GND	
BD10	VSS	GND	
BD12	VSS	GND	
BD14	VSS	GND	
BD16	VSS	GND	
BD2	VSS	GND	
BD4	VSS	GND	
BD42	VTTD	PWR	
BD44	RSVD		
BD46	RSVD		
BD48	BCLK_SELECT[0]	CMOS	I
BD50	RSVD		
BD52	PROCHOT_N	ODCMOS	I/O
BD54	VSS	GND	
BD56	VSS	GND	
BD58	RSVD		
BD6	VSS	GND	
BD8	VSS	GND	
BE1	VCC	PWR	
BE11	VCC	PWR	
BE13	VCC	PWR	
BE15	VCC	PWR	
BE17	VCC	PWR	
BE3	VCC	PWR	
BE43	RSVD		
BE45	RSVD		
BE47	RSVD		
BE49	VSS	GND	
BE5	VCC	PWR	
BE51	VSS	GND	
BE53	RSVD		
BE55	RSVD		

Table 8-2. Land Number (Sheet 13 of 45)

Land No.	Land Name	Buffer Type	Direction
BE57	RSVD		
BE7	VCC	PWR	
BE9	VCC	PWR	
BF10	VCC	PWR	
BF12	VCC	PWR	
BF14	VCC	PWR	
BF16	VCC	PWR	
BF2	VCC	PWR	
BF4	VCC	PWR	
BF42	VSS	GND	
BF44	VSS	GND	
BF46	RSVD		
BF48	TESTHI_BF48	Open Drain	I/O
BF50	RSVD		
BF52	RSVD		
BF54	RSVD		
BF56	RSVD		
BF58	RSVD		
BF6	VCC	PWR	
BF8	VCC	PWR	
BG1	VCC	PWR	
BG11	VCC	PWR	
BG13	VCC	PWR	
BG15	VCC	PWR	
BG17	VCC	PWR	
BG3	VCC	PWR	
BG43	RSVD		
BG45	RSVD		
BG47	VSS	GND	
BG49	RSVD		
BG5	VCC	PWR	
BG51	RSVD		
BG53	RSVD		
BG55	RSVD		
BG57	RSVD		
BG7	VCC	PWR	
BG9	VCC	PWR	
BH10	VCC	PWR	
BH12	VCC	PWR	
BH14	VCC	PWR	
BH16	VCC	PWR	
BH2	VCC	PWR	
BH4	VCC	PWR	
BH42	VTTD	PWR	
BH44	RSVD		

Table 8-2. Land Number (Sheet 14 of 45)

Land No.	Land Name	Buffer Type	Direction
BH46	RSVD		
BH48	TESTHI_BH48	Open Drain	I/O
BH50	RSVD		
BH52	RSVD		
BH54	RSVD		
BH56	RSVD		
BH58	VSS	GND	
BH6	VCC	PWR	
BH8	VCC	PWR	
BJ1	VCC	PWR	
BJ11	VCC	PWR	
BJ13	VCC	PWR	
BJ15	VCC	PWR	
BJ17	VCC	PWR	
BJ3	VCC	PWR	
BJ43	RSVD		
BJ45	RSVD		
BJ47	PECI	PECI	I/O
BJ49	RSVD		
BJ5	VCC	PWR	
BJ51	RSVD		
BJ53	PWRGOOD	CMOS	I
BJ55	VSS	GND	
BJ57	VSS	GND	
BJ7	VCC	PWR	
BJ9	VCC	PWR	
BK10	VCC	PWR	
BK12	VCC	PWR	
BK14	VCC	PWR	
BK16	VCC	PWR	
BK2	VCC	PWR	
BK4	VCC	PWR	
BK42	VSS	GND	
BK44	RSVD		
BK46	VSS	GND	
BK48	VSS	GND	
BK50	VSS	GND	
BK52	VSS	GND	
BK54	VSS	GND	
BK56	VTTD	PWR	
BK58	RSVD		
BK6	VCC	PWR	
BK8	VCC	PWR	
BL1	VSS	GND	
BL11	VSS	GND	

Table 8-2. Land Number (Sheet 15 of 45)

Land No.	Land Name	Buffer Type	Direction
BL13	VSS	GND	
BL15	VSS	GND	
BL17	VSS	GND	
BL3	VSS	GND	
BL43	RSVD		
BL45	RSVD		
BL47	THERMTRIP_N	ODCMOS	O
BL49	VSS	GND	
BL5	VSS	GND	
BL51	VTTD	PWR	
BL53	RSVD		
BL55	RSVD		
BL57	RSVD		
BL7	VSS	GND	
BL9	VSS	GND	
BM10	VSS	GND	
BM12	VSS	GND	
BM14	VSS	GND	
BM16	VSS	GND	
BM2	VSS	GND	
BM4	VSS	GND	
BM42	VTTD	PWR	
BM44	RSVD		
BM46	RSVD		
BM48	RSVD		
BM50	RSVD		
BM52	RSVD		
BM54	RSVD		
BM56	RSVD		
BM58	RSVD		
BM6	VSS	GND	
BM8	VSS	GND	
BN1	VCC	PWR	
BN11	VCC	PWR	
BN13	VCC	PWR	
BN15	VCC	PWR	
BN17	VCC	PWR	
BN3	VCC	PWR	
BN43	VSS	GND	
BN45	VSS	GND	
BN47	RSVD		
BN49	RSVD		
BN5	VCC	PWR	
BN51	RSVD		
BN53	RSVD		

Table 8-2. Land Number (Sheet 16 of 45)

Land No.	Land Name	Buffer Type	Direction
BN55	RSVD		
BN57	RSVD		
BN7	VCC	PWR	
BN9	VCC	PWR	
BP10	VCC	PWR	
BP12	VCC	PWR	
BP14	VCC	PWR	
BP16	VCC	PWR	
BP2	VCC	PWR	
BP4	VCC	PWR	
BP42	VTTD_SENSE		O
BP44	RSVD		
BP46	RSVD		
BP48	RSVD		
BP50	RSVD		
BP52	RSVD		
BP54	RSVD		
BP56	RSVD		
BP58	VSS	GND	
BP6	VCC	PWR	
BP8	VCC	PWR	
BR1	VCC	PWR	
BR11	VCC	PWR	
BR13	VCC	PWR	
BR15	VCC	PWR	
BR17	VCC	PWR	
BR3	VCC	PWR	
BR43	RSVD		
BR45	SVIDDATA	ODCMOS	I/O
BR47	RSVD		
BR49	RSVD		
BR5	VCC	PWR	
BR51	RSVD		
BR53	VSS	GND	
BR55	VTTD	PWR	
BR57	VSS	GND	
BR7	VCC	PWR	
BR9	VCC	PWR	
BT10	VCC	PWR	
BT12	VCC	PWR	
BT14	VCC	PWR	
BT16	VCC	PWR	
BT2	VCC	PWR	
BT4	VCC	PWR	
BT42	VSS_VTTD_SENSE		O

Table 8-2. Land Number (Sheet 17 of 45)

Land No.	Land Name	Buffer Type	Direction
BT44	RSVD		
BT46	VSS	GND	
BT48	VSS	GND	
BT50	VSS	GND	
BT52	VSS	GND	
BT54	VSS	GND	
BT56	VSS	GND	
BT58	RSVD		
BT6	VCC	PWR	
BT8	VCC	PWR	
BU1	VCC	PWR	
BU11	VCC	PWR	
BU13	VCC	PWR	
BU15	VCC	PWR	
BU17	VCC	PWR	
BU3	VCC	PWR	
BU43	RSVD		
BU45	VSS	GND	
BU47	VTTD	PWR	
BU49	SKTOCC_N		O
BU5	VCC	PWR	
BU51	VSS	GND	
BU53	RSVD		
BU55	RSVD		
BU57	RSVD		
BU7	VCC	PWR	
BU9	VCC	PWR	
BV10	VCC	PWR	
BV12	VCC	PWR	
BV14	VCC	PWR	
BV16	VCC	PWR	
BV2	VCC	PWR	
BV4	VCC	PWR	
BV42	VTTD	PWR	
BV44	TMS	CMOS	I
BV46	RSVD		
BV48	RSVD		
BV50	RSVD		
BV52	RSVD		
BV54	RSVD		
BV56	RSVD		
BV58	RSVD		
BV6	VCC	PWR	
BV8	VCC	PWR	
BW1	VSS	GND	

Table 8-2. Land Number (Sheet 18 of 45)

Land No.	Land Name	Buffer Type	Direction
BW11	VSS	GND	
BW13	VSS	GND	
BW15	VSS	GND	
BW17	VSS	GND	
BW3	VCC_SENSE		O
BW43	TDI	CMOS	I
BW45	RSVD		
BW47	RSVD		
BW49	RSVD		
BW5	VSS	GND	
BW51	RSVD		
BW53	RSVD		
BW55	RSVD		
BW57	RSVD		
BW7	VSS	GND	
BW9	DDR0_DQ[28]	SSTL	I/O
BY10	DDR0_DQ[24]	SSTL	I/O
BY12	DDR0_DQ[25]	SSTL	I/O
BY14	VCCPLL	PWR	
BY16	DDR_VREFDQRX_C01	DC	I
BY18	VCC	PWR	
BY2	VSS_VCC_SENSE		O
BY20	VTTD	PWR	
BY22	VTTD	PWR	
BY24	VSS	GND	
BY26	VCC	PWR	
BY28	VCC	PWR	
BY30	VCC	PWR	
BY32	VCC	PWR	
BY34	VCC	PWR	
BY36	VCC	PWR	
BY38	VCC	PWR	
BY4	VSS	GND	
BY40	VCC	PWR	
BY42	VSS	GND	
BY44	TCK	CMOS	I
BY46	RSVD		
BY48	RSVD		
BY50	RSVD		
BY52	RSVD		
BY54	RSVD		
BY56	RSVD		
BY58	VSS	GND	
BY6	DDR0_DQ[04]	SSTL	I/O
BY8	VSS	GND	

Table 8-2. Land Number (Sheet 19 of 45)

Land No.	Land Name	Buffer Type	Direction
C11	VSS	GND	
C13	VSS	GND	
C15	VCCD_23	PWR	
C17	VCCD_23	PWR	
C19	VCCD_23	PWR	
C21	VCCD_23	PWR	
C23	VCCD_23	PWR	
C25	DDR3_ECC[3]	SSTL	I/O
C3	VSS	GND	
C33	VSS	GND	
C35	DDR3_DQ[21]	SSTL	I/O
C37	DDR3_DQ[02]	SSTL	I/O
C39	VSS	GND	
C41	VSS	GND	
C43	DMI_TX_DP[1]	PCIEX	O
C45	DMI_TX_DP[3]	PCIEX	O
C47	DMI_RX_DP[0]	PCIEX	I
C49	DMI_RX_DP[2]	PCIEX	I
C5	VSS	GND	
C51	PE1A_RX_DP[0]	PCIEX3	I
C53	RSVD		
C55	VSS	GND	
C7	DDR3_DQ[52]	SSTL	I/O
C9	DDR3_DQ[34]	SSTL	I/O
CA1	DDR0_DQ[12]	SSTL	I/O
CA11	VSS	GND	
CA13	VCCPLL	PWR	
CA15	VCCPLL	PWR	
CA17	DDR01_RCOMP[0]	Analog	I
CA19	VSS	GND	
CA21	VTTD	PWR	
CA23	VTTD	PWR	
CA25	VCC	PWR	
CA27	VSS	GND	
CA29	VCC	PWR	
CA3	DDR0_DQ[13]	SSTL	I/O
CA31	VSS	GND	
CA33	VSS	GND	
CA35	VSS	GND	
CA37	VSS	GND	
CA39	VSS	GND	
CA41	VSS	GND	
CA43	TDO	ODCMOS	O
CA45	RSVD		
CA47	RSVD		

Table 8-2. Land Number (Sheet 20 of 45)

Land No.	Land Name	Buffer Type	Direction
CA49	RSVD		
CA5	VSS	GND	
CA51	RSVD		
CA53	VTTA	PWR	
CA55	VSS	GND	
CA57	VSS	GND	
CA7	DDR0_DQ[05]	SSTL	I/O
CA9	DDR0_DQ[29]	SSTL	I/O
CB10	RSVD		
CB12	DDR0_DQ[26]	SSTL	I/O
CB14	DDR0_ECC[4]	SSTL	I/O
CB16	VSS	GND	
CB18	DDR_RESET_C01_N	CMOS1.5v	O
CB2	DDR0_DQ[08]	SSTL	I/O
CB20	DDR01_RCOMP[2]	Analog	I
CB22	MEM_HOT_C01_N	ODCMOS	I/O
CB24	RSVD		
CB26	RSVD		
CB28	RSVD		
CB30	DDR0_DQ[37]	SSTL	I/O
CB32	RSVD		
CB34	DDR0_DQ[39]	SSTL	I/O
CB36	VSS	GND	
CB38	DDR0_DQ[48]	SSTL	I/O
CB4	DDR0_DQ[09]	SSTL	I/O
CB40	DDR0_DQS_DN[06]	SSTL	I/O
CB42	DDR0_DQ[55]	SSTL	I/O
CB44	SVIDCLK	ODCMOS	O
CB46	VSS	GND	
CB48	VSS	GND	
CB50	VSS	GND	
CB52	VSS	GND	
CB54	RSVD		
CB56	VSS	GND	
CB6	VSS	GND	
CB8	VSS	GND	
CC11	RSVD		
CC13	VSS	GND	
CC15	DDR0_ECC[1]	SSTL	I/O
CC17	DDR0_DQS_DP[08]	SSTL	I/O
CC19	DDR01_RCOMP[1]	Analog	I
CC21	RSVD		
CC23	RSVD		
CC25	RSVD		
CC27	RSVD		

Table 8-2. Land Number (Sheet 21 of 45)

Land No.	Land Name	Buffer Type	Direction
CC29	VSS	GND	
CC3	VSS	GND	
CC31	DDR0_DQ[33]	SSTL	I/O
CC33	DDR0_DQS_DP[04]	SSTL	I/O
CC35	DDR0_DQ[35]	SSTL	I/O
CC37	DDR0_DQ[52]	SSTL	I/O
CC39	RSVD		
CC41	DDR0_DQ[54]	SSTL	I/O
CC43	VSS	GND	
CC45	VTTA	PWR	
CC47	VSS	GND	
CC49	VSS	GND	
CC5	RSVD		
CC51	CAT_ERR_N	ODCMOS	I/O
CC53	CORE_RBIAS_SENSE	Analog	I
CC55	RSVD		
CC7	DDR0_DQ[00]	SSTL	I/O
CC9	VSS	GND	
CD10	DDR0_DQS_DN[03]	SSTL	I/O
CD12	DDR0_DQ[27]	SSTL	I/O
CD14	DDR0_ECC[5]	SSTL	I/O
CD16	RSVD		
CD18	VSS	GND	
CD20	VCCD_01	PWR	
CD22	VCCD_01	PWR	
CD24	VCCD_01	PWR	
CD26	VCCD_01	PWR	
CD28	VCCD_01	PWR	
CD30	DDR0_DQ[36]	SSTL	I/O
CD32	RSVD		
CD34	DDR0_DQ[38]	SSTL	I/O
CD36	VSS	GND	
CD38	DDR0_DQ[49]	SSTL	I/O
CD4	RSVD		
CD40	DDR0_DQS_DP[06]	SSTL	I/O
CD42	DDR0_DQ[51]	SSTL	I/O
CD44	RSVD		
CD46	RSVD		
CD48	RSVD		
CD50	RSVD		
CD52	RSVD		
CD54	RSVD		
CD56	RSVD		
CD6	VSS	GND	
CD8	DDR0_DQ[01]	SSTL	I/O

Table 8-2. Land Number (Sheet 22 of 45)

Land No.	Land Name	Buffer Type	Direction
CE11	DDR0_DQS_DP[03]	SSTL	I/O
CE13	VSS	GND	
CE15	DDR0_ECC[0]	SSTL	I/O
CE17	DDR0_DQS_DN[08]	SSTL	I/O
CE19	RSVD		
CE21	DDR0_CLK_DN[2]	SSTL	O
CE23	DDR0_CLK_DN[1]	SSTL	O
CE25	DDR0_ODT[0]	SSTL	O
CE27	DDR0_ODT[1]	SSTL	O
CE29	DDR0_RAS_N	SSTL	O
CE3	DDR0_DQS_DN[01]	SSTL	I/O
CE31	DDR0_DQ[32]	SSTL	I/O
CE33	DDR0_DQS_DN[04]	SSTL	I/O
CE35	DDR0_DQ[34]	SSTL	I/O
CE37	DDR0_DQ[53]	SSTL	I/O
CE39	RSVD		
CE41	DDR0_DQ[50]	SSTL	I/O
CE43	RSVD		
CE45	RSVD		
CE47	RSVD		
CE49	RSVD		
CE5	VSS	GND	
CE51	RSVD		
CE53	CORE_RBIAS	Analog	I/O
CE55	RSVD		
CE7	RSVD		
CE9	VSS	GND	
CF10	DDR0_DQ[31]	SSTL	I/O
CF12	VSS	GND	
CF14	VSS	GND	
CF16	RSVD		
CF18	DDR0_ECC[3]	SSTL	I/O
CF20	RSVD		
CF22	DDR0_CLK_DN[3]	SSTL	O
CF24	DDR0_CLK_DN[0]	SSTL	O
CF26	DDR0_CS_N[5]	SSTL	O
CF28	DDR0_ODT[3]	SSTL	O
CF30	VSS	GND	
CF32	VSS	GND	
CF34	VSS	GND	
CF36	VSS	GND	
CF38	VSS	GND	
CF4	DDR0_DQS_DP[01]	SSTL	I/O
CF40	VSS	GND	
CF42	VSS	GND	

Table 8-2. Land Number (Sheet 23 of 45)

Land No.	Land Name	Buffer Type	Direction
CF44	RSVD		
CF46	RSVD		
CF48	RSVD		
CF50	RSVD		
CF52	RSVD		
CF54	RSVD		
CF56	RSVD		
CF6	VSS	GND	
CF8	RSVD		
CG11	RSVD		
CG13	DDR0_DQ[20]	SSTL	I/O
CG15	VSS	GND	
CG17	DDR0_ECC[6]	SSTL	I/O
CG19	DDR0_MA[14]	SSTL	O
CG21	DDR0_CLK_DP[2]	SSTL	O
CG23	DDR0_CLK_DP[1]	SSTL	O
CG25	DDR0_MA[02]	SSTL	O
CG27	DDR0_CS_N[4]	SSTL	O
CG29	DDR0_MA[13]	SSTL	O
CG3	DDR0_DQ[14]	SSTL	I/O
CG31	VSS	GND	
CG33	VSS	GND	
CG35	VSS	GND	
CG37	VSS	GND	
CG39	VSS	GND	
CG41	VSS	GND	
CG43	VSS	GND	
CG45	RSVD		
CG47	RSVD		
CG49	RSVD		
CG5	DDR0_DQ[15]	SSTL	I/O
CG51	RSVD		
CG53	VSS	GND	
CG55	VTTA	PWR	
CG7	DDR0_DQS_DN[00]	SSTL	I/O
CG9	VSS	GND	
CH10	DDR0_DQ[30]	SSTL	I/O
CH12	VSS	GND	
CH14	DDR0_DQS_DN[02]	SSTL	I/O
CH16	VSS	GND	
CH18	DDR0_ECC[2]	SSTL	I/O
CH20	DDR0_CKE[2]	SSTL	O
CH22	DDR0_CLK_DP[3]	SSTL	O
CH24	DDR0_CLK_DP[0]	SSTL	O
CH26	DDR0_CS_N[1]	SSTL	O

Table 8-2. Land Number (Sheet 24 of 45)

Land No.	Land Name	Buffer Type	Direction
CH28	DDR0_ODT[2]	SSTL	O
CH30	DDR0_DQ[45]	SSTL	I/O
CH32	RSVD		
CH34	DDR0_DQ[47]	SSTL	I/O
CH36	VSS	GND	
CH38	DDR0_DQ[56]	SSTL	I/O
CH4	DDR0_DQ[10]	SSTL	I/O
CH40	DDR0_DQS_DN[07]	SSTL	I/O
CH42	DDR0_DQ[58]	SSTL	I/O
CH44	VSS	GND	
CH46	VSS	GND	
CH48	VSS	GND	
CH50	VSS	GND	
CH52	VSS	GND	
CH54	VSS	GND	
CH56	EAR_N	ODCMOS	I/O
CH6	VSS	GND	
CH8	DDR0_DQS_DP[00]	SSTL	I/O
CJ11	VSS	GND	
CJ13	RSVD		
CJ15	DDR0_DQ[22]	SSTL	I/O
CJ17	VSS	GND	
CJ19	VCCD_01	PWR	
CJ21	VCCD_01	PWR	
CJ23	VCCD_01	PWR	
CJ25	VCCD_01	PWR	
CJ27	VCCD_01	PWR	
CJ29	VSS	GND	
CJ3	VSS	GND	
CJ31	DDR0_DQ[41]	SSTL	I/O
CJ33	DDR0_DQS_DP[05]	SSTL	I/O
CJ35	DDR0_DQ[43]	SSTL	I/O
CJ37	DDR0_DQ[60]	SSTL	I/O
CJ39	RSVD		
CJ41	DDR0_DQ[62]	SSTL	I/O
CJ43	VSS	GND	
CJ45	VSS	GND	
CJ47	VSS	GND	
CJ49	VTTA	PWR	
CJ5	DDR0_DQ[11]	SSTL	I/O
CJ51	VSS	GND	
CJ53	RSVD		
CJ55	RSVD		
CJ7	DDR0_DQ[06]	SSTL	I/O
CJ9	VSS	GND	

Table 8-2. Land Number (Sheet 25 of 45)

Land No.	Land Name	Buffer Type	Direction
CK10	VSS	GND	
CK12	DDR0_DQ[16]	SSTL	I/O
CK14	DDR0_DQS_DP[02]	SSTL	I/O
CK16	DDR0_DQ[18]	SSTL	I/O
CK18	DDR0_ECC[7]	SSTL	I/O
CK20	DDR0_MA[12]	SSTL	O
CK22	DDR0_MA[08]	SSTL	O
CK24	DDR0_MA[03]	SSTL	O
CK26	DDR0_MA[10]	SSTL	O
CK28	RSVD		
CK30	DDR0_DQ[44]	SSTL	I/O
CK32	RSVD		
CK34	DDR0_DQ[46]	SSTL	I/O
CK36	VSS	GND	
CK38	DDR0_DQ[57]	SSTL	I/O
CK4	VSS	GND	
CK40	DDR0_DQS_DP[07]	SSTL	I/O
CK42	DDR0_DQ[59]	SSTL	I/O
CK44	RESET_N	CMOS	I
CK46	RSVD		
CK48	RSVD		
CK50	RSVD		
CK52	RSVD		
CK54	RSVD		
CK56	RSVD		
CK6	VSS	GND	
CK8	DDR0_DQ[02]	SSTL	I/O
CL11	DDR0_DQ[21]	SSTL	I/O
CL13	RSVD		
CL15	DDR0_DQ[23]	SSTL	I/O
CL17	VSS	GND	
CL19	DDR0_CKE[0]	SSTL	O
CL21	DDR0_MA[11]	SSTL	O
CL23	DDR0_MA[05]	SSTL	O
CL25	DDR0_MA[00]	SSTL	O
CL27	RSVD		
CL29	DDR0_CAS_N	SSTL	O
CL3	DDR1_DQ[05]	SSTL	I/O
CL31	DDR0_DQ[40]	SSTL	I/O
CL33	DDR0_DQS_DN[05]	SSTL	I/O
CL35	DDR0_DQ[42]	SSTL	I/O
CL37	DDR0_DQ[61]	SSTL	I/O
CL39	RSVD		
CL41	DDR0_DQ[63]	SSTL	I/O
CL43	VSS	GND	

Table 8-2. Land Number (Sheet 26 of 45)

Land No.	Land Name	Buffer Type	Direction
CL45	RSVD		
CL47	RSVD		
CL49	RSVD		
CL5	VSS	GND	
CL51	RSVD		
CL53	RSVD		
CL55	RSVD		
CL7	DDR0_DQ[07]	SSTL	I/O
CL9	DDR0_DQ[03]	SSTL	I/O
CM10	VSS	GND	
CM12	DDR0_DQ[17]	SSTL	I/O
CM14	VSS	GND	
CM16	DDR0_DQ[19]	SSTL	I/O
CM18	DDR0_CKE[1]	SSTL	O
CM20	DDR0_BA[2]	SSTL	O
CM22	DDR0_MA[07]	SSTL	O
CM24	DDR0_MA[04]	SSTL	O
CM26	RSVD		
CM28	DDR0_BA[0]	SSTL	O
CM30	VSS	GND	
CM32	VSS	GND	
CM34	VSS	GND	
CM36	VSS	GND	
CM38	VSS	GND	
CM4	DDR1_DQ[04]	SSTL	I/O
CM40	VSS	GND	
CM42	VSS	GND	
CM44	BCLK0_DN	CMOS	I
CM46	RSVD		
CM48	RSVD		
CM50	RSVD		
CM52	RSVD		
CM54	RSVD		
CM56	RSVD		
CM6	VSS	GND	
CM8	VSS	GND	
CN11	VSS	GND	
CN13	VSS	GND	
CN15	VSS	GND	
CN17	VSS	GND	
CN19	DDR0_MA[15]	SSTL	O
CN21	DDR0_MA[09]	SSTL	O
CN23	DDR0_MA[06]	SSTL	O
CN25	DDR0_CS_N[0]	SSTL	O
CN27	DDR0_BA[1]	SSTL	O

Table 8-2. Land Number (Sheet 27 of 45)

Land No.	Land Name	Buffer Type	Direction
CN29	DDR0_WE_N	SSTL	O
CN3	VSS	GND	
CN31	VSS	GND	
CN33	VSS	GND	
CN35	VSS	GND	
CN37	VSS	GND	
CN39	VSS	GND	
CN41	DDR_VREFDQTX_C01	DC	O
CN43	BCLK0_DP	CMOS	I
CN45	RSVD		
CN47	RSVD		
CN49	RSVD		
CN5	VSS	GND	
CN51	RSVD		
CN53	VSS	GND	
CN55	VSS	GND	
CN57	VSS	GND	
CN7	VSS	GND	
CN9	VSS	GND	
CP10	DDR1_DQ[19]	SSTL	I/O
CP12	VSS	GND	
CP14	RSVD		
CP16	VSS	GND	
CP18	DDR0_CKE[3]	SSTL	O
CP2	DDR1_DQ[01]	SSTL	I/O
CP20	VCCD_01	PWR	
CP22	VCCD_01	PWR	
CP24	VCCD_01	PWR	
CP26	VCCD_01	PWR	
CP28	VCCD_01	PWR	
CP30	DDR1_DQ[33]	SSTL	I/O
CP32	DDR1_DQS_DP[04]	SSTL	I/O
CP34	DDR1_DQ[35]	SSTL	I/O
CP36	VSS	GND	
CP38	RSVD		
CP4	DDR1_DQ[00]	SSTL	I/O
CP40	VSS	GND	
CP42	VSS	GND	
CP44	VSS	GND	
CP46	VSS	GND	
CP48	VSS	GND	
CP50	VSS	GND	
CP52	VSS	GND	
CP54	RSVD		
CP56	VSS	GND	

Table 8-2. Land Number (Sheet 28 of 45)

Land No.	Land Name	Buffer Type	Direction
CP58	RSVD		
CP6	DDR1_DQ[20]	SSTL	I/O
CP8	RSVD		
CR1	RSVD		
CR11	VSS	GND	
CR13	DDR1_DQ[24]	SSTL	I/O
CR15	DDR1_DQS_DN[03]	SSTL	I/O
CR17	DDR1_DQ[26]	SSTL	I/O
CR19	RSVD		
CR21	RSVD		
CR23	RSVD		
CR25	DDR0_MA[01]	SSTL	O
CR27	RSVD		
CR29	DDR1_DQ[37]	SSTL	I/O
CR3	DDR1_DQS_DP[00]	SSTL	I/O
CR31	RSVD		
CR33	DDR1_DQ[39]	SSTL	I/O
CR35	VSS	GND	
CR37	DDR1_DQ[48]	SSTL	I/O
CR39	DDR1_DQS_DN[06]	SSTL	I/O
CR41	DDR1_DQ[50]	SSTL	I/O
CR43	SVIDALERT_N	CMOS	I
CR45	VTTA	PWR	
CR47	VSS	GND	
CR49	VSS	GND	
CR5	VSS	GND	
CR51	VTTA	PWR	
CR53	RSVD		
CR55	RSVD		
CR57	RSVD		
CR7	DDR1_DQ[16]	SSTL	I/O
CR9	VSS	GND	
CT10	DDR1_DQ[18]	SSTL	I/O
CT12	DDR1_DQ[28]	SSTL	I/O
CT14	RSVD		
CT16	DDR1_DQ[30]	SSTL	I/O
CT18	RSVD		
CT2	RSVD		
CT20	DDR1_CKE[0]	SSTL	O
CT22	DDR1_ODT[0]	SSTL	O
CT24	DDR1_CS_N[5]	SSTL	O
CT26	RSVD		
CT28	VSS	GND	
CT30	DDR1_DQ[32]	SSTL	I/O
CT32	DDR1_DQS_DN[04]	SSTL	I/O

Table 8-2. Land Number (Sheet 29 of 45)

Land No.	Land Name	Buffer Type	Direction
CT34	DDR1_DQ[34]	SSTL	I/O
CT36	DDR1_DQ[52]	SSTL	I/O
CT38	RSVD		
CT4	DDR1_DQS_DN[00]	SSTL	I/O
CT40	DDR1_DQ[54]	SSTL	I/O
CT42	VSS	GND	
CT44	RSVD		
CT46	RSVD		
CT48	RSVD		
CT50	RSVD		
CT52	RSVD		
CT54	TRST_N	CMOS	I
CT56	RSVD		
CT58	RSVD		
CT6	DDR1_DQ[21]	SSTL	I/O
CT8	RSVD		
CU1	VSS	GND	
CU11	VSS	GND	
CU13	DDR1_DQ[25]	SSTL	I/O
CU15	DDR1_DQS_DP[03]	SSTL	I/O
CU17	DDR1_DQ[27]	SSTL	I/O
CU19	DDR1_CKE[1]	SSTL	O
CU21	RSVD		
CU23	DDR1_CS_N[1]	SSTL	O
CU25	DDR1_CS_N[4]	SSTL	O
CU27	RSVD		
CU29	DDR1_DQ[36]	SSTL	I/O
CU3	VSS	GND	
CU31	RSVD		
CU33	DDR1_DQ[38]	SSTL	I/O
CU35	VSS	GND	
CU37	DDR1_DQ[49]	SSTL	I/O
CU39	DDR1_DQS_DP[06]	SSTL	I/O
CU41	DDR1_DQ[51]	SSTL	I/O
CU43	RSVD		
CU45	RSVD		
CU47	RSVD		
CU49	RSVD		
CU5	VSS	GND	
CU51	CORE_VREF_CAP		I/O
CU53	RSVD		
CU55	RSVD		
CU57	RSVD		
CU7	DDR1_DQ[17]	SSTL	I/O
CU9	DDR1_DQS_DP[02]	SSTL	I/O

Table 8-2. Land Number (Sheet 30 of 45)

Land No.	Land Name	Buffer Type	Direction
CV10	DDR1_DQ[23]	SSTL	I/O
CV12	DDR1_DQ[29]	SSTL	I/O
CV14	VSS	GND	
CV16	DDR1_DQ[31]	SSTL	I/O
CV18	VSS	GND	
CV2	DDR1_DQ[06]	SSTL	I/O
CV20	DDR1_CLK_DN[0]	SSTL	O
CV22	DDR1_CLK_DN[1]	SSTL	O
CV24	DDR1_CLK_DP[2]	SSTL	O
CV26	DDR1_ODT[3]	SSTL	O
CV28	DDR1_WE_N	SSTL	O
CV30	VSS	GND	
CV32	VSS	GND	
CV34	VSS	GND	
CV36	DDR1_DQ[53]	SSTL	I/O
CV38	VSS	GND	
CV4	DDR1_DQ[02]	SSTL	I/O
CV40	DDR1_DQ[55]	SSTL	I/O
CV42	VSS	GND	
CV44	RSVD		
CV46	RSVD		
CV48	RSVD		
CV50	RSVD		
CV52	RSVD		
CV54	VSS	GND	
CV56	RSVD		
CV58	VSS	GND	
CV6	VSS	GND	
CV8	DDR1_DQS_DN[02]	SSTL	I/O
CW1	TEST1		O
CW11	VSS	GND	
CW13	VSS	GND	
CW15	VSS	GND	
CW17	DRAM_PWR_OK_C01	CMOS1.5v	I
CW19	VCCD_01	PWR	
CW21	VCCD_01	PWR	
CW23	VCCD_01	PWR	
CW25	VCCD_01	PWR	
CW27	VCCD_01	PWR	
CW29	VSS	GND	
CW3	DDR1_DQ[07]	SSTL	I/O
CW31	VSS	GND	
CW33	VSS	GND	
CW35	VSS	GND	
CW37	VSS	GND	

Table 8-2. Land Number (Sheet 31 of 45)

Land No.	Land Name	Buffer Type	Direction
CW39	VSS	GND	
CW41	DDR_SDA_C01	ODCMOS	I/O
CW43	RSVD		
CW45	RSVD		
CW47	RSVD		
CW49	RSVD		
CW5	VSS	GND	
CW51	VSS	GND	
CW53	VSS	GND	
CW55	VSS	GND	
CW57	VSS	GND	
CW7	VSS	GND	
CW9	DDR1_DQ[22]	SSTL	I/O
CY10	VSS	GND	
CY12	VSS	GND	
CY14	RSVD		
CY16	VSS	GND	
CY18	DDR1_CKE[2]	SSTL	O
CY2	VSS	GND	
CY20	DDR1_CLK_DP[0]	SSTL	O
CY22	DDR1_CLK_DP[1]	SSTL	O
CY24	DDR1_CLK_DN[2]	SSTL	O
CY26	DDR1_ODT[2]	SSTL	O
CY28	RSVD		
CY30	DDR1_CAS_N	SSTL	O
CY32	DDR1_DQ[45]	SSTL	I/O
CY34	DDR1_DQS_DN[05]	SSTL	I/O
CY36	VSS	GND	
CY38	RSVD		
CY4	DDR1_DQ[03]	SSTL	I/O
CY40	VSS	GND	
CY42	DDR_SCL_C01	ODCMOS	I/O
CY44	VSS	GND	
CY46	RSVD		
CY48	RSVD		
CY50	VSS	GND	
CY52	VSS	GND	
CY54	RSVD		
CY56	RSVD		
CY58	RSVD		
CY6	DDR1_DQ[12]	SSTL	I/O
CY8	VSS	GND	
D10	DDR3_DQS_DP[04]	SSTL	I/O
D12	DDR3_DQ[32]	SSTL	I/O
D14	RSVD		

Table 8-2. Land Number (Sheet 32 of 45)

Land No.	Land Name	Buffer Type	Direction
D16	RSVD		
D18	DDR3_MA[10]	SSTL	O
D2	VSS	GND	
D20	DDR3_MA[04]	SSTL	O
D22	DDR3_MA[08]	SSTL	O
D24	DDR3_MA[14]	SSTL	O
D26	VSS	GND	
D32	DDR3_DQ[18]	SSTL	I/O
D34	RSVD		
D36	VSS	GND	
D38	DDR3_DQS_DP[00]	SSTL	I/O
D4	TEST3		O
D40	DDR3_DQ[05]	SSTL	I/O
D42	DMI_TX_DN[0]	PCIEX	O
D44	DMI_TX_DN[2]	PCIEX	O
D46	RSVD		
D48	DMI_RX_DN[1]	PCIEX	I
D50	DMI_RX_DN[3]	PCIEX	I
D52	PE1A_RX_DP[1]	PCIEX3	I
D54	PE1A_RX_DP[2]	PCIEX3	I
D56	RSVD		
D6	DDR3_DQ[53]	SSTL	I/O
D8	VSS	GND	
DA11	VSS	GND	
DA13	DDR1_ECC[4]	SSTL	I/O
DA15	DDR1_ECC[6]	SSTL	I/O
DA17	DDR1_CKE[3]	SSTL	O
DA19	DDR1_MA[09]	SSTL	O
DA21	DDR1_CLK_DN[3]	SSTL	O
DA23	DDR1_MA[03]	SSTL	O
DA25	DDR1_ODT[1]	SSTL	O
DA27	RSVD		
DA29	RSVD		
DA3	VSS	GND	
DA31	DDR1_DQ[44]	SSTL	I/O
DA33	DDR1_DQ[40]	SSTL	I/O
DA35	DDR1_DQ[43]	SSTL	I/O
DA37	DDR1_DQ[60]	SSTL	I/O
DA39	DDR1_DQ[62]	SSTL	I/O
DA41	VSS	GND	
DA43	VSS	GND	
DA45	VSS	GND	
DA47	VSS	GND	
DA49	VTTA	PWR	
DA5	VSS	GND	

Table 8-2. Land Number (Sheet 33 of 45)

Land No.	Land Name	Buffer Type	Direction
DA51	VSS	GND	
DA53	RSVD		
DA55	RSVD		
DA57	RSVD		
DA7	DDR1_DQ[08]	SSTL	I/O
DA9	VSS	GND	
DB10	DDR1_DQ[14]	SSTL	I/O
DB12	VSS	GND	
DB14	RSVD		
DB16	DDR1_ECC[3]	SSTL	I/O
DB18	DDR1_MA[14]	SSTL	O
DB2	VSS	GND	
DB20	DDR1_MA[08]	SSTL	O
DB22	DDR1_MA[04]	SSTL	O
DB24	DDR1_CS_N[0]	SSTL	O
DB26	DDR1_BA[0]	SSTL	O
DB28	DDR1_RAS_N	SSTL	O
DB30	DDR1_MA[13]	SSTL	O
DB32	VSS	GND	
DB34	DDR1_DQS_DP[05]	SSTL	I/O
DB36	VSS	GND	
DB38	RSVD		
DB4	TEST0		O
DB40	DDR1_DQ[59]	SSTL	I/O
DB42	RSVD		
DB44	RSVD		
DB46	RSVD		
DB48	RSVD		
DB50	RSVD		
DB52	RSVD		
DB54	RSVD		
DB56	RSVD		
DB58	VSS	GND	
DB6	DDR1_DQ[13]	SSTL	I/O
DB8	RSVD		
DC11	DDR1_DQ[10]	SSTL	I/O
DC13	DDR1_ECC[5]	SSTL	I/O
DC15	DDR1_DQS_DP[08]	SSTL	I/O
DC17	DDR1_MA[15]	SSTL	O
DC19	DDR1_MA[12]	SSTL	O
DC21	DDR1_CLK_DP[3]	SSTL	O
DC23	DDR1_MA[00]	SSTL	O
DC25	DDR1_BA[1]	SSTL	O
DC3	VSS	GND	
DC33	RSVD		

Table 8-2. Land Number (Sheet 34 of 45)

Land No.	Land Name	Buffer Type	Direction
DC35	DDR1_DQ[42]	SSTL	I/O
DC37	DDR1_DQ[61]	SSTL	I/O
DC39	DDR1_DQS_DP[07]	SSTL	I/O
DC41	VSS	GND	
DC43	RSVD		
DC45	RSVD		
DC47	RSVD		
DC49	RSVD		
DC5	VSS	GND	
DC51	RSVD		
DC53	RSVD		
DC55	RSVD		
DC7	DDR1_DQ[09]	SSTL	I/O
DC9	DDR1_DQS_DN[01]	SSTL	I/O
DD10	VSS	GND	
DD12	VSS	GND	
DD14	VSS	GND	
DD16	DDR1_ECC[2]	SSTL	I/O
DD18	VCCD_01	PWR	
DD20	VCCD_01	PWR	
DD22	VCCD_01	PWR	
DD24	VCCD_01	PWR	
DD26	VCCD_01	PWR	
DD32	DDR1_DQ[41]	SSTL	I/O
DD34	VSS	GND	
DD36	VSS	GND	
DD38	VSS	GND	
DD40	DDR1_DQ[58]	SSTL	I/O
DD42	RSVD		
DD44	RSVD		
DD46	RSVD		
DD48	RSVD		
DD50	RSVD		
DD52	RSVD		
DD54	RSVD		
DD6	VSS	GND	
DD8	RSVD		
DE11	DDR1_DQ[11]	SSTL	I/O
DE13	DDR1_ECC[0]	SSTL	I/O
DE15	DDR1_DQS_DN[08]	SSTL	I/O
DE17	VSS	GND	
DE19	DDR1_MA[11]	SSTL	O
DE21	DDR1_MA[06]	SSTL	O
DE23	DDR1_MA[01]	SSTL	O
DE25	RSVD		

Table 8-2. Land Number (Sheet 35 of 45)

Land No.	Land Name	Buffer Type	Direction
DE33	RSVD		
DE35	DDR1_DQ[47]	SSTL	I/O
DE37	DDR1_DQ[56]	SSTL	I/O
DE39	DDR1_DQS_DN[07]	SSTL	I/O
DE41	VSS	GND	
DE43	RSVD		
DE45	RSVD		
DE47	RSVD		
DE49	RSVD		
DE51	RSVD		
DE53	VSS	GND	
DE55	RSVD		
DE7	VSS	GND	
DE9	DDR1_DQS_DP[01]	SSTL	I/O
DF10	DDR1_DQ[15]	SSTL	I/O
DF12	VSS	GND	
DF14	DDR1_ECC[1]	SSTL	I/O
DF16	DDR1_ECC[7]	SSTL	I/O
DF18	DDR1_BA[2]	SSTL	O
DF20	DDR1_MA[07]	SSTL	O
DF22	DDR1_MA[05]	SSTL	O
DF24	DDR1_MA[02]	SSTL	O
DF26	DDR1_MA[10]	SSTL	O
DF34	DDR1_DQ[46]	SSTL	I/O
DF36	VSS	GND	
DF38	DDR1_DQ[57]	SSTL	I/O
DF40	DDR1_DQ[63]	SSTL	I/O
DF42	VSS	GND	
DF44	VSS	GND	
DF46	VSS	GND	
DF48	VSS	GND	
DF50	VSS	GND	
DF52	VSS	GND	
DF8	VSS	GND	
E1	VSS	GND	
E11	RSVD		
E13	MEM_HOT_C23_N	ODCMOS	I/O
E15	RSVD		
E17	DDR3_ODT[2]	SSTL	O
E19	DDR3_BA[1]	SSTL	O
E21	DDR3_MA[01]	SSTL	O
E23	DDR3_MA[12]	SSTL	O
E25	DDR3_ECC[2]	SSTL	I/O
E27	DDR3_DQS_DP[08]	SSTL	I/O
E29	VSS	GND	

Table 8-2. Land Number (Sheet 36 of 45)

Land No.	Land Name	Buffer Type	Direction
E3	VSS	GND	
E31	VSS	GND	
E33	DDR3_DQS_DP[02]	SSTL	I/O
E35	DDR3_DQ[20]	SSTL	I/O
E37	DDR3_DQ[03]	SSTL	I/O
E39	RSVD		
E41	VSS	GND	
E43	DMI_TX_DN[1]	PCIEX	O
E45	DMI_TX_DN[3]	PCIEX	O
E47	DMI_RX_DN[0]	PCIEX	I
E49	DMI_RX_DN[2]	PCIEX	I
E5	VSS	GND	
E51	PE1A_RX_DN[0]	PCIEX3	I
E53	RSVD		
E55	PE1A_RX_DP[3]	PCIEX3	I
E57	RSVD		
E7	DDR3_DQ[48]	SSTL	I/O
E9	DDR3_DQ[35]	SSTL	I/O
F10	DDR3_DQ[38]	SSTL	I/O
F12	DDR3_DQ[36]	SSTL	I/O
F14	RSVD		
F16	RSVD		
F18	DDR3_ODT[1]	SSTL	O
F2	TEST2		O
F20	DDR3_MA[02]	SSTL	O
F22	DDR3_MA[06]	SSTL	O
F24	DDR3_MA[15]	SSTL	O
F26	DDR3_ECC[6]	SSTL	I/O
F28	RSVD		
F30	DDR3_ECC[4]	SSTL	I/O
F32	DDR3_DQ[19]	SSTL	I/O
F34	DDR3_DQ[17]	SSTL	I/O
F36	VSS	GND	
F38	DDR3_DQ[06]	SSTL	I/O
F4	DDR3_DQ[60]	SSTL	I/O
F40	DDR3_DQ[04]	SSTL	I/O
F42	VSS	GND	
F44	VSS	GND	
F46	RSVD		
F48	VSS	GND	
F50	VSS	GND	
F52	PE1A_RX_DN[1]	PCIEX3	I
F54	PE1A_RX_DN[2]	PCIEX3	I
F56	RSVD		
F58	RSVD		

Table 8-2. Land Number (Sheet 37 of 45)

Land No.	Land Name	Buffer Type	Direction
F6	DDR3_DQ[49]	SSTL	I/O
F8	VSS	GND	
G1	VSS	GND	
G11	RSVD		
G13	VCCD_23	PWR	
G15	RSVD		
G17	DDR3_CS_N[5]	SSTL	O
G19	DDR3_CS_N[0]	SSTL	O
G21	RSVD		
G23	DDR3_MA[09]	SSTL	O
G25	VSS	GND	
G27	DDR3_DQS_DN[08]	SSTL	I/O
G29	DDR3_ECC[0]	SSTL	I/O
G3	DDR3_DQ[56]	SSTL	I/O
G31	VSS	GND	
G33	DDR3_DQS_DN[02]	SSTL	I/O
G35	VSS	GND	
G37	VSS	GND	
G39	RSVD		
G41	VSS	GND	
G43	VSA	PWR	
G45	VSS	GND	
G47	VSS	GND	
G49	VSA	PWR	
G5	VSS	GND	
G51	VSS	GND	
G53	VSS	GND	
G55	PE1A_RX_DN[3]	PCIEX3	I
G57	VSS	GND	
G7	RSVD		
G9	VSS	GND	
H10	VSS	GND	
H12	VSS	GND	
H14	VSS	GND	
H16	VCCD_23	PWR	
H18	VCCD_23	PWR	
H2	DDR3_DQ[57]	SSTL	I/O
H20	VCCD_23	PWR	
H22	VCCD_23	PWR	
H24	VCCD_23	PWR	
H26	DDR3_ECC[7]	SSTL	I/O
H28	RSVD		
H30	DDR3_ECC[5]	SSTL	I/O
H32	VSS	GND	
H34	VSS	GND	

Table 8-2. Land Number (Sheet 38 of 45)

Land No.	Land Name	Buffer Type	Direction
H36	DDR3_DQ[15]	SSTL	I/O
H38	VSS	GND	
H4	DDR3_DQ[61]	SSTL	I/O
H40	VSS	GND	
H42	PE1A_TX_DP[0]	PCIEX3	O
H44	PE1A_TX_DP[2]	PCIEX3	O
H46	PE1B_TX_DP[4]	PCIEX3	O
H48	PE1B_TX_DP[6]	PCIEX3	O
H50	PE3A_TX_DP[0]	PCIEX3	O
H52	VSS	GND	
H54	VSS	GND	
H56	RSVD		
H58	RSVD		
H6	RSVD		
H8	VSS	GND	
J1	DDR_VREFDQRX_C23	DC	I
J11	VSS	GND	
J13	DDR3_DQ[40]	SSTL	I/O
J15	RSVD		
J17	DDR3_ODT[3]	SSTL	O
J19	DDR3_CS_N[1]	SSTL	O
J21	DDR3_CLK_DN[1]	SSTL	O
J23	DDR3_CLK_DN[0]	SSTL	O
J25	DDR3_CKE[2]	SSTL	O
J27	VSS	GND	
J29	DDR3_ECC[1]	SSTL	I/O
J3	RSVD		
J31	VSS	GND	
J33	VSS	GND	
J35	DDR3_DQ[11]	SSTL	I/O
J37	DDR3_DQS_DP[01]	SSTL	I/O
J39	VSS	GND	
J41	VSS	GND	
J43	PE1A_TX_DP[1]	PCIEX3	O
J45	PE1A_TX_DP[3]	PCIEX3	O
J47	PE1B_TX_DP[5]	PCIEX3	O
J49	PE1B_TX_DP[7]	PCIEX3	O
J5	VSS	GND	
J51	PE3A_TX_DP[1]	PCIEX3	O
J53	PE1B_RX_DP[4]	PCIEX3	I
J55	VSS	GND	
J57	PE1B_RX_DP[6]	PCIEX3	I
J7	DDR3_DQS_DN[06]	SSTL	I/O
J9	DDR3_DQ[42]	SSTL	I/O
K10	DDR3_DQ[46]	SSTL	I/O

Table 8-2. Land Number (Sheet 39 of 45)

Land No.	Land Name	Buffer Type	Direction
K12	RSVD		
K14	DDR3_DQ[44]	SSTL	I/O
K16	RSVD		
K18	DDR3_CS_N[4]	SSTL	O
K2	VSS	GND	
K20	DDR3_CLK_DP[2]	SSTL	O
K22	DDR3_CLK_DN[3]	SSTL	O
K24	DDR3_CKE[0]	SSTL	O
K26	VSS	GND	
K28	VSS	GND	
K30	VSS	GND	
K32	DDR3_DQ[29]	SSTL	I/O
K34	VSS	GND	
K36	DDR3_DQ[14]	SSTL	I/O
K38	RSVD		
K4	RSVD		
K40	DDR3_DQ[13]	SSTL	I/O
K42	PE1A_TX_DN[0]	PCIEX3	O
K44	PE1A_TX_DN[2]	PCIEX3	O
K46	PE1B_TX_DN[4]	PCIEX3	O
K48	PE1B_TX_DN[6]	PCIEX3	O
K50	PE3A_TX_DN[0]	PCIEX3	O
K52	PMSYNC	CMOS	I
K54	PE1B_RX_DP[5]	PCIEX3	I
K56	PE1B_RX_DP[7]	PCIEX3	I
K58	RSVD		
K6	DDR3_DQS_DP[06]	SSTL	I/O
K8	VSS	GND	
L1	DDR3_DQ[62]	SSTL	I/O
L11	DDR3_DQS_DN[05]	SSTL	I/O
L13	DDR3_DQ[41]	SSTL	I/O
L15	DRAM_PWR_OK_C23	CMOS1.5v	I
L17	DDR2_BA[1]	SSTL	O
L19	DDR3_ODT[0]	SSTL	O
L21	DDR3_CLK_DP[1]	SSTL	O
L23	DDR3_CLK_DP[0]	SSTL	O
L25	VSS	GND	
L27	DDR3_DQ[27]	SSTL	I/O
L29	VSS	GND	
L3	DDR3_DQS_DN[07]	SSTL	I/O
L31	DDR3_DQ[25]	SSTL	I/O
L33	DDR3_DQ[28]	SSTL	I/O
L35	DDR3_DQ[10]	SSTL	I/O
L37	DDR3_DQS_DN[01]	SSTL	I/O
L39	DDR3_DQ[09]	SSTL	I/O

Table 8-2. Land Number (Sheet 40 of 45)

Land No.	Land Name	Buffer Type	Direction
L41	VSS	GND	
L43	PE1A_TX_DN[1]	PCIEX3	O
L45	PE1A_TX_DN[3]	PCIEX3	O
L47	PE1B_TX_DN[5]	PCIEX3	O
L49	PE1B_TX_DN[7]	PCIEX3	O
L5	VSS	GND	
L51	PE3A_TX_DN[1]	PCIEX3	O
L53	PE1B_RX_DN[4]	PCIEX3	I
L55	PE2A_RX_DP[0]	PCIEX3	I
L57	PE1B_RX_DN[6]	PCIEX3	I
L7	DDR3_DQ[54]	SSTL	I/O
L9	DDR3_DQ[43]	SSTL	I/O
M10	DDR3_DQ[47]	SSTL	I/O
M12	RSVD		
M14	DDR3_DQ[45]	SSTL	I/O
M16	RSVD		
M18	RSVD		
M2	DDR3_DQ[63]	SSTL	I/O
M20	DDR3_CLK_DN[2]	SSTL	O
M22	DDR3_CLK_DP[3]	SSTL	O
M24	DDR3_CKE[1]	SSTL	O
M26	DDR3_DQ[31]	SSTL	I/O
M28	DDR3_DQ[26]	SSTL	I/O
M30	RSVD		
M32	DDR3_DQ[24]	SSTL	I/O
M34	VSS	GND	
M36	VSS	GND	
M38	RSVD		
M4	DDR3_DQS_DP[07]	SSTL	I/O
M40	DDR3_DQ[12]	SSTL	I/O
M42	VSS	GND	
M44	VSS	GND	
M46	VSS	GND	
M48	RSVD		
M50	VSS	GND	
M52	VSS	GND	
M54	PE1B_RX_DN[5]	PCIEX3	I
M56	PE1B_RX_DN[7]	PCIEX3	I
M6	DDR3_DQ[55]	SSTL	I/O
M8	VSS	GND	
N11	DDR3_DQS_DP[05]	SSTL	I/O
N13	VSS	GND	
N15	VCCD_23	PWR	
N17	VCCD_23	PWR	
N19	VCCD_23	PWR	

Table 8-2. Land Number (Sheet 41 of 45)

Land No.	Land Name	Buffer Type	Direction
N21	VCCD_23	PWR	
N23	VCCD_23	PWR	
N25	DDR3_CKE[3]	SSTL	O
N27	DDR3_DQ[30]	SSTL	I/O
N29	DDR3_DQS_DP[03]	SSTL	I/O
N3	DDR3_DQ[58]	SSTL	I/O
N31	RSVD		
N33	VSS	GND	
N35	VSS	GND	
N37	VSS	GND	
N39	DDR3_DQ[08]	SSTL	I/O
N41	VSS	GND	
N43	VSS	GND	
N45	VSA	PWR	
N47	VSS	GND	
N49	VSS	GND	
N5	VSS	GND	
N51	VSA	PWR	
N53	VSS	GND	
N55	PE2A_RX_DN[0]	PCIEX3	I
N7	DDR3_DQ[50]	SSTL	I/O
N9	VSS	GND	
P10	VSS	GND	
P12	VSS	GND	
P14	VSS	GND	
P16	DDR2_WE_N	SSTL	O
P18	DDR2_CS_N[5]	SSTL	O
P20	DDR2_MA[04]	SSTL	O
P22	DDR2_MA[07]	SSTL	O
P24	DDR2_BA[2]	SSTL	O
P26	VSS	GND	
P28	DDR3_DQS_DN[03]	SSTL	I/O
P30	VSS	GND	
P32	VSS	GND	
P34	DDR2_DQ[21]	SSTL	I/O
P36	DDR2_DQ[02]	SSTL	I/O
P38	VSS	GND	
P4	DDR3_DQ[59]	SSTL	I/O
P40	VSS	GND	
P42	DDR_VREFDQTX_C23	DC	O
P44	PE3D_TX_DN[15]	PCIEX3	O
P46	PE3C_TX_DP[8]	PCIEX3	O
P48	PE3A_TX_DP[3]	PCIEX3	O
P50	PE3B_TX_DP[6]	PCIEX3	O
P52	PE3B_TX_DP[4]	PCIEX3	O

Table 8-2. Land Number (Sheet 42 of 45)

Land No.	Land Name	Buffer Type	Direction
P54	VSS	GND	
P56	VSS	GND	
P6	DDR3_DQ[51]	SSTL	I/O
P8	VSS	GND	
R11	VSS	GND	
R13	DDR2_DQ[48]	SSTL	I/O
R15	DDR2_MA[13]	SSTL	O
R17	DDR2_BA[0]	SSTL	O
R19	DDR2_MA[01]	SSTL	O
R21	DDR2_MA[06]	SSTL	O
R23	DDR2_MA[09]	SSTL	O
R25	RSVD		
R27	RSVD		
R29	VSS	GND	
R3	VSS	GND	
R31	VSS	GND	
R33	DDR2_DQ[17]	SSTL	I/O
R35	VSS	GND	
R37	DDR2_DQ[06]	SSTL	I/O
R39	VSS	GND	
R41	DDR2_DQ[04]	SSTL	I/O
R43	DDR_SDA_C23	ODCMOS	I/O
R45	PE3C_TX_DP[10]	PCIEX3	O
R47	PE3A_TX_DP[2]	PCIEX3	O
R49	PE3B_TX_DP[7]	PCIEX3	O
R5	VSS	GND	
R51	PE3B_TX_DP[5]	PCIEX3	O
R53	PRDY_N	CMOS	O
R55	VSS	GND	
R7	VSS	GND	
R9	DDR2_DQ[54]	SSTL	I/O
T10	DDR2_DQ[50]	SSTL	I/O
T12	RSVD		
T14	DDR2_DQ[52]	SSTL	I/O
T16	DDR2_CAS_N	SSTL	O
T18	DDR2_MA[10]	SSTL	O
T20	DDR2_MA[03]	SSTL	O
T22	DDR2_MA[08]	SSTL	O
T24	DDR2_MA[12]	SSTL	O
T26	DDR2_CKE[1]	SSTL	O
T28	VSS	GND	
T30	DDR2_DQ[23]	SSTL	I/O
T32	RSVD		
T34	DDR2_DQ[20]	SSTL	I/O
T36	DDR2_DQ[03]	SSTL	I/O

Table 8-2. Land Number (Sheet 43 of 45)

Land No.	Land Name	Buffer Type	Direction
T38	DDR2_DQS_DN[00]	SSTL	I/O
T4	VSS	GND	
T40	DDR2_DQ[00]	SSTL	I/O
T42	VSS	GND	
T44	PE3D_TX_DP[15]	PCIEX3	O
T46	PE3C_TX_DN[8]	PCIEX3	O
T48	PE3A_TX_DN[3]	PCIEX3	O
T50	PE3B_TX_DN[6]	PCIEX3	O
T52	PE3B_TX_DN[4]	PCIEX3	O
T54	PE2A_RX_DP[1]	PCIEX3	I
T56	PE2A_RX_DP[2]	PCIEX3	I
T6	VSS	GND	
T8	VSS	GND	
U11	DDR2_DQS_DN[06]	SSTL	I/O
U13	DDR2_DQ[49]	SSTL	I/O
U15	DDR23_RCOMP[0]	Analog	I
U17	DDR2_RAS_N	SSTL	O
U19	DDR2_MA[02]	SSTL	O
U21	DDR2_MA[05]	SSTL	O
U23	DDR2_MA[11]	SSTL	O
U25	DDR2_MA[15]	SSTL	O
U27	DDR2_CKE[2]	SSTL	O
U29	DDR2_DQ[19]	SSTL	I/O
U3	DDR2_DQ[60]	SSTL	I/O
U31	DDR2_DQS_DP[02]	SSTL	I/O
U33	DDR2_DQ[16]	SSTL	I/O
U35	VSS	GND	
U37	DDR2_DQ[07]	SSTL	I/O
U39	RSVD		
U41	DDR2_DQ[05]	SSTL	I/O
U43	DDR_SCL_C23	ODCMOS	I/O
U45	PE3C_TX_DN[10]	PCIEX3	O
U47	PE3A_TX_DN[2]	PCIEX3	O
U49	PE3B_TX_DN[7]	PCIEX3	O
U5	VSS	GND	
U51	PE3B_TX_DN[5]	PCIEX3	O
U53	PREQ_N	CMOS	I/O
U55	PE2A_RX_DP[3]	PCIEX3	I
U7	DDR2_DQ[44]	SSTL	I/O
U9	DDR2_DQ[55]	SSTL	I/O
V10	DDR2_DQ[51]	SSTL	I/O
V12	RSVD		
V14	DDR2_DQ[53]	SSTL	I/O
V16	VCCD_23	PWR	
V18	VCCD_23	PWR	

Table 8-2. Land Number (Sheet 44 of 45)

Land No.	Land Name	Buffer Type	Direction
V20	VCCD_23	PWR	
V22	VCCD_23	PWR	
V24	VCCD_23	PWR	
V26	VSS	GND	
V28	VSS	GND	
V30	DDR2_DQ[22]	SSTL	I/O
V32	RSVD		
V34	VSS	GND	
V36	VSS	GND	
V38	DDR2_DQS_DP[00]	SSTL	I/O
V4	DDR2_DQ[61]	SSTL	I/O
V40	DDR2_DQ[01]	SSTL	I/O
V42	VSS	GND	
V44	VSS	GND	
V46	VSS	GND	
V48	VSS	GND	
V50	VSS	GND	
V52	RSVD		
V54	PE2A_RX_DN[1]	PCIEX3	I
V56	PE2A_RX_DN[2]	PCIEX3	I
V6	DDR2_DQ[40]	SSTL	I/O
V8	VSS	GND	
W11	DDR2_DQS_DP[06]	SSTL	I/O
W13	VSS	GND	
W15	RSVD		
W17	RSVD		
W19	DDR2_ODT[1]	SSTL	O
W21	DDR2_CLK_DN[2]	SSTL	O
W23	DDR2_CLK_DN[3]	SSTL	O
W25	DDR2_MA[14]	SSTL	O
W27	DDR2_ECC[6]	SSTL	I/O
W29	DDR2_DQ[18]	SSTL	I/O
W3	DDR2_DQ[56]	SSTL	I/O
W31	DDR2_DQS_DN[02]	SSTL	I/O
W33	VSS	GND	
W35	DDR2_DQ[29]	SSTL	I/O
W37	VSS	GND	
W39	RSVD		
W41	VSS	GND	
W43	VSS	GND	
W45	VSS	GND	
W47	VSS	GND	
W49	VTTA	PWR	
W5	VSS	GND	
W51	VSS	GND	

Table 8-2. Land Number (Sheet 45 of 45)

Land No.	Land Name	Buffer Type	Direction
W53	VSS	GND	
W55	PE2A_RX_DN[3]	PCIEX3	I
W7	DDR2_DQ[45]	SSTL	I/O
W9	VSS	GND	
Y10	VSS	GND	
Y12	VSS	GND	
Y14	DDR23_RCOMP[2]	Analog	I
Y16	RSVD		
Y18	DDR2_ODT[3]	SSTL	O
Y20	DDR2_ODT[0]	SSTL	O
Y22	DDR2_CLK_DN[1]	SSTL	O
Y24	DDR2_CLK_DN[0]	SSTL	O
Y26	DDR2_ECC[2]	SSTL	I/O
Y28	VSS	GND	
Y30	VSS	GND	
Y32	VSS	GND	
Y34	RSVD		
Y36	VSS	GND	
Y38	VSS	GND	
Y4	DDR2_DQ[57]	SSTL	I/O
Y40	VSS	GND	
Y42	VSS	GND	
Y44	PE3D_TX_DP[13]	PCIEX3	O
Y46	PE3C_TX_DP[11]	PCIEX3	O
Y48	RSVD		
Y50	PE3B_RX_DP[4]	PCIEX3	I
Y52	PE3B_RX_DP[5]	PCIEX3	I
Y54	VTTA	PWR	
Y56	VSS	GND	
Y6	DDR2_DQ[41]	SSTL	I/O
Y8	RSVD		

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9 Package Mechanical Specifications

For mechanical specifications and design guidelines refer to the *Intel® Core™ i7 Processor Family for the LGA-2011 Socket Thermal Mechanical Specification and Design Guide*.

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