

Features

- **MPEG/II-Layer 3 Hardwired Decoder**
 - Stand-alone MP3 Decoder
 - 48, 44.1, 32, 24, 22.05, 16 kHz Sampling Frequency
 - Separated Digital Volume Control on Left and Right Channels (Software Control using 31 Steps)
 - Bass, Medium, and Treble Control (31 Steps)
 - Bass Boost Sound Effect
 - Ancillary Data Extraction
 - CRC Error and MPEG Frame Synchronization Indicators
- **Programmable Audio Output for Interfacing With Common Audio DAC**
 - PCM Format Compatible
 - I²S Format Compatible
- **8-bit MCU C51 Core Based (F_{MAX} = 20 MHz)**
- **2304 bytes of Internal RAM**
- **64K bytes of Code Memory**
 - Flash: AT89C51SND1A, ROM: AT83C51SND1A
- **4K bytes of Boot Flash Memory (AT89C51SND1A)**
 - ISP: Download from USB or UART to any External Memory Cards
- **USB Rev 1.1 Controller**
 - Full Speed Data Transmission
- **Built-in PLL**
 - MP3 Audio Clocks
 - USB Clock
- **MultiMediaCard™ Interface Compatibility**
- **Atmel DataFlash® SPI Interface Compatibility**
- **IDE/ATAPI Interface**
- **2 Channels 10-bit ADC, 8 kHz (8 true bit)**
 - Battery Voltage Monitoring
 - Voice Recording Controlled by Software
- **Up to 44 bits of General-purpose I/Os for:**
 - 4-bit Interrupt Keyboard Port for a 4 x n Matrix
 - Smartmedia® Software Interface
- **Two Standard 16-bit Timers/Counters**
- **Hardware Watchdog Timer**
- **Standard Full Duplex UART with Baud Rate Generator**
- **Two-wire Master and Slave Modes Controller**
- **SPI Master and Slave Modes Controller**
- **Power Management**
 - Power-on reset
 - Software Programmable MCU Clock
 - Idle Mode, Power-down Mode
- **Operating Conditions:**
 - 3V, ±10%, 25 mA Typical Operating at 25°C
 - Temperature Range: -40°C to +85°C
- **Packages**
 - TQFP80, PLCC84 (Development Board)
 - Dice

Description

The AT8xC51SND1A is a fully integrated stand-alone hardwired MPEG/II-Layer 3 decoder with a C51 microcontroller core handling data flow and MP3-player control.

The AT89C51SND1A includes 64K bytes of Flash memory and allows In-System Programming through an embedded 4K bytes of Boot Flash Memory.



Single Chip Flash with MP3 Decoder and Man Machine Interface

AT8xC51SND1A Design Guide

Preliminary

Rev. 4109C-8051-03/02





The AT83C51SND1A includes 64K bytes of ROM memory.

The AT8xC51SND1A includes 2304 bytes of RAM memory.

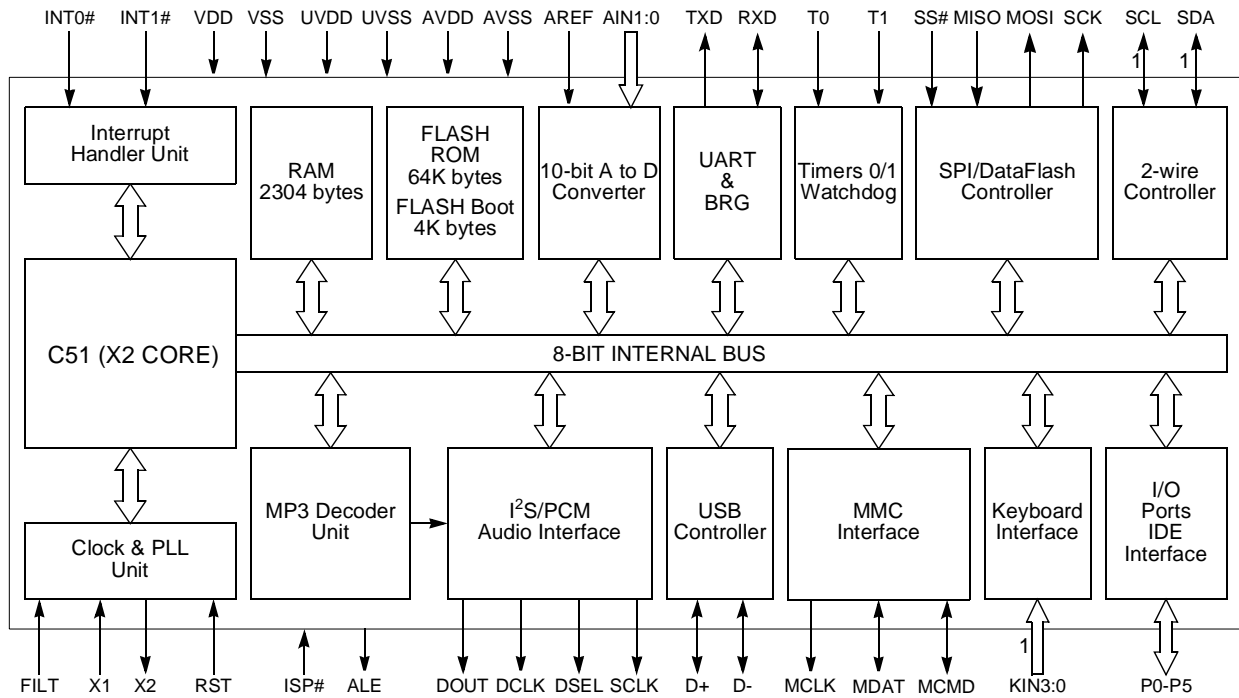
The AT8xC51SND1A provides all necessary features for man machine interface like timers, keyboard port, serial or parallel interface (USB, two-wire, SPI, IDE), ADC input, I²S output, and all external memory interface (NAND or NOR Flash, SmartMedia, MultiMedia).

Typical Applications

- MP3-Player
- PDA, Camera, Mobile Phone MP3
- Car Audio/Multimedia MP3
- Home Audio/Multimedia MP3

Block Diagram

Figure 1. AT8xC51SND1A Block Diagram



1 Alternate function of Port 1

2 Alternate function of Port 3

3 Alternate function of Port 4

Clock Controller

The AT8xC51SND1A clock controller is based on an on-chip oscillator feeding an on-chip Phase Lock Loop (PLL). All internal clocks to the peripherals and CPU core are generated by this controller.

Oscillator

The AT8xC51SND1A X1 and X2 pins are the input and the output of a single-stage on-chip inverter (see Figure 2), that can be configured with off-chip components such as a Pierce oscillator (see Figure 3). Value of capacitors and crystal characteristics are detailed in the Section “DC Characteristics” of the AT8xC51SND1A datasheet.

The oscillator outputs three different clocks: a clock for the PLL, a clock for the CPU core, and a clock for the peripherals symbolized as shown in Figure 2. These clocks are either enabled or not enabled, depending on the power reduction mode as detailed in “Power Management” on page 41. The peripheral clock is used to generate the Timer 0, Timer 1, MMC, ADC, SPI, and Port sampling clocks.

Figure 2. Oscillator Block Diagram and Symbol

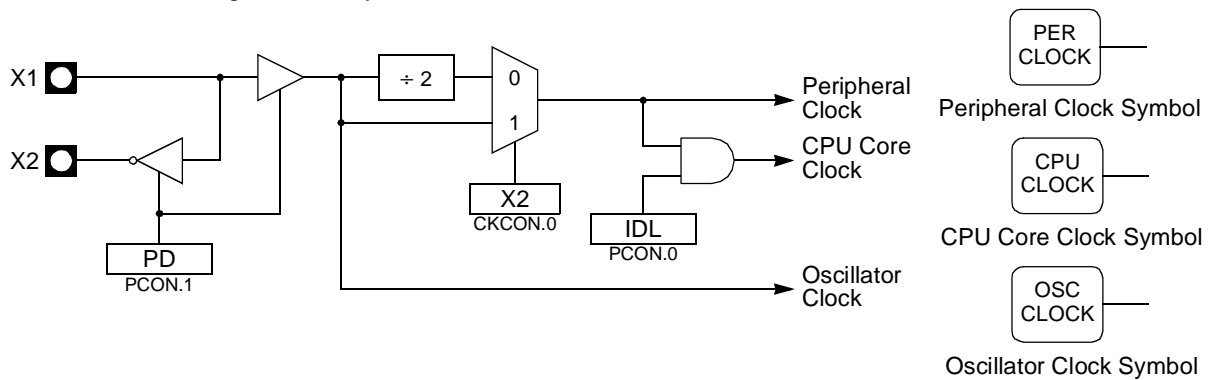
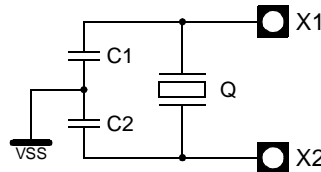


Figure 3. Crystal Connection

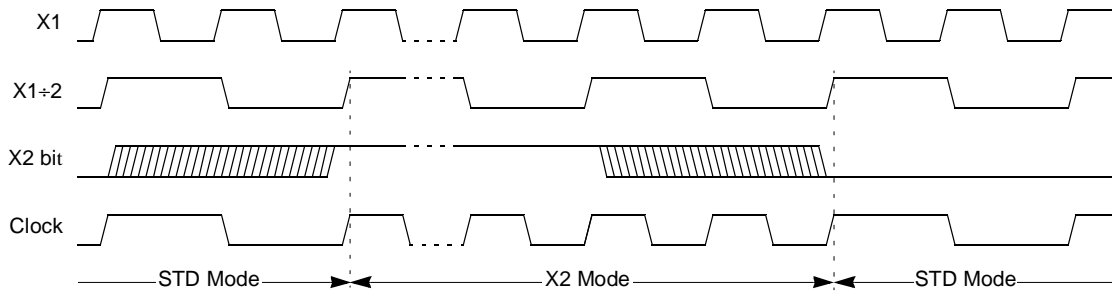


X2 Feature

Unlike standard C51 products that require 12 oscillator clock periods per machine cycle, the AT8xC51SND1A needs only 6 oscillator clock periods per machine cycle. This feature called the “X2 feature” can be enabled using the X2 bit⁽¹⁾ in CKCON (see Table 1) and allows the AT8xC51SND1A to operate in 6 or 12 oscillator clock periods per machine cycle. As shown in Figure 2, both CPU and peripheral clocks are affected by this feature. Figure 4 shows the X2 mode switching waveforms. After reset the standard mode is activated. In standard mode the CPU and peripheral clock frequency is the oscillator frequency divided by 2 while in X2 mode, it is the oscillator frequency.

Note: 1. The X2 bit reset value depends on the X2B bit in the Hardware Byte (see Table 6 on page 15). Using the AT89C51SND1A (Flash Version) the system can boot either in standard or X2 mode depending on the X2B value. Using AT83C51SND1A (ROM Version) the system always boots in standard mode. X2B bit can be changed to X2 mode later by software.

Figure 4. Mode Switching Waveforms



Note: In order to prevent any incorrect operation while operating in X2 mode, you must be aware that all peripherals using clock frequency as time reference (timers...) will have their time reference divided by two. For example, a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms.

PLL

PLL Description

The AT8xC51SND1A PLL is used to generate internal high frequency clock (the PLL Clock) synchronized with an external low-frequency (the Oscillator Clock). The PLL clock provides the MP3 decoder, the audio interface, and the USB interface clocks. Figure 5 shows the internal structure of the PLL.

The PFLD block is the Phase Frequency Comparator and Lock Detector. This block makes the comparison between the reference clock coming from the N divider and the reverse clock coming from the R divider and generates some pulses on the Up or Down signal depending on the edge position of the reverse clock. The PLEN bit in PLLCON register is used to enable the clock generation. When the PLL is locked, the bit PLOCK in PLLCON register (see Table 2) is set.

The CHP block is the Charge Pump that generates the voltage reference for the VCO by injecting or extracting charges from the external filter connected on PFILT pin (see Figure 6). Value of the filter components are detailed in the Section “DC Characteristics” of the AT8xC51SND1A datasheet.

The VCO block is the Voltage Controlled Oscillator controlled by the voltage V_{ref} produced by the charge pump. It generates a square wave signal: the PLL clock.

Figure 5. PLL Block Diagram and Symbol

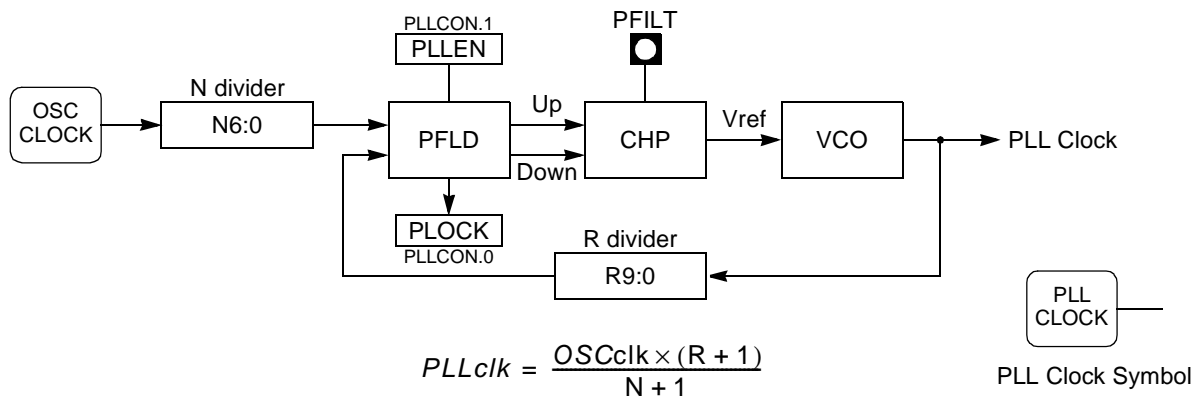
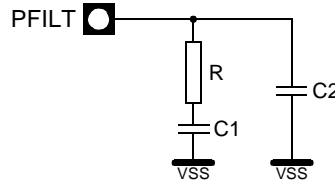


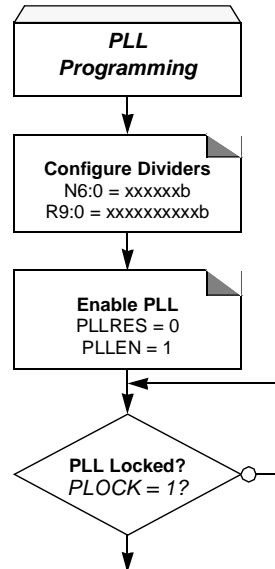
Figure 6. PLL Filter Connection



PLL Programming

The PLL is programmed using the flow shown in Figure 7. As soon as clock generation is enabled, you must wait until the lock indicator is set to ensure the clock output is stable. The PLL clock frequency will depend on MP3 decoder clock and audio interface clock frequencies.

Figure 7. PLL Programming Flow



Registers

Table 1. CKCON Register

CKCON (S:8Fh) – Clock Control Register

7	6	5	4	3	2	1	0
-	WDX2	-	-	-	T1X2	T0X2	X2

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	WDX2	Watchdog Clock Control Bit Set to select the oscillator clock divided by two as watchdog clock input (X2 independent). Clear to select the peripheral clock as watchdog clock input (X2 dependent).
5-3	-	Reserved The value read from these bits is indeterminate. Do not set these bits.
2	T1X2	Timer 1 Clock Control Bit Set to select the oscillator clock divided by two as timer 1 clock input (X2 independent). Clear to select the peripheral clock as timer 1 clock input (X2 dependent).
1	T0X2	Timer 0 Clock Control Bit Set to select the oscillator clock divided by two as timer 0 clock input (X2 independent). Clear to select the peripheral clock as timer 0 clock input (X2 dependent).
0	X2	System Clock Control Bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{CPU} = F_{PER} = F_{OSC}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{CPU} = F_{PER} = F_{OSC}$).

Reset Value = 0000 000Xb

Table 2. PLLCON Register

PLLCON (S:E9h) – PLL Control Register.

	7	6	5	4	3	2	1	0
	R1	R0	-	-	PLLRES	-	PLLEN	PLOCK

Bit Number	Bit Mnemonic	Description
7-6	R1:0	PLL Least Significant Bits R Divider 2 LSB of the 10-bit R divider.
5-4	-	Reserved The value read from these bits is always 0. Do not set these bits.
3	PLLRES	PLL Reset Bit Set this bit to reset the PLL. Clear this bit to free the PLL and allow enabling.
2	-	Reserved The value read from this bit is always 0. Do not set this bit.
1	PLLEN	PLL Enable Bit Set to enable the PLL. Clear to disable the PLL.
0	PLOCK	PLL Lock Indicator Set by hardware when PLL is locked. Clear by hardware when PLL is unlocked.

Reset Value = 0000 1000b

Table 3. PLLNDIV Register

PLLNDIV (S:EEh) – PLL N Divider Register.

	7	6	5	4	3	2	1	0
	-	N6	N5	N4	N3	N2	N1	N0

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is always 0. Do not set this bit.
6-0	N6:0	PLL N Divider 7-bit N divider.

Reset Value = 0000 0000b

Table 4. PLLRDIV Register

PLLRDIV (S:EFh) – PLL R Divider Register

7	6	5	4	3	2	1	0
R9	R8	R7	R6	R5	R4	R3	R2
Bit Number	Bit Mnemonic	Description					
7 - 0	R9:2	PLL Most Significant Bits R Divider 8 MSB of the 10-bit R divider.					

Reset Value = 0000 0000b

Program/Code Memory

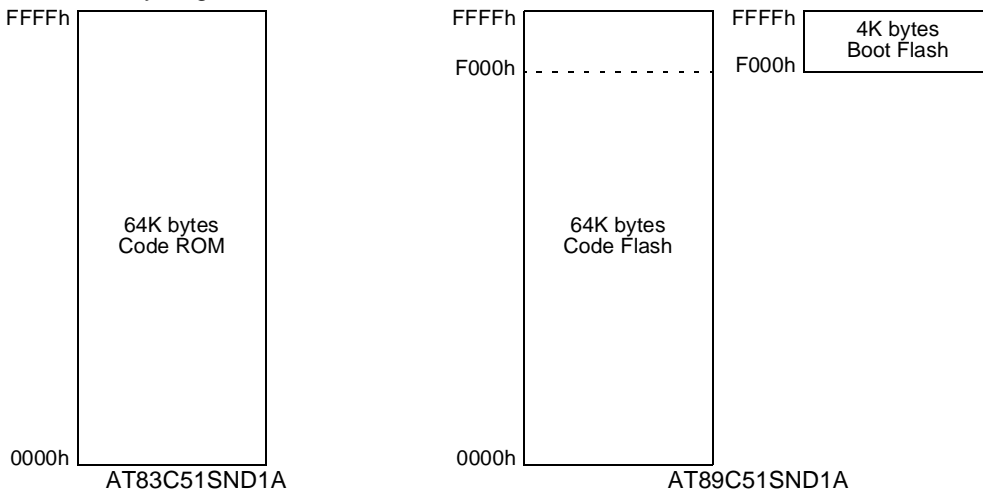
The AT89C51SND1A and AT83C51SND1A implement 64K bytes of on-chip program/code memory. Figure 8 shows the split of internal and external program/code memory spaces depending on the product.

The AT83C51SND1A product provides the internal program/code memory in ROM memory while the AT89C51SND1A product provides it in Flash memory. These two products do not allow external code memory execution.

The Flash memory increases EPROM and ROM functionality by in-circuit electrical erasure and programming. The high voltage needed for programming or erasing Flash cells is generated on-chip using the standard VDD voltage, made possible by the internal charge pump. Thus, the AT89C51SND1A can be programmed using only one voltage and allows in application software programming. Hardware programming mode is also available using common programming tool.

The AT89C51SND1A implements an additional 4K bytes of on-chip boot Flash memory provided in Flash memory. This boot memory is delivered programmed with a standard boot loader software allowing In-System Programming (ISP). It also contains some Application Programming Interfaces routines named API routines allowing In Application Programming (IAP) by using user's own boot loader.

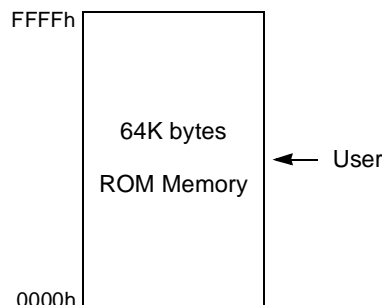
Figure 8. Program/Code Memory Organization



ROM Memory Architecture

As shown in Figure 9 the AT83C51SND1A ROM memory is composed of two spaces detailed in the following paragraphs.

Figure 9. ROM Memory Architecture



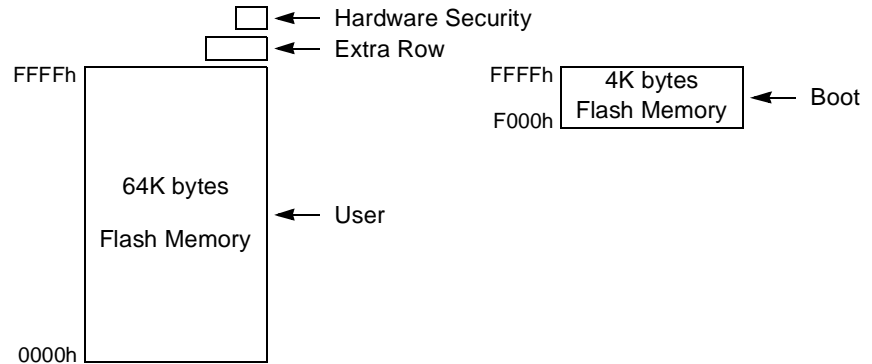
User Space

This space is composed of a 64K bytes ROM memory programmed during the manufacturing process. It contains you's application code.

Flash Memory Architecture

As shown in Figure 1 the AT89C51SND1A Flash memory is composed of four spaces detailed in the following paragraphs.

Figure 1. Flash Memory Architecture



User Space

This space is composed of a 64K bytes Flash memory organized in 512 pages of 128 bytes. It contains you's application code.

This space can be read or written by both software and hardware modes.

Boot Space

This space is composed of a 4K bytes Flash memory. It contains the boot loader for In-System Programming and the routines for In Application Programming.

This space can only be read or written by hardware mode using a parallel programming tool.

Hardware Security Space

This space is composed of one byte: the Hardware Security Byte (HSB see Table 6) divided in two separate nibbles. The MSN contains the X2 mode configuration bit and the Boot Loader Jump Bit as detailed in Section and can be written by software while the LSN contains the lock system level to protect the memory content against piracy as detailed in Section and can only be written by hardware.

Extra Row Space

This space is composed of two bytes:

- the Software Boot Vector (SBV see Table 7).
This byte is used by the software boot loader to build the boot address.
- the Software Security Byte (SSB see Figure).
This byte is used to lock the execution of some boot loader commands.

Hardware Security System

The AT89C51SND1A implements three lock bits LB2:0 in the LSN of HSB (see Table 6) providing three levels of security for user's program as described in Table 5 while the AT83C51SND1A is always set in read disabled mode.

Level 0 is the level of an erased part and does not enable any security feature.

Level 1 locks the hardware programming of both user and boot memories.

Level 2 locks also hardware verifying of both user and boot memories

Level 3 locks also the external execution.

Table 5. Lock Bits Features

Level	LB2 ²	LB1	LB0	Internal Execution	External Execution	Hardware Verifying	Hardware Programming	Software Programming
0	U	U	U	Enable	Enable	Enable	Enable	Enable
1	U	U	P	Enable	Enable	Enable	Disable	Enable
2	U	P	X	Enable	Enable	Disable	Disable	Enable
3 ³	P	X	X	Enable	Disable	Disable	Disable	Enable

Notes: 1. U means unprogrammed, P means programmed and X means don't care (programmed or unprogrammed).

2. LB2 is not implemented in the T8xC51SND1 products.

3. AT89C51SND1A products are delivered with third level programmed to ensure that the code programmed by software using ISP or user's boot loader being secured from any hardware piracy.

Boot Memory Execution

As internal C51 code space is limited to 64K bytes, some mechanisms are implemented to allow boot memory to be mapped in the code space for execution at addresses from F000h to FFFFh. The boot memory is enabled by setting the ENBOOT bit in AUXR1 (see Figure 2). The three ways to set this bit are detailed in the following sections.

Software Boot Mapping

The software way to set ENBOOT consists in writing to AUXR1 from you's software. This enables boot loader or API routines execution.

Hardware Condition Boot Mapping

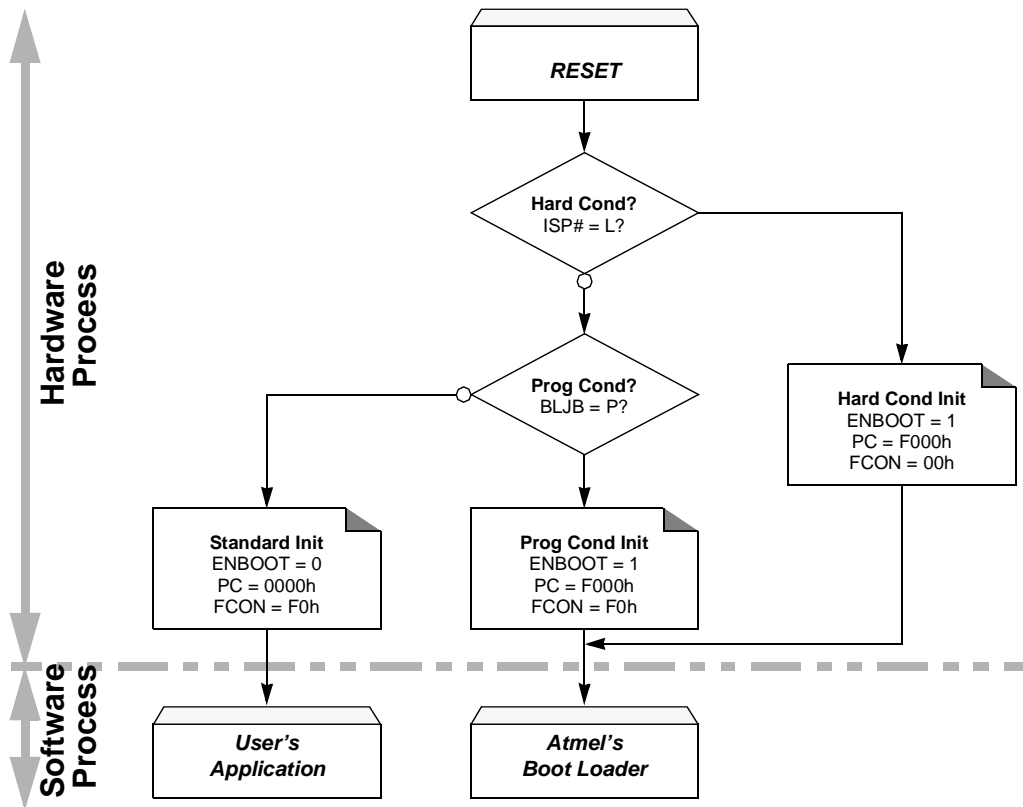
The hardware condition is based on the ISP# pin. When driving this pin to low level, the chip reset sets ENBOOT and forces the reset vector to F000h instead of 0000h in order to execute the boot loader software.

As shown in Figure 10 the hardware condition always allows in-system recovery when user's memory has been corrupted.

Programmed Condition Boot Mapping

The programmed condition is based on the Boot Loader Jump Bit (BLJB) in HSB. As shown in Figure 10 when this bit is programmed (by hardware or software programming mode), the chip reset set ENBOOT and forces the reset vector to F000h instead of 0000h, in order to execute the boot loader software.

Figure 10. Hardware Boot Process Algorithm



The software process (boot loader) is detailed in the section “In System and In-Application Programming” of the AT8xC51SND1A datasheet.

Preventing Flash Corruption

See “Reset Recommendation to Prevent Flash Corruption” on page 41 in the section Power Management.

Registers

Figure 2. AUXR1 Register
AUXR1 (S:A2h) – Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	ENBOOT	-	GF3	0	-	DPS

Table 4.

Bit Number	Bit Mnemonic	Description
7 - 6	-	Reserved The value read from these bits are indeterminate. Do not set these bits.
5	ENBOOT	Enable Boot Flash Set this bit to map the boot flash in the code space between at addresses F000h to FFFFh. Clear this bit to disable boot flash.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	GF3	General Flag This bit is a general-purpose user flag.
2	0	Always Zero This bit is stuck to logic 0 to allow INC AUXR1 instruction without affecting GF3 flag.
1	-	Reserved for Data Pointer Extension.
0	DPS	Data Pointer Select Bit Set to select second data pointer: DPTR1. Clear to select first data pointer: DPTR0.

Reset Value = XXXX 00X0b

Hardware Bytes

Table 6. HSB Byte – Hardware Security Byte

7	6	5	4	3	2	1	0
X2B	BLJB	-	-	-	LB2	LB1	LB0

Table 5.

Bit Number	Bit Mnemonic	Description
7	X2B ¹	X2 Bit Program this bit to start in X2 mode. Unprogram (erase) this bit to start in standard mode.
6	BLJB	Boot Loader Jump Bit Program this bit to execute the boot loader at address F000h on next reset. Unprogram (erase) this bit to execute user's application at address 0000h on next reset.
5 - 4	-	Reserved The value read from these bits is always unprogrammed. Do not program these bits.
3		Reserved The value read from this bit is always unprogrammed. Do not program this bit.
2 - 0	LB2:0	Hardware Lock Bits Refer to Table 5 for bits description.

Reset Value = XXUU UXXX, UUUU UUUU after an hardware full chip erase.

- Note:
1. X2B initializes the X2 bit in CKCON during the reset phase.
 2. Bits 0 to 3 (MSN) can only be programmed by hardware mode.

Table 7. SBV Byte – Software Boot Vector

7	6	5	4	3	2	1	0
ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8

Table 3.

Bit Number	Bit Mnemonic	Description
7 - 0	ADD15:8	MSB of you's boot loader 16-bit address location Refer to the AT8xC51SND1A datasheet for usage information (boot loader dependent).

Reset Value = XXXX XXXX, UUUU UUUU after an hardware full chip erase.

Table 8. SSB Byte – Software Security Byte

7	6	5	4	3	2	1	0
SSB7	SSB6	SSB5	SSB4	SSB3	SSB2	SSB1	SSB0

Table 4.

Bit Number	Bit Mnemonic	Description
7 - 0	SSB7:0	Software Security Byte Data Refer to the AT8xC51SND1A datasheet for usage information (boot loader dependent).



Reset Value = XXXX XXXX, UUUU UUUU after an hardware full chip erase.

Data Memory

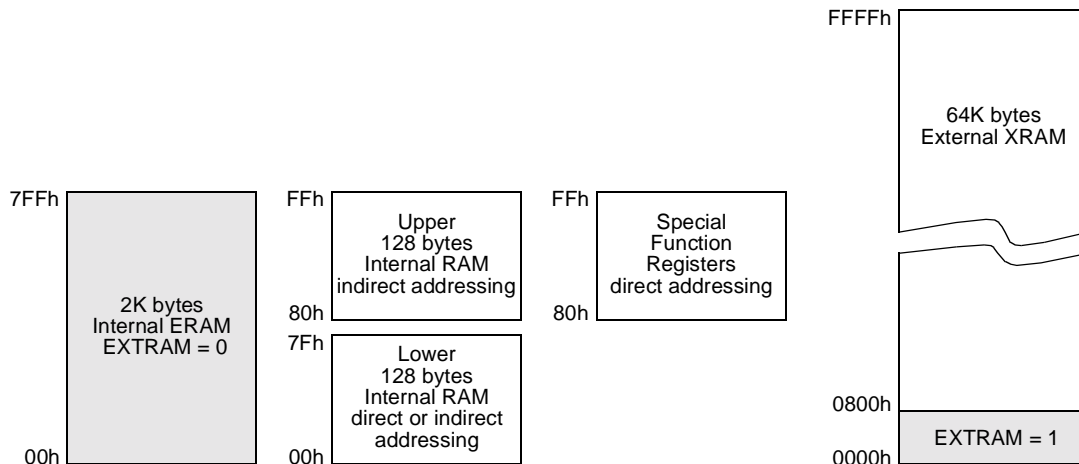
The AT8xC51SND1A provides data memory access in two different spaces:

1. The internal space mapped in three separate segments:
 - the lower 128 bytes RAM segment
 - the upper 128 bytes RAM segment
 - the expanded 2048 bytes RAM segment
2. The external space.

A fourth internal segment is available but dedicated to Special Function Registers, SFRs, (addresses 80h to FFh) accessible by direct addressing mode. For information on this segment, refer to the Section “Special Function Registers”, page 24.

Figure 11 shows the internal and external data memory spaces organization.

Figure 11. Internal and External Data Memory Organization



Internal Space

Lower 128 Bytes RAM

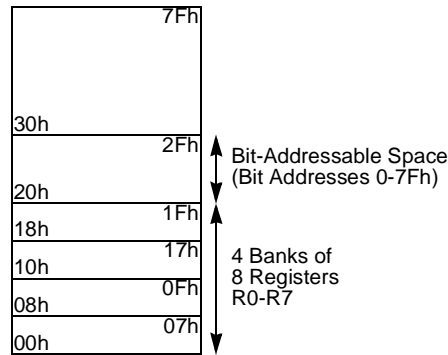
The lower 128 bytes of RAM (see Figure 3) are accessible from address 00h to 7Fh using direct or indirect addressing modes. The lowest 32 bytes are grouped into 4 banks of 8 registers (R0 to R7). Two bits RS0 and RS1 in PSW register (see Table 12) select which bank is in use according to Table 9. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing, and can be used for context switching in interrupt service routines.

Table 9. Register Bank Selection

RS1	RS0	Description
0	0	Register bank 0 from 00h to 07h
0	1	Register bank 1 from 08h to 0Fh
1	0	Register bank 2 from 10h to 17h
1	1	Register bank 3 from 18h to 1Fh

The next 16 bytes above the register banks form a block of bit-addressable memory space. The C51 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00h to 7Fh.

Figure 3. Lower 128 bytes Internal RAM Organization



Upper 128 Bytes RAM

The upper 128 bytes of RAM are accessible from address 80h to FFh using only indirect addressing mode.

Expanded RAM

The on-chip 2Kbytes of expanded RAM (ERAM) are accessible from address 0000h to 07FFh using indirect addressing mode through MOVX instructions. In this address range, EXTRAM bit in AUXR register (see Table 13) is used to select the ERAM (default) or the XRAM. As shown in Figure 11 when EXTRAM = 0, the ERAM is selected and when EXTRAM = 1, the XRAM is selected (see Section). The ERAM memory can be resized using XRS1:0 bits in AUXR register to dynamically increase external access to the XRAM space. Table 10 details the selected ERAM size and address range.

Table 10. ERAM Size Selection

XRS1	XRS0	ERAM Size	Address
0	0	256 bytes	0 to 00FFh
0	1	512 bytes	0 to 01FFh
1	0	1K bytes	0 to 03FFh
1	1	2K bytes	0 to 07FFh

Note: Lower 128 bytes RAM, Upper 128 bytes RAM, and expanded RAM are made of volatile memory cells. This means that the RAM content is indeterminate after power-up and must then be initialized properly.

External Space

Memory Interface

The external memory interface comprises the external bus (port 0 and port 2) as well as the bus control signals (RD#, WR#, and ALE).

Figure 4 shows the structure of the external address bus. P0 carries address A7:0 while P2 carries address A15:8. Data D7:0 is multiplexed with A7:0 on P0. Table 11 describes the external memory interface signals.

Figure 4. External Data Memory Interface Structure

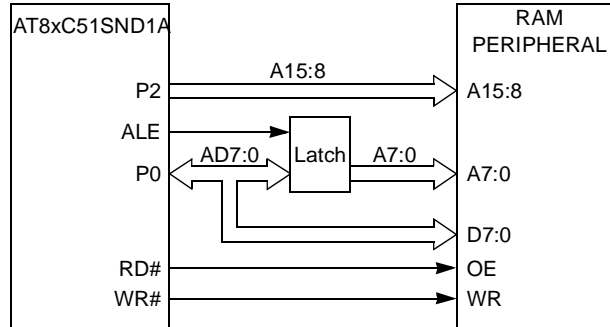


Table 11. External Data Memory Interface Signals

Signal Name	Type	Description	Alternate Function
A15:8	O	Address Lines Upper address lines for the external bus.	P2.7:0
AD7:0	I/O	Address/Data Lines Multiplexed lower address lines and data for the external memory.	P0.7:0
ALE	O	Address Latch Enable ALE signals indicates that valid address information are available on lines AD7:0.	-
RD#	O	Read Read signal output to external data memory.	P3.7
WR#	O	Write Write signal output to external memory.	P3.6

Page Access Mode

The AT8xC51SND1A implements a feature called Page Access that disables the output of DPH on P2 when executing MOVX @DPTR instruction. Page Access is enable by setting the DPHDIS bit in AUXR register.

Page Access is useful when application uses both ERAM and 256 bytes of XRAM. In this case, software modifies intensively EXTRAM bit to select access to ERAM or XRAM and must save it if used in interrupt service routine. Page Access allows external access above 00FFh address without generating DPH on P2. Thus ERAM is accessed using MOVX @Ri or MOVX @DPTR with DPTR < 0100h, and XRAM is accessed using MOVX @DPTR with DPTR ≥ 0100h while keeping P2 for general I/O usage.

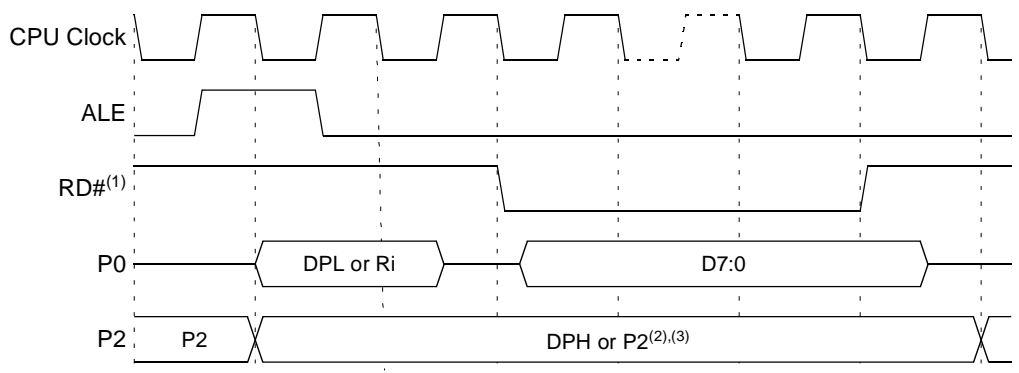
External Bus Cycles

This section describes the bus cycles the AT8xC51SND1A executes to read (see Figure 5), and write data (see Figure 6) in the external data memory. External memory cycle takes 6 CPU clock periods. This is equivalent to 12 oscillator clock period in standard mode or 6 oscillator clock periods in X2 mode. For further information on X2 mode, refer to the Section “X2 Feature”, page 4.

Slow peripherals can be accessed by stretching the read and write cycles. This is done using the M0 bit in AUXR register. Setting this bit changes the width of the RD# and WR# signals from 3 to 15 CPU clock periods.

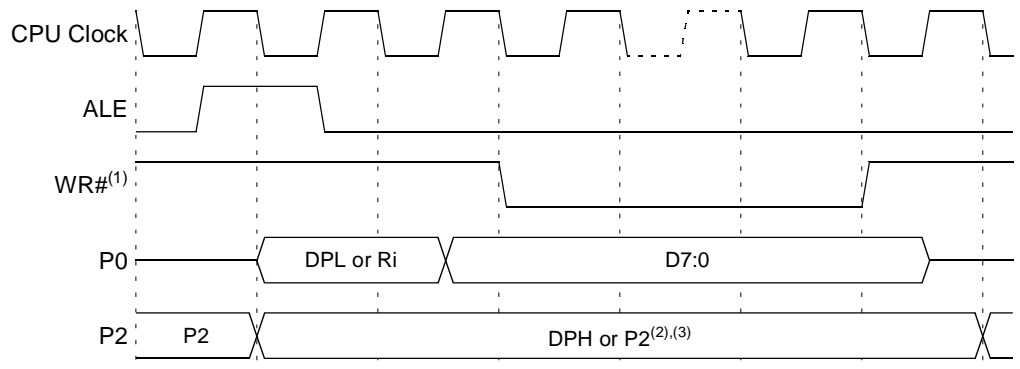
For simplicity, the accompanying figures depict the bus cycle waveforms in idealized form and do not provide precise timing information. For bus cycle timing parameters refer to the Section “AC Characteristics” of the AT8xC51SND1A datasheet.

Figure 5. External Data Read Waveforms



- Notes:
1. RD# signal may be stretched using M0 bit in AUXR register.
 2. When executing MOVX @Ri instruction, P2 outputs SFR content.
 3. When executing MOVX @DPTR instruction, if DPHDIS is set (Page Access Mode), P2 outputs SFR content instead of DPH.

Figure 6. External Data Write Waveforms



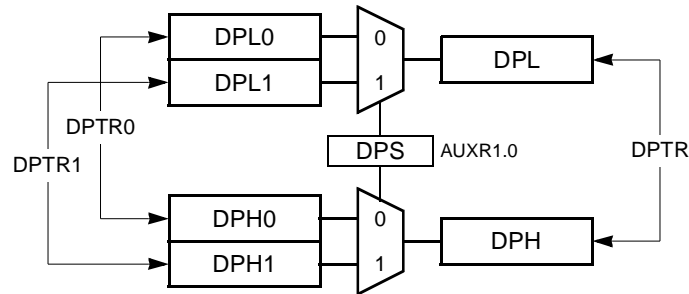
- Notes:
1. WR# signal may be stretched using M0 bit in AUXR register.
 2. When executing MOVX @Ri instruction, P2 outputs SFR content.
 3. When executing MOVX @DPTR instruction, if DPHDIS is set (Page Access Mode), P2 outputs SFR content instead of DPH.

Dual Data Pointer

Description

The AT8xC51SND1A implements a second data pointer for speeding up code execution and reducing code size in case of intensive usage of external memory accesses. DPTR0 and DPTR1 are seen by the CPU as DPTR and are accessed using the SFR addresses 83h and 84h that are the DPH and DPL addresses. The DPS bit in AUXR1 register (see Table 14) is used to select whether DPTR is the data pointer 0 or the data pointer 1 (see Figure 7).

Figure 7. Dual Data Pointer Implementation



Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a “source” pointer and the other one as a “destination” pointer.

Hereafter is an example of block move implementation using the two pointers and coded in assembler. The latest C compiler also takes advantage of this feature by providing enhanced algorithm libraries.

The INC instruction is a short (2 bytes) and fast (6 CPU clocks) way to manipulate the DPS bit in the AUXR1 register. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry.

```
; ASCII block move using dual data pointers
; Modifies DPTR0, DPTR1, A and PSW
; Ends when encountering NULL character
; Note: DPS exits opposite of entry state unless an extra INC AUXR1 is added
```

```
AUXR1 EQU 0A2h
```

```
move: mov DPTR, #SOURCE ; address of SOURCE
      inc AUXR1 ; switch data pointers
      mov DPTR, #DEST ; address of DEST
mv_loop: inc AUXR1 ; switch data pointers
         movx A, @DPTR ; get a byte from SOURCE
         inc DPTR ; increment SOURCE address
         inc AUXR1 ; switch data pointers
         movx @DPTR, A ; write the byte to DEST
         inc DPTR ; increment DEST address
         jnz mv_loop ; check for NULL terminator
end_move:
```

Registers

Table 12. PSW Register
PSW (S:8Eh) – Program Status Word Register

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P
Bit Number	Bit Mnemonic	Description					
7	CY	Carry Flag Carry out from bit 1 of ALU operands.					
6	AC	Auxiliary Carry Flag Carry out from bit 1 of addition operands.					
5	F0	User Definable Flag 0.					
4-3	RS1:0	Register Bank Select Bits Refer to Table 9 for bits description.					
2	OV	Overflow Flag Overflow set by arithmetic operations.					
1	F1	User Definable Flag 1.					
0	P	Parity Bit Set when ACC contains an odd number of 1's. Cleared when ACC contains an even number of 1's.					

Reset Value = 0000 0000b

Table 13. AUXR Register
AUXR (S:8Eh) – Auxiliary Control Register

7	6	5	4	3	2	1	0
-	EXT16	M0	DPHDIS	XRS1	XRS0	EXTRAM	AO

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	EXT16	External 16-bit Access Enable Bit Set to enable 16-bit access mode during MOVX instructions. Clear to disable 16-bit access mode and enable standard 8-bit access mode during MOVX instructions.
5	M0	External Memory Access Stretch Bit Set to stretch RD# or WR# signals duration to 15 CPU clock periods. Clear not to stretch RD# or WR# signals and set duration to 3 CPU clock periods.
4	DPHDIS	DPH Disable Bit Set to disable DPH output on P2 when executing MOVX @DPTR instruction. Clear to enable DPH output on P2 when executing MOVX @DPTR instruction.
3-2	XRS1:0	Expanded RAM Size Bits Refer to Table 10 for ERAM size description.
1	EXTRAM	External RAM Enable Bit Set to select the external XRAM when executing MOVX @Ri or MOVX @DPTR instructions. Clear to select the internal expanded RAM when executing MOVX @Ri or MOVX @DPTR instructions.
0	AO	ALE Output Enable Bit Set to output the ALE signal only during MOVX instructions. Clear to output the ALE signal at a constant rate of $F_{CPU}/3$.

Reset Value = X000 1101b

Table 14. AUXR1 Register
AUXR1 (S:A2h) – Auxiliary Control Register 1

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7-4	-	Reserved The value read from these bits is indeterminate. Do not set these bits.
3	GF3	General Purpose Flag 3.
2	0	Always Zero This bit is stuck to logic 0 to allow INC AUXR1 instruction without affecting GF3 flag.
1	-	Reserved for Data Pointer Extension.
0	DPS	Data Pointer Select Bit Set to select second data pointer: DPTR1. Clear to select first data pointer: DPTR0.

Reset Value = XXXX 00X0b



Special Function Registers

The Special Function Registers (SFRs) of the AT8xC51SND1A derivatives fall into the categories detailed in Table 15 to Table 31. The relative addresses of these SFRs are provided together with their reset values in Table 32. In this table, the bit-addressable registers are identified by Note 1.

Table 15. C51 Core SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator								
B	F0h	B Register								
PSW	D0h	Program Status Word	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81h	Stack Pointer								
DPL	82h	Data Pointer Low byte								
DPH	83h	Data Pointer High byte								

Table 16. System Management SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PCON	87h	Power Control	SMOD1	SMOD0	-	-	GF1	GF0	PD	IDL
AUXR	8Eh	Auxiliary Register 0	-	EXT16	M0	DPHDIS	XRS1	XRS0	EXTRA M	AO
AUXR1	A2h	Auxiliary Register 1	-	-	ENBOO T	-	GF3	0	-	DPS
NVERS	FBh	Version Number	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0

Table 17. PLL and System Clock SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CKCON	8Fh	Clock Control	-	-	-	-	-	-	-	X2
PLLCON	E9h	PLL Control	R1	R0	-	-	PLLRES	-	PLLEN	PLOCK
PLLNDIV	EEh	PLL N Divider	-	N6	N5	N4	N3	N2	N1	N0
PLLRDIV	EFh	PLL R Divider	R9	R8	R7	R6	R5	R4	R3	R2

Table 18. Interrupt SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EAUD	EMP3	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1	-	EUSB	-	EKB	EADC	ESPI	EI2C	EMMC
IPH0	B7h	Interrupt Priority Control High 0	-	IPHAUD	IPHMP3	IPHS	IPHT1	IPHX1	IPHT0	IPHX0
IPL0	B8h	Interrupt Priority Control Low 0	-	IPLAUD	IPLMP3	IPLS	IPLT1	IPLX1	IPLT0	IPLX0
IPH1	B3h	Interrupt Priority Control High 1	-	IPHUSB	-	IPHKB	IPHADC	IPHSPI	IPHI2C	IPHMMC
IPL1	B2h	Interrupt Priority Control Low 1	-	IPLUSB	-	IPLKB	IPLADC	IPLSPI	IPLI2C	IPLMMC

Table 19. Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0	80h	8-bit Port 0								
P1	90h	8-bit Port 1								
P2	A0h	8-bit Port 2								
P3	B0h	8-bit Port 3								
P4	C0h	8-bit Port 4								
P5	D8h	4-bit Port 5	-	-	-	-				

Table 20. Flash Memory SFR

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
FCON	D1h	Flash Control	FPL3	FPL2	FPL1	FPL0	FPS	FMOD1	FMOD0	FBUSY

Table 21. Timer SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TCON	88h	Timer/Counter 0 and 1 Control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	Timer/Counter 0 and 1 Modes	GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00
TL0	8Ah	Timer/Counter 0 Low Byte								
TH0	8Ch	Timer/Counter 0 High Byte								
TL1	8Bh	Timer/Counter 1 Low Byte								
TH1	8Dh	Timer/Counter 1 High Byte								
WDTRST	A6h	WatchDog Timer Reset								
WDTPRG	A7h	WatchDog Timer Program	-	-	-	-	-	WTO2	WTO1	WTO0

Table 22. MP3 Decoder SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
MP3CON	AAh	MP3 Control	MPEN	MPBBS T	CRCE	MSKAN C	MSKRE Q	MSKLAY	MSKSY N	MSKCR C
MP3STA	C8h	MP3 Status	MPANC	MPREQ	ERRLAY	ERRSY N	ERRCR C	MPFS1	MPFS0	MPVER
MP3STA1	AFh	MP3 Status 1	-	-	-	MPFRE Q	MPBRE Q	-	-	-

Table 22. MP3 Decoder SFRs (Continued)

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
MP3DAT	AC _h	MP3 Data	MPD7	MPD6	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0
MP3ANC	AD _h	MP3 Ancillary Data	AND7	AND6	AND5	AND4	AND3	AND2	AND1	AND0
MP3VOL	9E _h	MP3 Audio Volume Control Left	-	-	-	VOL4	VOL3	VOL2	VOL1	VOL0
MP3VOR	9F _h	MP3 Audio Volume Control Right	-	-	-	VOR4	VOR3	VOR2	VOR1	VOR0
MP3BAS	B4 _h	MP3 Audio Bass Control	-	-	-	BAS4	BAS3	BAS2	BAS1	BAS0
MP3MED	B5 _h	MP3 Audio Medium Control	-	-	-	MED4	MED3	MED2	MED1	MED0
MP3TRE	B6 _h	MP3 Audio Treble Control	-	-	-	TRE4	TRE3	TRE2	TRE1	TRE0
MP3CLK	EB _h	MP3 Clock Divider	-	-	-	MPCD4	MPCD3	MPCD2	MPCD1	MPCD0

Table 23. Audio Interface SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
AUDCON0	9A _h	Audio Control 0	JUST4	JUST3	JUST2	JUST1	JUST0	POL	DSIZ	HLR
AUDCON1	9B _h	Audio Control 1	SRC	DRQEN	MSREQ	MUDRN	-	DUP1	DUP0	AUDEN
AUDSTA	9C _h	Audio Status	SREQ	UDRN	AUBUS Y	-	-	-	-	-
AUDDAT	9D _h	Audio Data	AUD7	AUD6	AUD5	AUD4	AUD3	AUD2	AUD1	AUD0
AUDCLK	E _h	Audio Clock Divider	-	-	-	AUCD4	AUCD3	AUCD2	AUCD1	AUCD0

Table 24. USB Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
USBCON	BCh	USB Global Control	USBE	SUSPCLK	SDRMWUP	-	UPRSM	RMWUPE	CONFIG	FADDEN
USBADDR	C6h	USB Address	FEN	UADD6	UADD5	UADD4	UADD3	UADD2	UADD1	UADD0
USBINT	BDh	USB Global Interrupt	-	-	WUPCPU	EORINT	SOFINT	-	-	SPINT
USBIEN	BEh	USB Global Interrupt Enable	-	-	EWUPCPU	EEORINT	ESOFINT	-	-	ESPINT
UEPNUM	C7h	USB Endpoint Number	-	-	-	-	-	-	EPNUM1	EPNUM0
UEPCONX	D4h	USB Endpoint X Control	EPEN	-	-	-	DTGL	EPDIR	EPTYPE1	EPTYPE0
UEPSTAX	CEh	USB Endpoint X Status	DIR	-	STALLRQ	TXRDY	STLCRC	RXSETUP	RXOUT	TXCMP
UEPRST	D5h	USB Endpoint Reset	-	-	-	-	EP3RST	EP2RST	EP1RST	EP0RST
UEPINT	F8h	USB Endpoint Interrupt	-	-	-	-	EP3INT	EP2INT	EP1INT	EPOINT
UEPIEN	C2h	USB Endpoint Interrupt Enable	-	-	-	-	EP3INTE	EP2INTE	EP1INTE	EPOINTE
UEPDATX	CFh	USB Endpoint X Fifo Data	FDAT7	FDAT6	FDAT5	FDAT4	FDAT3	FDAT2	FDAT1	FDAT0
UBYCTX	E2h	USB Endpoint X Byte Counter	-	BYCT6	BYCT5	BYCT4	BYCT3	BYCT2	BYCT1	BYCT0
UFNUML	BAh	USB Frame Number Low	FNUM7	FNUM6	FNUM5	FNUM4	FNUM3	FNUM2	FNUM1	FNUM0
UFNUMH	BBh	USB Frame Number High	-	-	CRCOK	CRCERR	-	FNUM10	FNUM9	FNUM8
USBCLK	EAh	USB Clock Divider	-	-	-	-	-	-	USBCD1	USBCD0

Table 25. MMC Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
MMCON0	E4h	MMC Control 0	DRPTR	DTPTR	CRPTR	CTPTR	MBLOCK	DFMT	RFMT	CRCDIS
MMCON1	E5h	MMC Control 1	BLEN3	BLEN2	BLEN1	BLEN0	DATDIR	DATEN	RESPEN	CMDEN
MMCON2	E6h	MMC Control 2	MMCEN	DCR	CCR	-	-	DATD1	DATD0	FLOWC
MMSTA	DEh	MMC Control and Status	-	-	CBUSY	CRC16S	DATFS	CRC7S	RESPFS	CFLCK
MMINT	E7h	MMC Interrupt	MCBI	EORI	EOCI	EOF1	F2FI	F1FI	F2EI	F1EI
MMMSK	DFh	MMC Interrupt Mask	MCBM	EORM	EOCM	EOFM	F2FM	F1FM	F2EM	F1EM
MMCMD	DDh	MMC Command	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0
MMDAT	DCh	MMC Data	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0
MMCLK	EDh	MMC Clock Divider	MMCD7	MMCD6	MMCD5	MMCD4	MMCD3	MMCD2	MMCD1	MMCD0

Table 26. IDE Interface SFR

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
DAT16H	F9h	High Order Data Byte	D15	D14	D13	D12	D11	D10	D9	D8

Table 27. Serial I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								
BDRCON	92h	Baud Rate Control				BRR	TBCK	RBCK	SPD	SRC
BRL	91h	Baud Rate Reload								

Table 28. SPI Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SPCON	C3h	SPI Control	SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0
SPSTA	C4h	SPI Status	SPIF	WCOL	-	MODF	-	-	-	-
SPDAT	C5h	SPI Data	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0

Table 29. Two-wire Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SSCON	93h	Synchronous Serial control	SSCR2	SSPE	SSSTA	SSSTO	SSI	SSAA	SSCR1	SSCR0
SSSTA	94h	Synchronous Serial Status	SSC4	SSC3	SSC2	SSC1	SSC0	0	0	0
SSDAT	95h	Synchronous Serial Data	SSD7	SSD6	SSD5	SSD4	SSD3	SSD2	SSD1	SSD0
SSADR	96h	Synchronous Serial Address	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSGC

Table 30. Keyboard Interface SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
KBCON	A3h	Keyboard Control	KINL3	KINL2	KINL1	KINL0	KINM3	KINM2	KINM1	KINM0
KBSTA	A4h	Keyboard Status	KPDE	-	-	-	KINF3	KINF2	KINF1	KINF0

Table 31. A/D Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ADCON	F3h	ADC Control	-	ADIDL	ADEN	ADEOC	ADSST	-	-	ADCS
ADCLK	F2h	ADC Clock Divider	-	-	-	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
ADDL	F4h	ADC Data Low Byte	-	-	-	-	-	-	ADAT1	ADAT0
ADDH	F5h	ADC Data High Byte	ADAT9	ADAT8	ADAT7	ADAT6	ADAT5	ADAT4	ADAT3	ADAT2

Table 32. SFR Addresses and Reset Values

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	UEPINT 0000 0000	DAT16H XXXX XXXX		NVERS ⁽²⁾ 1000 0010					FFh
F0h	B ⁽¹⁾ 0000 0000		ADCLK 0000 0000	ADCON 0000 0000	ADDL 0000 0000	ADDH 0000 0000			F7h
E8h		PLLCON 0000 1000	USBCLK 0000 0000	MP3CLK 0000 0000	AUDCLK 0000 0000	MMCLK 0000 0000	PLLNDIV 0000 0000	PLLRDIV 0000 0000	EFh
E0h	ACC ⁽¹⁾ 0000 0000		UBYCTLX 0000 0000		MMCON0 0000 0000	MMCON1 0000 0000	MMCON2 0000 0000	MMINT 0000 0011	E7h
D8h	P5 ⁽¹⁾ XXXX 1111				MMDAT 1111 1111	MMCMD 1111 1111	MMSTA 0000 0000	MMMSK 1111 1111	DFh
D0h	PSW ¹ 0000 0000	FCON ⁽³⁾ 1111 0000 ⁽⁴⁾			UEPCONX 0000 0000	UEPRST 0000 0000			D7h
C8h	MP3STA ⁽¹⁾ 0000 0001						UEPSTAX 0000 0000	UEPDATX 0000 0000	CFh
C0h	P4 ⁽¹⁾ 1111 1111		UEPIEN 0000 0000	SPCON 0001 0100	SPSTA 0000 0000	SPDAT XXXX XXXX	USBADDR 1000 0000	UEPNUM 0000 0000	C7h
B8h	IPL0 ⁽¹⁾ X000 0000	SADEN 0000 0000	UFNUML 0000 0000	UFNUMH 0000 0000	USBCON 0000 0000	USBINT 0000 0000	USBIEN 0001 0000		BFh
B0h	P3 ⁽¹⁾ 1111 1111	IEN1 0000 0000	IPL1 0000 0000	IPH1 0000 0000	MP3BAS 0000 0000	MP3MED 0000 0000	MP3TRE 0000 0000	IPH0 X000 0000	B7h
A8h	IEN0 ⁽¹⁾ 0000 0000	SADDR 0000 0000	MP3CON 0011 1111		MP3DAT 0000 0000	MP3ANC 0000 0000		MP3STA1 0100 0001	AFh
A0h	P2 ⁽¹⁾ 1111 1111		AUXR1 XXXX 00X0	KBCON 0000 1111	KBSTA 0000 0000		WDTRST XXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	AUDCON0 0000 1000	AUDCON1 1011 0010	AUDSTA 1100 0000	AUDDAT 1111 1111	MP3VOL 0000 0000	MP3VOR 0000 0000	9Fh
90h	P1 ⁽¹⁾ 1111 1111	BRL 0000 0000	BDRCON XXX0 0000	SSCON 0000 0000	SSSTA 1111 1000	SSDAT 1111 1111	SSADR 1111 1110		97h
88h	TCON ⁽¹⁾ 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR X000 1101	CKCON 0000 000X ⁽⁵⁾	8Fh
80h	P0 ⁽¹⁾ 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON XXXX 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

 Reserved 

- Notes:
1. SFR registers with least significant nibble address equal to 0 or 8 are bit-addressable.
 2. NVERS reset value depends on the silicon version.
 3. FCON register is only available in AT89C51SND1A product.
 4. FCON reset value is 00h in case of reset with hardware condition.
 5. CKCON reset value depends on the X2B bit (programmed or unprogrammed) in the Hardware Byte.

Interrupt System

The AT8xC51SND1A, like other control-oriented computer architectures, employs a program interrupt method. This operation branches to a subroutine and performs some service in response to the interrupt. When the subroutine completes, execution resumes at the point where the interrupt occurred. Interrupts may occur as a result of internal AT8xC51SND1A activity (e.g., timer overflow) or at the initiation of electrical signals external to the microcontroller (e.g., keyboard). In all cases, interrupt operation is programmed by the system designer, who determines priority of interrupt service relative to normal code execution and other interrupt service routines. All of the interrupt sources are enabled or disabled by the system designer and may be manipulated dynamically.

A typical interrupt event chain occurs as follows:

- An internal or external device initiates an interrupt-request signal. The AT8xC51SND1A, latches this event into a flag buffer.
- The priority of the flag is compared to the priority of other interrupts by the interrupt handler. A high priority causes the handler to set an interrupt flag.
- This signals the instruction execution unit to execute a context switch. This context switch breaks the current flow of instruction sequences. The execution unit completes the current instruction prior to a save of the program counter (PC) and reloads the PC with the start address of a software service routine.
- The software service routine executes assigned tasks and as a final activity performs a RETI (return from interrupt) instruction. This instruction signals completion of the interrupt, resets the interrupt-in-progress priority and reloads the program counter. Program operation then continues from the original point of interruption.

Table 33. Interrupt System Signals

Signal Name	Type	Description	Alternate Function
INT0#	I	External Interrupt 0 See Section "External Interrupts", page 34.	P3.2
INT1#	I	External Interrupt 1 See Section "External Interrupts", page 34.	P3.3
KIN3:0	I	Keyboard Interrupt Inputs See Section "Keyboard Interface", page 157.	P1.3:0

Six interrupt registers are used to control the interrupt system. Two 8-bit registers are used to enable separately the interrupt sources: IEN0 and IEN1 registers (see Table 36 and Table 37).

Four 8-bit registers are used to establish the priority level of the thirteen sources: IPH0, IPL0, IPH1 and IPL1 registers (see Table 38 to Table 41).

Interrupt System Priorities

Each of the eleven interrupt sources on the AT8xC51SND1A can be individually programmed to one of four priority levels. This is accomplished by one bit in the Interrupt Priority High registers (IPH0 and IPH1) and one bit in the Interrupt Priority Low registers (IPL0 and IPL1). This provides each interrupt source four possible priority levels according to Table 34.

Table 34. Priority Levels

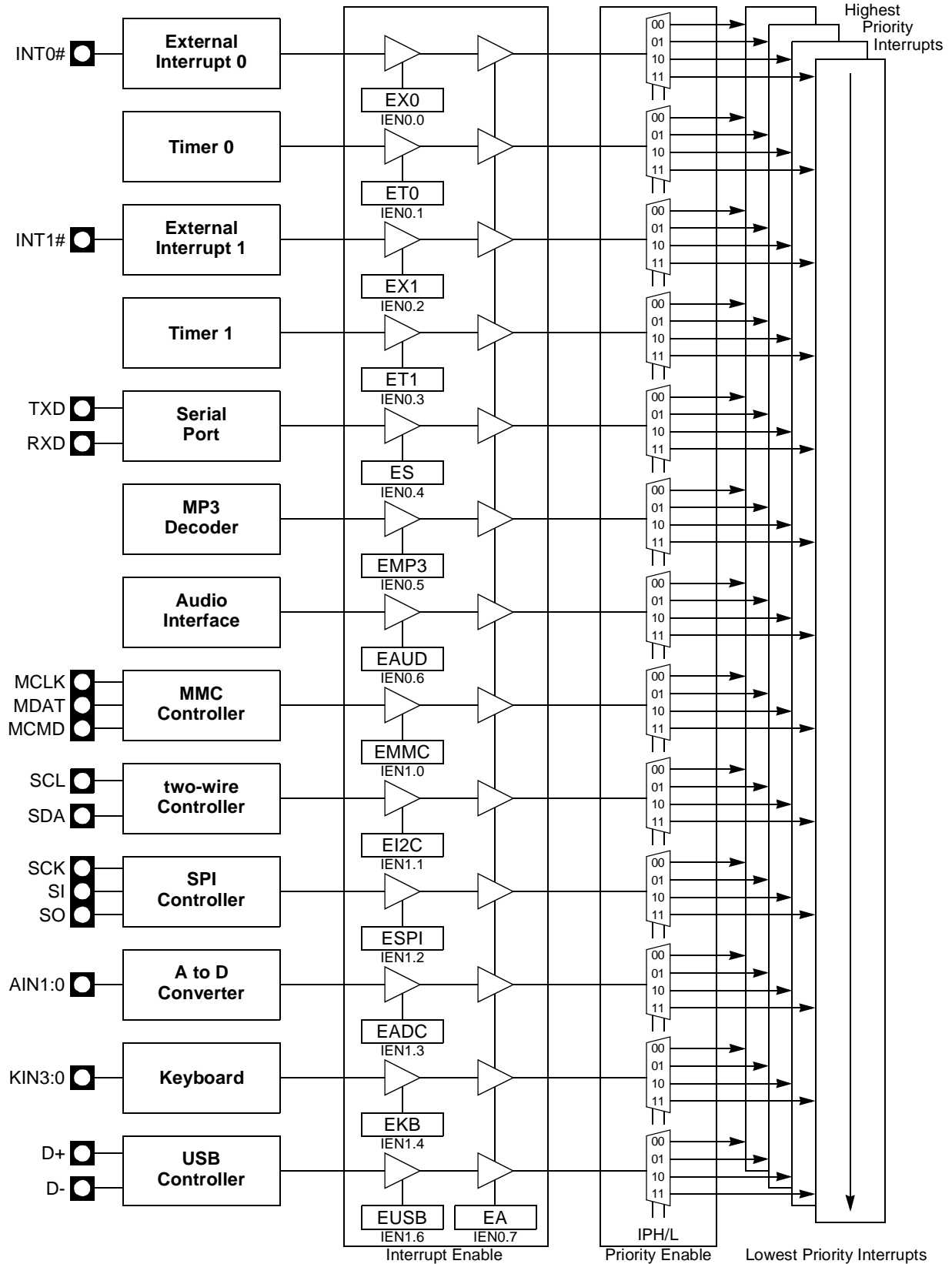
IPHxx	IPLxx	Priority Level
0	0	0 Lowest
0	1	1
1	0	2
1	1	3 Highest

A low-priority interrupt is always interrupted by a higher priority interrupt but not by another interrupt of lower or equal priority. Higher priority interrupts are serviced before lower priority interrupts. The response to simultaneous occurrence of equal priority interrupts is determined by an internal hardware polling sequence detailed in Table 35. Thus within each priority level there is a second priority structure determined by the polling sequence. The interrupt control system is shown in Figure 12.

Table 35. Priority Within Same Level

Interrupt Name	Priority Number	Interrupt Address Vectors	Interrupt request flag cleared by hardware (H) or by software (S)
INT0#	1 (Highest Priority)	C:0003h	H if edge, S if level
Timer 0	2	C:000Bh	H
INT1#	3	C:0013h	H if edge, S if level
Timer 1	4	C:001Bh	H
Serial Port	5	C:0023h	S
MP3 Decoder	6	C:002Bh	S
Audio Interface	7	C:0033h	S
MMC Interface	8	C:003Bh	S
two-wire Controller	9	C:0043h	S
SPI Controller	10	C:004Bh	S
A to D Converter	11	C:0053h	S
Keyboard	12	C:005Bh	S
Reserved	13	C:0063h	-
USB	14	C:006Bh	S
Reserved	15 (Lowest Priority)	C:0073h	-

Figure 12. Interrupt Control System



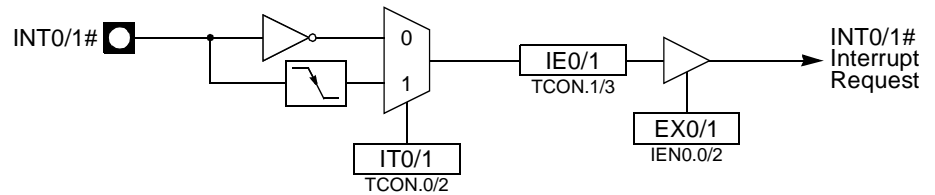
External Interrupts

INT1:0# Inputs

External interrupts INT0# and INT1# (INTn#, n = 0 or 1) pins may each be programmed to be level-triggered or edge-triggered, dependent upon bits IT0 and IT1 (ITn, n = 0 or 1) in TCON register as shown in Figure 8. If ITn = 0, INTn# is triggered by a low level at the pin. If ITn = 1, INTn# is negative-edge triggered. External interrupts are enabled with bits EX0 and EX1 (EXn, n = 0 or 1) in IEN0. Events on INTn# set the interrupt request flag IEn in TCON register. If the interrupt is edge-triggered, the request flag is cleared by hardware when vectoring to the interrupt service routine. If the interrupt is level-triggered, the interrupt service routine must clear the request flag and the interrupt must be deasserted before the end of the interrupt service routine.

INT0# and INT1# inputs provide both the capability to exit from Power-down mode on low level signals as detailed in Section “Exiting Power-down Mode”, page 43.

Figure 8. INT1:0# Input Circuitry



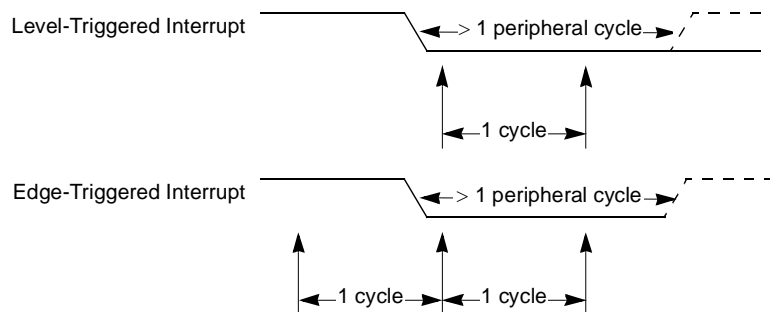
KIN3:0 Inputs

External interrupts KIN0 to KIN3 provide the capability to connect a matrix keyboard. For detailed information on these inputs, refer to Section “Keyboard Interface”, page 157.

Input Sampling

External interrupt pins (INT1:0# and KIN3:0) are sampled once per peripheral cycle (6 peripheral clock periods) (see Figure 9). A level-triggered interrupt pin held low or high for more than 6 peripheral clock periods (12 oscillator in standard mode or 6 oscillator clock periods in X2 mode) guarantees detection. Edge-triggered external interrupts must hold the request pin low for at least 6 peripheral clock periods.

Figure 9. Minimum Pulse Timings



Registers

Table 36. IEN0 Register
IEN0 (S:A8h) – Interrupt Enable Register 0

7	6	5	4	3	2	1	0
EA	EAUD	EMP3	ES	ET1	EX1	ET0	EX0
Bit Number	Bit Mnemonic	Description					
7	EA	Enable All Interrupt Bit Set to enable all interrupts. Clear to disable all interrupts. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its interrupt enable bit.					
6	EAUD	Audio Interface Interrupt Enable Bit Set to enable audio interface interrupt. Clear to disable audio interface interrupt.					
5	EMP3	MP3 Decoder Interrupt Enable Bit Set to enable MP3 decoder interrupt. Clear to disable MP3 decoder interrupt.					
4	ES	Serial Port Interrupt Enable Bit Set to enable serial port interrupt. Clear to disable serial port interrupt.					
3	ET1	Timer 1 Overflow Interrupt Enable Bit Set to enable timer 1 overflow interrupt. Clear to disable timer 1 overflow interrupt.					
2	EX1	External Interrupt 1 Enable bit Set to enable external interrupt 1. Clear to disable external interrupt 1.					
1	ET0	Timer 0 Overflow Interrupt Enable Bit Set to enable timer 0 overflow interrupt. Clear to disable timer 0 overflow interrupt.					
0	EX0	External Interrupt 0 Enable Bit Set to enable external interrupt 0. Clear to disable external interrupt 0.					

Reset Value = 0000 0000b

Table 37. IEN1 Register
 IEN1 (S:B1h) – Interrupt Enable Register 1

7	6	5	4	3	2	1	0
-	EUSB	-	EKB	EADC	ESPI	EI2C	EMMC
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The value read from this bit is always 0. Do not set this bit.					
6	EUSB	USB Interface Interrupt Enable Bit Set this bit to enable USB interrupts. Clear this bit to disable USB interrupts.					
5	-	Reserved The value read from this bit is always 0. Do not set this bit.					
4	EKB	Keyboard Interface Interrupt Enable Bit Set to enable Keyboard interrupt. Clear to disable Keyboard interrupt.					
3	EADC	A to D Converter Interrupt Enable Bit Set to enable ADC interrupt. Clear to disable ADC interrupt.					
2	ESPI	SPI Controller Interrupt Enable Bit Set to enable SPI interrupt. Clear to disable SPI interrupt.					
1	EI2C	Two-wire Controller Interrupt Enable Bit Set to enable two-wire interrupt. Clear to disable two-wire interrupt.					
0	EMMC	MMC Interface Interrupt Enable Bit Set to enable MMC interrupt. Clear to disable MMC interrupt.					

Reset Value = 0000 0000b

Table 38. IPH0 Register
IPH0 (S:B7h) – Interrupt Priority High Register 0

7	6	5	4	3	2	1	0
-	IPHAUD	IPHMP3	IPHS	IPHT1	IPHX1	IPHT0	IPHX0
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
6	IPHAUD	Audio Interface Interrupt Priority Level MSB Refer to Table 34 for priority level description.					
5	IPHMP3	MP3 Decoder Interrupt Priority Level MSB Refer to Table 34 for priority level description.					
4	IPHS	Serial Port Interrupt Priority Level MSB Refer to Table 34 for priority level description.					
3	IPHT1	Timer 1 Interrupt Priority Level MSB Refer to Table 34 for priority level description.					
2	IPHX1	External Interrupt 1 Priority Level MSB Refer to Table 34 for priority level description.					
1	IPHT0	Timer 0 Interrupt Priority Level MSB Refer to Table 34 for priority level description.					
0	IPHX0	External Interrupt 0 Priority Level MSB Refer to Table 34 for priority level description.					

Reset Value = X000 0000b

Table 39. IPH1 Register
IPH1 (S:B3h) – Interrupt Priority High Register 1

7	6	5	4	3	2	1	0
-	IPHUSB	-	IPHKB	IPHADC	IPHSPI	IPHI2C	IPHMMC
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The value read from this bit is always 0. Do not set this bit.					
6	IPHUSB	USB Interrupt Priority Level MSB Refer to Table 34 for priority level description.					
5	-	Reserved The value read from this bit is always 0. Do not set this bit.					
4	IPHKB	Keyboard Interrupt Priority Level MSB Refer to Table 34 for priority level description.					
3	IPHADC	A to D Converter Interrupt Priority Level MSB Refer to Table 34 for priority level description.					
2	IPHSPI	SPI Interrupt Priority Level MSB Refer to Table 34 for priority level description.					
1	IPHI2C	Two-wire Controller Interrupt Priority Level MSB Refer to Table 34 for priority level description.					
0	IPHMMC	MMC Interrupt Priority Level MSB Refer to Table 34 for priority level description.					

Reset Value = 0000 0000b

Table 40. IPL0 Register
IPL0 (S:B8h) - Interrupt Priority Low Register 0

7	6	5	4	3	2	1	0
-	IPLAUD	IPLMP3	IPLS	IPLT1	IPLX1	IPLT0	IPLX0
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
6	IPLAUD	Audio Interface Interrupt Priority Level LSB Refer to Table 34 for priority level description.					
5	IPLMP3	MP3 Decoder Interrupt Priority Level LSB Refer to Table 34 for priority level description.					
4	IPLS	Serial Port Interrupt Priority Level LSB Refer to Table 34 for priority level description.					
3	IPLT1	Timer 1 Interrupt Priority Level LSB Refer to Table 34 for priority level description.					
2	IPLX1	External Interrupt 1 Priority Level LSB Refer to Table 34 for priority level description.					
1	IPLT0	Timer 0 Interrupt Priority Level LSB Refer to Table 34 for priority level description.					
0	IPLX0	External Interrupt 0 Priority Level LSB Refer to Table 34 for priority level description.					

Reset Value = X000 0000b

Table 41. IPL1 Register
IPL1 (S:B2h) – Interrupt Priority Low Register 1

	7	6	5	4	3	2	1	0
	-	IPLUSB	-	IPLKB	IPLADC	IPLSPI	IPLI2C	IPLMMC

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is always 0. Do not set this bit.
6	IPLUSB	USB Interrupt Priority Level LSB Refer to Table 34 for priority level description.
5	-	Reserved The value read from this bit is always 0. Do not set this bit.
4	IPLKB	Keyboard Interrupt Priority Level LSB Refer to Table 34 for priority level description.
3	IPLADC	A to D Converter Interrupt Priority Level LSB Refer to Table 34 for priority level description.
2	IPLSPI	SPI Interrupt Priority Level LSB Refer to Table 34 for priority level description.
1	IPLI2C	Two-wire Controller Interrupt Priority Level LSB Refer to Table 31 for priority level description.
0	IPLMMC	MMC Interrupt Priority Level LSB Refer to Table 34 for priority level description.

Reset Value = 0000 0000b

Power Management

Two power reduction modes are implemented in the AT8xC51SND1A: the Idle mode and the Power-down mode. These modes are detailed in the following sections. In addition to these power reduction modes, the clocks of the core and peripherals can be dynamically divided by 2 using the X2 mode detailed in Section “X2 Feature”, page 4.

Reset

A reset is required after applying power at turn-on. To achieve a valid reset, the reset signal must be maintained for at least 2 machine cycles (24 oscillator clock periods) while the oscillator is running. A device reset initializes the AT8xC51SND1A and vectors the CPU to address 0000h. RST input has a pull-down resistor allowing power-on reset by simply connecting an external capacitor to V_{DD} as shown in Figure 10. Resistor value and input characteristics are discussed in the Section “DC Characteristics” of the AT8xC51SND1A datasheet. The status of the Port pins during reset is detailed in Table 42.

Figure 10. Reset Circuitry and Power-On Reset

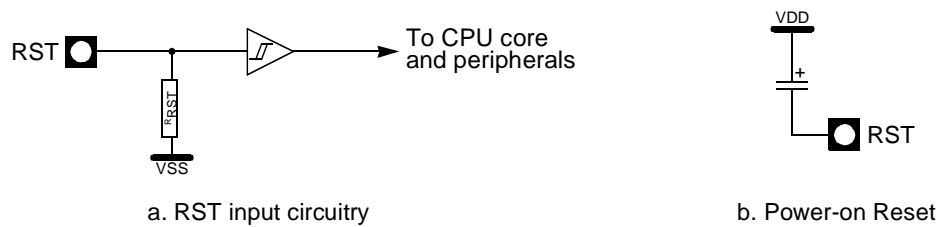


Table 42. Pin Conditions in Special Operating Modes

Mode	Port 0	Port 1	Port 2	Port 3	Port 4	Port 5	MMC	Audio
Reset	Floating	High	High	High	High	High	Floating	¹
Idle	Data	Data	Data	Data	Data	Data	Data	Data
Power-down	Data	Data	Data	Data	Data	Data	Data	Data

Note: 1. Refer to Section “Audio Output Interface”, page 67.

Reset Recommendation to Prevent Flash Corruption

A bad reset sequence will lead to bad microcontroller initialization and system registers like SFR’s, Program Counter, etc. will not be correctly initialized. A bad initialization may lead to unpredictable behaviour of the C51 microcontroller.

An example of this situation may occur in an instance where the bit ENBOOT in AUXR1 register is initialized from the hardware bit BLJB upon reset. Since this bit allows mapping of the bootloader in the code area, a reset failure can be critical.

If one wants the ENBOOT cleared in order to unmap the boot from the code area (yet due to a bad reset) the bit ENBOOT in SFR’s may be set. If the value of Program Counter is accidentally in the range of the boot memory addresses then a flash access (write or erase) may corrupt the Flash on-chip memory .

It is recommended to use an external reset circuitry featuring power supply monitoring to prevent system malfunction during periods of insufficient power supply voltage (power supply failure, power supply switched off).

Idle Mode

Idle mode is a power reduction mode that reduces the power consumption. In this mode, program execution halts. Idle mode freezes the clock to the CPU at known states while the peripherals continue to be clocked (refer to Section “Oscillator”, page 4). The CPU status before entering Idle mode is preserved, i.e., the program counter and program status word register retain their data for the duration of Idle mode. The contents of the SFRs and RAM are also retained. The status of the Port pins during Idle mode is detailed in Table 42.

Entering Idle Mode

To enter Idle mode, you must set the IDL bit in PCON register (see Table 43). The AT8xC51SND1A enters Idle mode upon execution of the instruction that sets IDL bit. The instruction that sets IDL bit is the last instruction executed.

Note: If IDL bit and PD bit are set simultaneously, the AT8xC51SND1A enters Power-down mode. Then it does not go in Idle mode when exiting Power-down mode.

Exiting Idle Mode

There are two ways to exit Idle mode:

1. Generate an enabled interrupt.
 - Hardware clears IDL bit in PCON register which restores the clock to the CPU. Execution resumes with the interrupt service routine. Upon completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Idle mode. The general-purpose flags (GF1 and GF0 in PCON register) may be used to indicate whether an interrupt occurred during normal operation or during Idle mode. When Idle mode is exited by an interrupt, the interrupt service routine may examine GF1 and GF0.
2. Generate a reset.
 - A logic high on the RST pin clears IDL bit in PCON register directly and asynchronously. This restores the clock to the CPU. Program execution momentarily resumes with the instruction immediately following the instruction that activated the Idle mode and may continue for a number of clock cycles before the internal reset algorithm takes control. Reset initializes the AT8xC51SND1A and vectors the CPU to address C:0000h.

Note: During the time that execution resumes, the internal RAM cannot be accessed; however, it is possible for the Port pins to be accessed. To avoid unexpected outputs at the Port pins, the instruction immediately following the instruction that activated Idle mode should not write to a Port pin or to the external RAM.

Power-down Mode

The Power-down mode places the AT8xC51SND1A in a very low power state. Power-down mode stops the oscillator and freezes all clocks at known states (refer to the Section “Oscillator”, page 4). The CPU status prior to entering Power-down mode is preserved, i.e., the program counter, program status word register retain their data for the duration of Power-down mode. In addition, the SFRs and RAM contents are preserved. The status of the Port pins during Power-down mode is detailed in Table 42.

Note: VDD may be reduced to as low as V_{RET} during Power-down mode to further reduce power dissipation. Take care, however, that VDD is not reduced until Power-down mode is invoked.

Entering Power-down Mode

To enter Power-down mode, set PD bit in PCON register. The AT8xC51SND1A enters the Power-down mode upon execution of the instruction that sets PD bit. The instruction that sets PD bit is the last instruction executed.

Exiting Power-down Mode

If VDD was reduced during the Power-down mode, do not exit Power-down mode until VDD is restored to the normal operating level.

There are two ways to exit the Power-down mode:

1. Generate an enabled external interrupt.
 - The AT8xC51SND1A provides capability to exit from Power-down using INT0#, INT1#, and KIN3:0 inputs. In addition, using KIN input provides high or low level exit capability (see Section “Keyboard Interface”, page 157). Hardware clears PD bit in PCON register which starts the oscillator and restores the clocks to the CPU and peripherals. Using INTx# input, execution resumes when the input is released (see Figure 13) while using KINx input, execution resumes after counting 1024 clock ensuring the oscillator is restarted properly (see Figure 14). This behavior is necessary for decoding the key while it is still pressed. In both cases, execution resumes with the interrupt service routine. Upon completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-down mode.

- Note:
1. The external interrupt used to exit Power-down mode must be configured as level sensitive (INT0# and INT1#) and must be assigned the highest priority. In addition, the duration of the interrupt must be long enough to allow the oscillator to stabilize. The execution will only resume when the interrupt is deasserted.
 2. Exit from power-down by external interrupt does not affect the SFRs nor the internal RAM content.

Figure 13. Power-down Exit Waveform Using INT1:0#

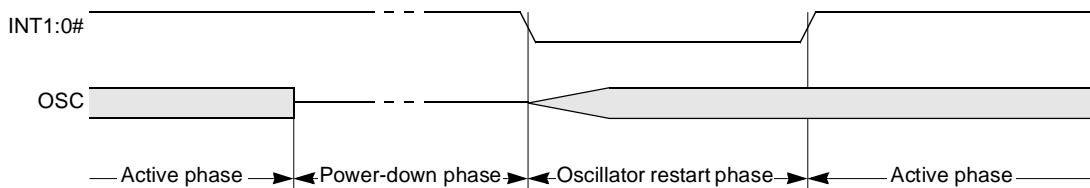
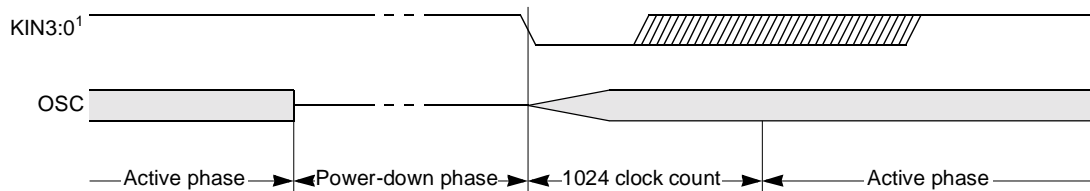


Figure 14. Power-down Exit Waveform Using KIN3:0



- Note:
1. KIN3:0 can be high or low level triggered.

2. Generate a reset.
 - A logic high on the RST pin clears PD bit in PCON register directly and asynchronously. This starts the oscillator and restores the clock to the CPU and peripherals. Program execution momentarily resumes with the instruction immediately following the instruction that activated Power-down mode and may continue for a number of clock cycles before the internal

reset algorithm takes control. Reset initializes the AT8xC51SND1A and vectors the CPU to address 0000h.

- Notes:
1. During the time that execution resumes, the internal RAM cannot be accessed; however, it is possible for the Port pins to be accessed. To avoid unexpected outputs at the Port pins, the instruction immediately following the instruction that activated the Power-down mode should not write to a Port pin or to the external RAM.
 2. Exit from power-down by reset redefines all the SFRs, but does not affect the internal RAM content.

Registers

Table 43. PCON Register

PCON (S:87h) – Power configuration Register

7	6	5	4	3	2	1	0
-	-	-	-	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7-4	-	Reserved The value read from these bits is indeterminate. Do not set these bits.
3	GF1	General-purpose flag 1 One use is to indicate whether an interrupt occurred during normal operation or during Idle mode.
2	GF0	General-purpose flag 0 One use is to indicate whether an interrupt occurred during normal operation or during Idle mode.
1	PD	Power-down Mode bit Cleared by hardware when an interrupt or reset occurs. Set to activate the Power-down mode. If IDL and PD are both set, PD takes precedence.
0	IDL	Idle Mode bit Cleared by hardware when an interrupt or reset occurs. Set to activate the Idle mode. If IDL and PD are both set, PD takes precedence.

Reset Value = XXXX 0000b

Timers/Counters

The AT8xC51SND1A implements two general-purpose, 16-bit Timers/Counters. They are identified as Timer 0 and Timer 1, and can be independently configured to operate in a variety of modes as a Timer or as an event Counter. When operating as a Timer, the Timer/Counter runs for a programmed length of time, then issues an interrupt request. When operating as a Counter, the Timer/Counter counts negative transitions on an external pin. After a preset number of counts, the Counter issues an interrupt request.

The various operating modes of each Timer/Counter are described in the following sections.

Timer/Counter Operations

For instance, a basic operation is Timer registers THx and TLx ($x = 0, 1$) connected in cascade to form a 16-bit Timer. Setting the run control bit (TRx) in TCON register (see Table 44) turns the Timer on by allowing the selected input to increment TLx. When TLx overflows it increments THx; when THx overflows it sets the Timer overflow flag (TFx) in TCON register. Setting the TRx does not clear the THx and TLx Timer registers. Timer registers can be accessed to obtain the current count or to enter preset values. They can be read at any time but TRx bit must be cleared to preset their values, otherwise the behavior of the Timer/Counter is unpredictable.

The C/Tx# control bit selects Timer operation or Counter operation by selecting the divided-down peripheral clock or external pin Tx as the source for the counted signal. TRx bit must be cleared when changing the mode of operation, otherwise the behavior of the Timer/Counter is unpredictable.

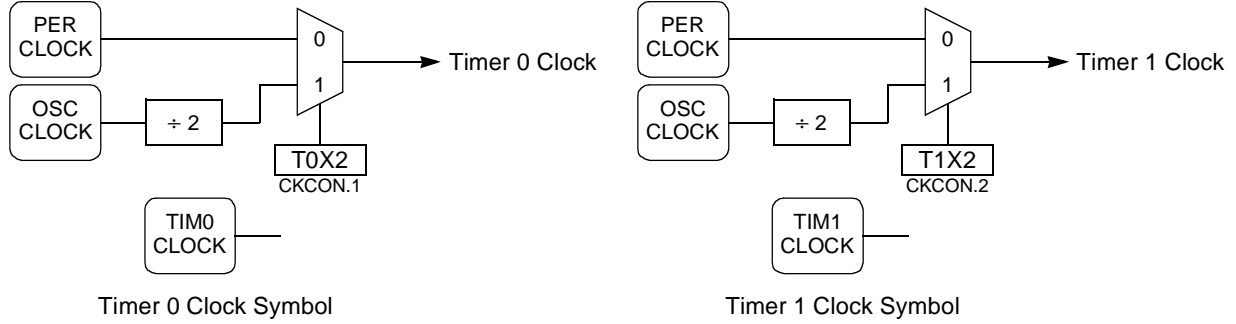
For Timer operation ($C/Tx\# = 0$), the Timer register counts the divided-down peripheral clock. The Timer register is incremented once every peripheral cycle (6 peripheral clock periods). The Timer clock rate is $F_{PER}/6$, i.e. $F_{OSC}/12$ in standard mode or $F_{OSC}/6$ in X2 mode.

For Counter operation ($C/Tx\# = 1$), the Timer register counts the negative transitions on the Tx external input pin. The external input is sampled every peripheral cycles. When the sample is high in one cycle and low in the next one, the Counter is incremented. Since it takes 2 cycles (12 peripheral clock periods) to recognize a negative transition, the maximum count rate is $F_{PER}/12$, i.e. $F_{OSC}/24$ in standard mode or $F_{OSC}/12$ in X2 mode. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full peripheral cycle.

Timer Clock Controller

As shown in Figure 15 the Timer 0 (FT0) and Timer 1 (FT1) clocks are derived from either the peripheral clock (F_{PER}) or the oscillator clock (F_{OSC}) depending on the T0X2 and T1X2 bits in CKCON register. These clocks are issued from the Clock Controller block as detailed in Section "CKCON Register", page 7. When T0X2 or T1X2 bit is set, the Timer 0 or Timer 1 clock frequency is fixed and equal to the oscillator clock frequency divided by 2. When cleared, the Timer clock frequency is equal to the oscillator clock frequency divided by 2 in standard mode or to the oscillator clock frequency in X2 mode.

Figure 15. Timer 0 and Timer 1 Clock Controller and Symbols



Timer 0

Timer 0 functions as either a Timer or event Counter in four modes of operation. Figure 16 to Figure 22 show the logical configuration of each mode.

Timer 0 is controlled by the four lower bits of TMOD register (see Table 45) and bits 0, 1, 4 and 5 of TCON register (see Table 44). TMOD register selects the method of Timer gating (GATE0), Timer or Counter operation (T/C0#) and mode of operation (M10 and M00). TCON register provides Timer 0 control functions: overflow flag (TF0), run control bit (TR0), interrupt flag (IE0) and interrupt type control bit (IT0).

For normal Timer operation (GATE0 = 0), setting TR0 allows TL0 to be incremented by the selected input. Setting GATE0 and TR0 allows external pin INT0# to control Timer operation.

Timer 0 overflow (count rolls over from all 1s to all 0s) sets TF0 flag generating an interrupt request.

It is important to stop Timer/Counter before changing mode.

Mode 0 (13-bit Timer)

Mode 0 configures Timer 0 as a 13-bit Timer which is set up as an 8-bit Timer (TH0 register) with a modulo 32 prescaler implemented with the lower five bits of TL0 register (see Figure 16). The upper three bits of TL0 register are indeterminate and should be ignored. Prescaler overflow increments TH0 register. Figure 17 gives the overflow period calculation formula.

Figure 16. Timer/Counter x (x = 0 or 1) in Mode 0

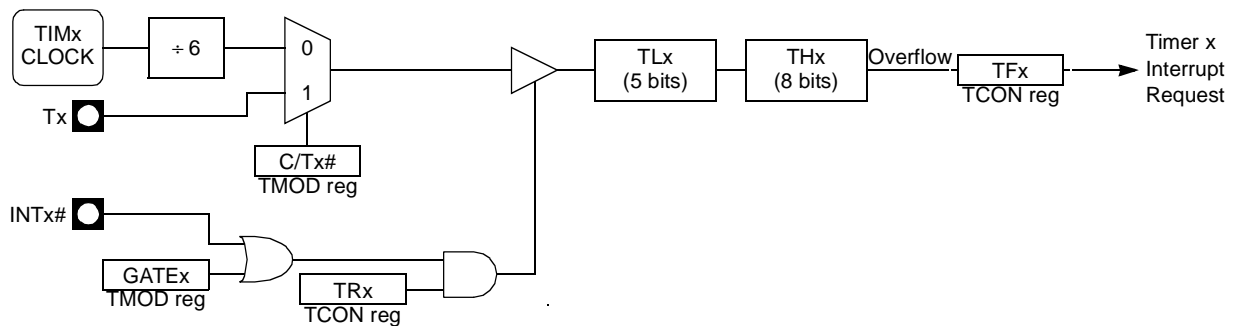


Figure 17. Mode 0 Overflow Period Formula

$$TF_{xPER} = \frac{6 \cdot (16384 - (TH_x, TL_x))}{F_{TIM_x}}$$

Mode 1 (16-bit Timer)

Mode 1 configures Timer 0 as a 16-bit Timer with TH0 and TL0 registers connected in cascade (see Figure 18). The selected input increments TL0 register. Figure 19 gives the overflow period calculation formula when in timer mode.

Figure 18. Timer/Counter x (x = 0 or 1) in Mode 1

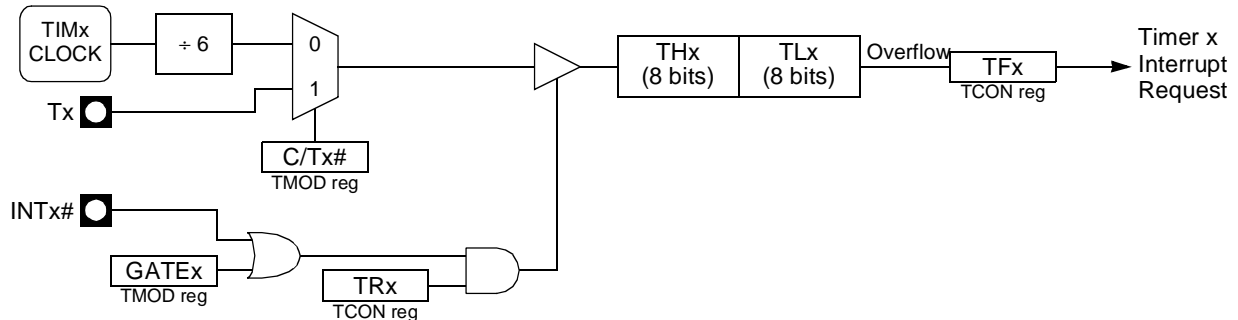


Figure 19. Mode 1 Overflow Period Formula

$$TF_{xPER} = \frac{6 \cdot (65536 - (TH_x, TL_x))}{F_{TIM_x}}$$

Mode 2 (8-bit Timer with Auto-Reload)

Mode 2 configures Timer 0 as an 8-bit Timer (TL0 register) that automatically reloads from TH0 register (see Table 46). TL0 overflow sets TF0 flag in TCON register and reloads TL0 with the contents of TH0, which is preset by software. When the interrupt request is serviced, hardware clears TF0. The reload leaves TH0 unchanged. The next reload value may be changed at any time by writing it to TH0 register. Figure 21 gives the autoreload period calculation formula when in timer mode.

Figure 20. Timer/Counter x (x = 0 or 1) in Mode 2

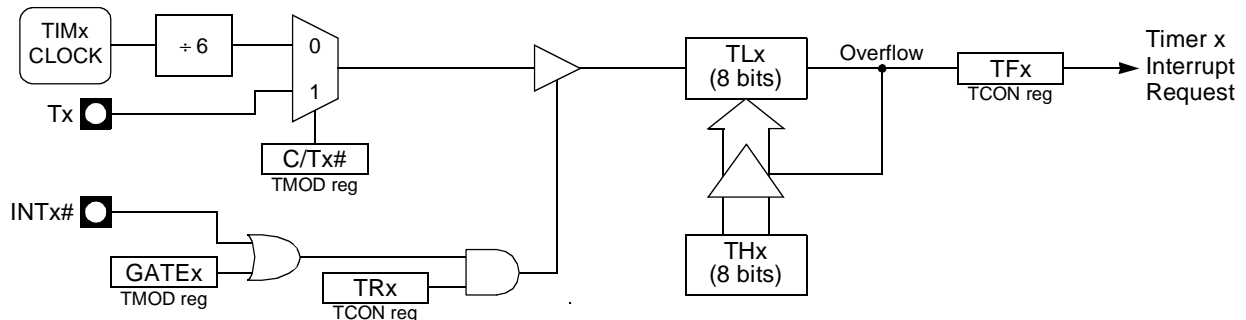


Figure 21. Mode 2 Autoreload Period Formula

$$TF_{xPER} = \frac{6 \cdot (256 - TH_x)}{F_{TIM_x}}$$

Mode 3 (Two 8-bit Timers)

Mode 3 configures Timer 0 such that registers TL0 and TH0 operate as separate 8-bit Timers (see Figure 22). This mode is provided for applications requiring an additional 8-bit Timer or Counter. TL0 uses the Timer 0 control bits C/T0# and GATE0 in TMOD register, and TR0 and TF0 in TCON register in the normal manner. TH0 is locked into a Timer function (counting $F_{T1}/6$) and takes over use of the Timer 1 interrupt (TF1) and run control (TR1) bits. Thus, operation of Timer 1 is restricted when Timer 0 is in mode 3. Figure 21 gives the autoreload period calculation formulas for both TF0 and TF1 flags.

Figure 22. Timer/Counter 0 in Mode 3: Two 8-bit Counters

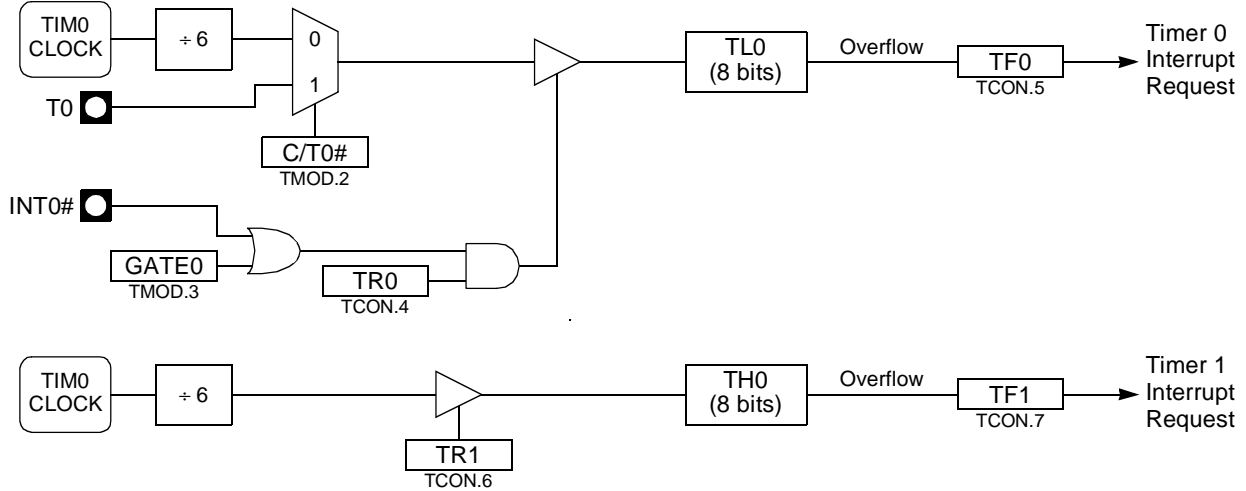


Figure 23. Mode 3 Overflow Period Formula

$$TF0_{PER} = \frac{6 \cdot (256 - TL0)}{F_{TIM0}} \qquad TF1_{PER} = \frac{6 \cdot (256 - TH0)}{F_{TIM0}}$$

Timer 1

Timer 1 is identical to Timer 0 excepted for Mode 3 which is a hold-count mode. Following comments help to understand the differences:

- Timer 1 functions as either a Timer or event Counter in three modes of operation. Figure 16 to Figure 20 show the logical configuration for modes 0, 1, and 2. Timer 1's mode 3 is a hold-count mode.
- Timer 1 is controlled by the four high-order bits of TMOD register (see Figure 45) and bits 2, 3, 6 and 7 of TCON register (see Figure 44). TMOD register selects the method of Timer gating (GATE1), Timer or Counter operation (C/T1#) and mode of operation (M11 and M01). TCON register provides Timer 1 control functions: overflow flag (TF1), run control bit (TR1), interrupt flag (IE1) and interrupt type control bit (IT1).
- Timer 1 can serve as the Baud Rate Generator for the Serial Port. Mode 2 is best suited for this purpose.
- For normal Timer operation (GATE1 = 0), setting TR1 allows TL1 to be incremented by the selected input. Setting GATE1 and TR1 allows external pin INT1# to control Timer operation.
- Timer 1 overflow (count rolls over from all 1s to all 0s) sets the TF1 flag generating an interrupt request.
- When Timer 0 is in mode 3, it uses Timer 1's overflow flag (TF1) and run control bit (TR1). For this situation, use Timer 1 only for applications that do not require an interrupt (such as a Baud Rate Generator for the Serial Port) and switch Timer 1 in and out of mode 3 to turn it off and on.
- It is important to stop the Timer/Counter before changing modes.

Mode 0 (13-bit Timer)

Mode 0 configures Timer 1 as a 13-bit Timer, which is set up as an 8-bit Timer (TH1 register) with a modulo-32 prescaler implemented with the lower 5 bits of the TL1 register (see Figure 16). The upper 3 bits of TL1 register are ignored. Prescaler overflow increments TH1 register.

Mode 1 (16-bit Timer)

Mode 1 configures Timer 1 as a 16-bit Timer with TH1 and TL1 registers connected in cascade (see Figure 18). The selected input increments TL1 register.

Mode 2 (8-bit Timer with Auto-Reload)

Mode 2 configures Timer 1 as an 8-bit Timer (TL1 register) with automatic reload from TH1 register on overflow (see Figure 20). TL1 overflow sets TF1 flag in TCON register and reloads TL1 with the contents of TH1, which is preset by software. The reload leaves TH1 unchanged.

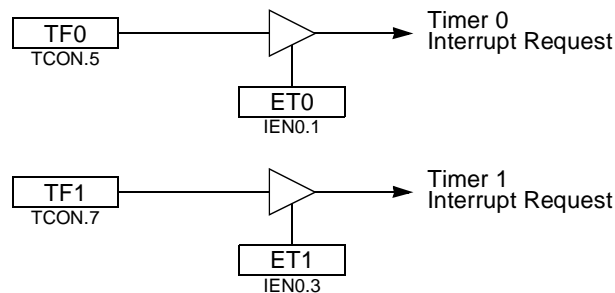
Mode 3 (Halt)

Placing Timer 1 in mode 3 causes it to halt and hold its count. This can be used to halt Timer 1 when TR1 run control bit is not available i.e. when Timer 0 is in mode 3.

Interrupt

Each Timer handles one interrupt source that is the timer overflow flag TF0 or TF1. This flag is set every time an overflow occurs. Flags are cleared when vectoring to the Timer interrupt routine. Interrupts are enabled by setting ETx bit in IEN0 register. This assumes interrupts are globally enabled by setting EA bit in IEN0 register.

Figure 24. Timer Interrupt System



Registers

Table 44. TCON Register

TCON (S:88h) – Timer/Counter Control Register

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Bit Number	Bit Mnemonic	Description					
7	TF1	Timer 1 Overflow Flag Cleared by hardware when processor vectors to interrupt routine. Set by hardware on Timer/Counter overflow, when Timer 1 register overflows.					
6	TR1	Timer 1 Run Control Bit Clear to turn off Timer/Counter 1. Set to turn on Timer/Counter 1.					
5	TF0	Timer 0 Overflow Flag Cleared by hardware when processor vectors to interrupt routine. Set by hardware on Timer/Counter overflow, when Timer 0 register overflows.					
4	TR0	Timer 0 Run Control Bit Clear to turn off Timer/Counter 0. Set to turn on Timer/Counter 0.					
3	IE1	Interrupt 1 Edge Flag Cleared by hardware when interrupt is processed if edge-triggered (see IT1). Set by hardware when external interrupt is detected on INT1# pin.					
2	IT1	Interrupt 1 Type Control Bit Clear to select low level active (level triggered) for external interrupt 1 (INT1#). Set to select falling edge active (edge triggered) for external interrupt 1.					
1	IE0	Interrupt 0 Edge Flag Cleared by hardware when interrupt is processed if edge-triggered (see IT0). Set by hardware when external interrupt is detected on INT0# pin.					
0	IT0	Interrupt 0 Type Control Bit Clear to select low level active (level triggered) for external interrupt 0 (INT0#). Set to select falling edge active (edge triggered) for external interrupt 0.					

Reset Value = 0000 0000b

Table 45. TMOD Register
 TMOD (S:89h) – Timer/Counter Mode Control Register

	7	6	5	4	3	2	1	0
	GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00

Bit Number	Bit Mnemonic	Description															
7	GATE1	Timer 1 Gating Control Bit Clear to enable Timer 1 whenever TR1 bit is set. Set to enable Timer 1 only while INT1# pin is high and TR1 bit is set.															
6	C/T1#	Timer 1 Counter/Timer Select Bit Clear for Timer operation: Timer 1 counts the divided-down system clock. Set for Counter operation: Timer 1 counts negative transitions on external pin T1.															
5	M11	Timer 1 Mode Select Bits <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="border-bottom: 1px solid black;"><u>M11</u></td> <td style="border-bottom: 1px solid black;"><u>M01</u></td> <td style="border-bottom: 1px solid black;"><u>Operating mode</u></td> </tr> <tr> <td>0</td> <td>0</td> <td>Mode 0: 8-bit Timer/Counter (TH1) with 5-bit prescaler (TL1).</td> </tr> <tr> <td>0</td> <td>1</td> <td>Mode 1: 16-bit Timer/Counter.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Mode 2: 8-bit auto-reload Timer/Counter (TL1).⁽¹⁾</td> </tr> <tr> <td>1</td> <td>1</td> <td>Mode 3: Timer 1 halted. Retains count.</td> </tr> </table>	<u>M11</u>	<u>M01</u>	<u>Operating mode</u>	0	0	Mode 0: 8-bit Timer/Counter (TH1) with 5-bit prescaler (TL1).	0	1	Mode 1: 16-bit Timer/Counter.	1	0	Mode 2: 8-bit auto-reload Timer/Counter (TL1). ⁽¹⁾	1	1	Mode 3: Timer 1 halted. Retains count.
<u>M11</u>	<u>M01</u>		<u>Operating mode</u>														
0	0		Mode 0: 8-bit Timer/Counter (TH1) with 5-bit prescaler (TL1).														
0	1		Mode 1: 16-bit Timer/Counter.														
1	0	Mode 2: 8-bit auto-reload Timer/Counter (TL1). ⁽¹⁾															
1	1	Mode 3: Timer 1 halted. Retains count.															
4	M01																
3	GATE0	Timer 0 Gating Control Bit Clear to enable Timer 0 whenever TR0 bit is set. Set to enable Timer/Counter 0 only while INT0# pin is high and TR0 bit is set.															
2	C/T0#	Timer 0 Counter/Timer Select Bit Clear for Timer operation: Timer 0 counts the divided-down system clock. Set for Counter operation: Timer 0 counts negative transitions on external pin T0.															
1	M10	Timer 0 Mode Select Bit <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="border-bottom: 1px solid black;"><u>M10</u></td> <td style="border-bottom: 1px solid black;"><u>M00</u></td> <td style="border-bottom: 1px solid black;"><u>Operating mode</u></td> </tr> <tr> <td>0</td> <td>0</td> <td>Mode 0: 8-bit Timer/Counter (TH0) with 5-bit prescaler (TL0).</td> </tr> <tr> <td>0</td> <td>1</td> <td>Mode 1: 16-bit Timer/Counter.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Mode 2: 8-bit auto-reload Timer/Counter (TL0).⁽²⁾</td> </tr> <tr> <td>1</td> <td>1</td> <td>Mode 3: TL0 is an 8-bit Timer/Counter. TH0 is an 8-bit Timer using Timer 1's TR0 and TF0 bits.</td> </tr> </table>	<u>M10</u>	<u>M00</u>	<u>Operating mode</u>	0	0	Mode 0: 8-bit Timer/Counter (TH0) with 5-bit prescaler (TL0).	0	1	Mode 1: 16-bit Timer/Counter.	1	0	Mode 2: 8-bit auto-reload Timer/Counter (TL0). ⁽²⁾	1	1	Mode 3: TL0 is an 8-bit Timer/Counter. TH0 is an 8-bit Timer using Timer 1's TR0 and TF0 bits.
<u>M10</u>	<u>M00</u>		<u>Operating mode</u>														
0	0		Mode 0: 8-bit Timer/Counter (TH0) with 5-bit prescaler (TL0).														
0	1		Mode 1: 16-bit Timer/Counter.														
1	0	Mode 2: 8-bit auto-reload Timer/Counter (TL0). ⁽²⁾															
1	1	Mode 3: TL0 is an 8-bit Timer/Counter. TH0 is an 8-bit Timer using Timer 1's TR0 and TF0 bits.															
0	M00																

Notes: 1. Reloaded from TH1 at overflow.
 2. Reloaded from TH0 at overflow.

Reset Value = 0000 0000b

Table 46. TH0 Register
 TH0 (S:8Ch) – Timer 0 High Byte Register

	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
7:0		High Byte of Timer 0.

Reset Value = 0000 0000b



Table 47. TL0 Register

TL0 (S:8Ah) – Timer 0 Low Byte Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-
Bit Number	Bit Mnemonic	Description					
7:0		Low Byte of Timer 0.					

Reset Value = 0000 0000b

Table 48. TH1 Register

TH1 (S:8Dh) – Timer 1 High Byte Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-
Bit Number	Bit Mnemonic	Description					
7:0		High Byte of Timer 1.					

Reset Value = 0000 0000b

Table 49. TL1 Register

TL1 (S:8Bh) – Timer 1 Low Byte Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-
Bit Number	Bit Mnemonic	Description					
7:0		Low Byte of Timer 1.					

Reset Value = 0000 0000b

Watchdog Timer

The AT8xC51SND1A implements a hardware Watchdog Timer (WDT) that automatically resets the chip if it is allowed to time out. The WDT provides a means of recovering from routines that do not complete successfully due to software or hardware malfunctions.

Description

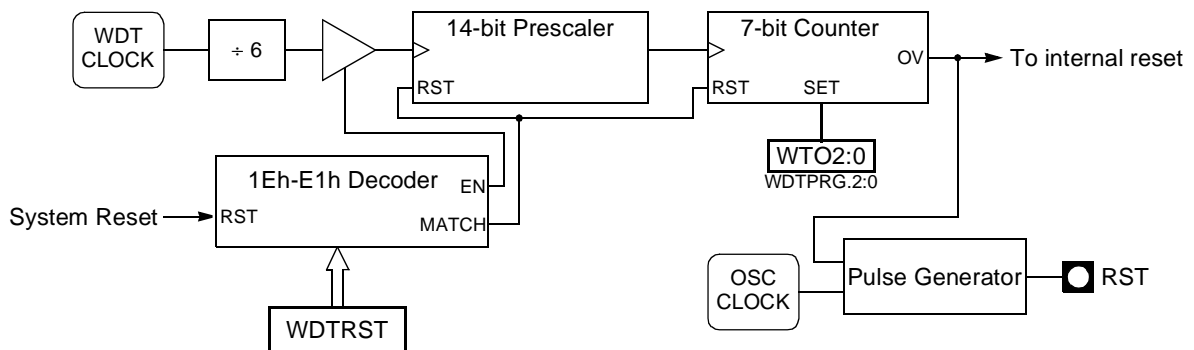
The WDT consists of a 14-bit prescaler followed by a 7-bit programmable counter. As shown in Figure 25, the 14-bit prescaler is fed by the WDT clock detailed in Section "Watchdog Clock Controller", page 53.

The Watchdog Timer Reset register (WDTRST, see Table 51) provides control access to the WDT, while the Watchdog Timer Program register (WDTPRG, see Figure 12) provides time-out period programming.

Three operations control the WDT:

- Chip reset clears and disables the WDT.
- Programming the time-out value to the WDTPRG register.
- Writing a specific two-byte sequence to the WDTRST register clears and enables the WDT.

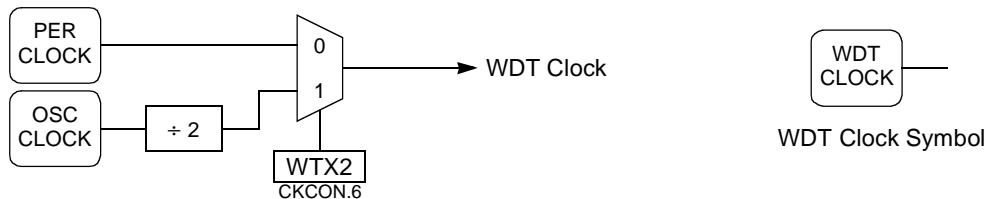
Figure 25. WDT Block Diagram



Watchdog Clock Controller

As shown in Figure 26 the WDT clock (F_{WDT}) is derived from either the peripheral clock (F_{PER}) or the oscillator clock (F_{OSC}) depending on the WTX2 bit in CKCON register. These clocks are issued from the Clock Controller block as detailed in Section "Clock Controller", page 4. When WTX2 bit is set, the WDT clock frequency is fixed and equal to the oscillator clock frequency divided by 2. When cleared, the WDT clock frequency is equal to the oscillator clock frequency divided by 2 in standard mode or to the oscillator clock frequency in X2 mode.

Figure 26. WDT Clock Controller and Symbol



Watchdog Operation

After reset, the WDT is disabled. The WDT is enabled by writing the sequence 1Eh and E1h into the WDTRST register. As soon as it is enabled, there is no way except the chip reset to disable it. If it is not cleared using the previous sequence, the WDT overflows and forces a chip reset. This overflow generates a high level 96 oscillator periods pulse on the RST pin to globally reset the application.

The WDT time-out period can be adjusted using WTO2:0 bits located in the WDTPRG register accordingly to the formula shown in Figure 11. In this formula, WTOval represents the decimal value of WTO2:0 bits. Table 50 reports the time-out period depending on the WDT frequency.

Figure 11. WDT Time-Out Formula

$$WDT_{TO} = \frac{6 \cdot ((2^{14} \cdot 2^{WTOval}) - 1)}{F_{WDT}}$$

Table 50. WDT Time-Out Computation

WTO2	WTO1	WTO0	F _{WDT}					
			6 MHz ⁽¹⁾	8 MHz ⁽¹⁾	10 MHz ⁽¹⁾	12 MHz ⁽²⁾	16 MHz ⁽²⁾	20 MHz ⁽²⁾
0	0	0	16.38 ms	12.28 ms	9.83 ms	8.19 ms	6.14 ms	4.92 ms
0	0	1	32.77 ms	24.57 ms	19.66 ms	16.38 ms	12.28 ms	9.83 ms
0	1	0	65.54 ms	49.14 ms	39.32 ms	32.77 ms	24.57 ms	19.66 ms
0	1	1	131.07 ms	98.28 ms	78.64 ms	65.54 ms	49.14 ms	39.32 ms
1	0	0	262.14 ms	196.56 ms	157.29 ms	131.07 ms	98.28 ms	78.64 ms
1	0	1	524.29 ms	393.12 ms	314.57 ms	262.14 ms	196.56 ms	157.29 ms
1	1	0	1.05 s	786.24 ms	629.15 ms	524.29 ms	393.12 ms	314.57 ms
1	1	1	2.10 s	1.57 s	1.26 s	1.05 s	786.24 ms	629.15 ms

Notes: 1. These frequencies are achieved in X1 mode, $F_{WDT} = F_{OSC} \div 2$.

2. These frequencies are achieved in X2 mode, $F_{WDT} = F_{OSC}$.

WDT Behavior During Idle and Power-down Modes

Operation of the WDT during power reduction modes deserves special attention. The WDT continues to count while the AT8xC51SND1A is in Idle mode. This means that you must dedicate some internal or external hardware to service the WDT during Idle mode. One approach is to use a peripheral Timer to generate an interrupt request when the Timer overflows. The interrupt service routine then clears the WDT, reloads the peripheral Timer for the next service period and puts the AT8xC51SND1A back into Idle mode.

The Power-down mode stops all phase clocks. This causes the WDT to stop counting and to hold its count. The WDT resumes counting from where it left off if the Power-down mode is terminated by INT0#, INT1# or keyboard interrupt. To ensure that the WDT does not overflow shortly after exiting the Power-down mode, it is recommended to clear the WDT just before entering Power-down mode.

The WDT is cleared and disabled if the Power-down mode is terminated by a reset.

Registers

Table 51. WDTRST Register

WDTRST (S:A6h Write only) – Watchdog Timer Reset Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
7 - 0	-	Watchdog Control Value.

Reset Value = XXXX XXXXb

Figure 12. WDTPRG Register

WDTPRG (S:A7h) – Watchdog Timer Program Register

7	6	5	4	3	2	1	0
-	-	-	-	-	WTO2	WTO1	WTO0

Bit Number	Bit Mnemonic	Description
7-3	-	Reserved The value read from these bits is indeterminate. Do not set these bits.
2-0	WTO2:0	Watchdog Timer Time-Out Selection Bits Refer to Table 50 for time-out periods.

Reset Value = XXXX X000b=

MP3 Decoder

The AT8xC51SND1A implements a MPEG I/II audio layer 3 decoder better known as MP3 decoder.

In MPEG I (ISO 11172-3) three layers of compression have been standardized supporting three sampling frequencies: 48, 44.1, and 32 kHz. Among these layers, layer 3 allows highest compression rate of about 12:1 while still maintaining CD audio quality. For example, 3 minutes of CD audio (16-bit PCM, 44.1 kHz) data, which needs about 32M Bytes of storage, can be encoded into only 2.7M Bytes of MPEG I audio layer 3 data.

In MPEG II (ISO 13818-3), three additional sampling frequencies: 24, 22.05, and 16 kHz are supported for low bit rates applications.

The AT8xC51SND1A can decode in real-time the MPEG I audio layer 3 encoded data into a PCM audio data, and also supports MPEG II audio layer 3 additional frequencies.

Additional features are supported by the AT8xC51SND1A MP3 decoder such as volume control, bass, medium, and treble controls, bass boost effect and ancillary data extraction.

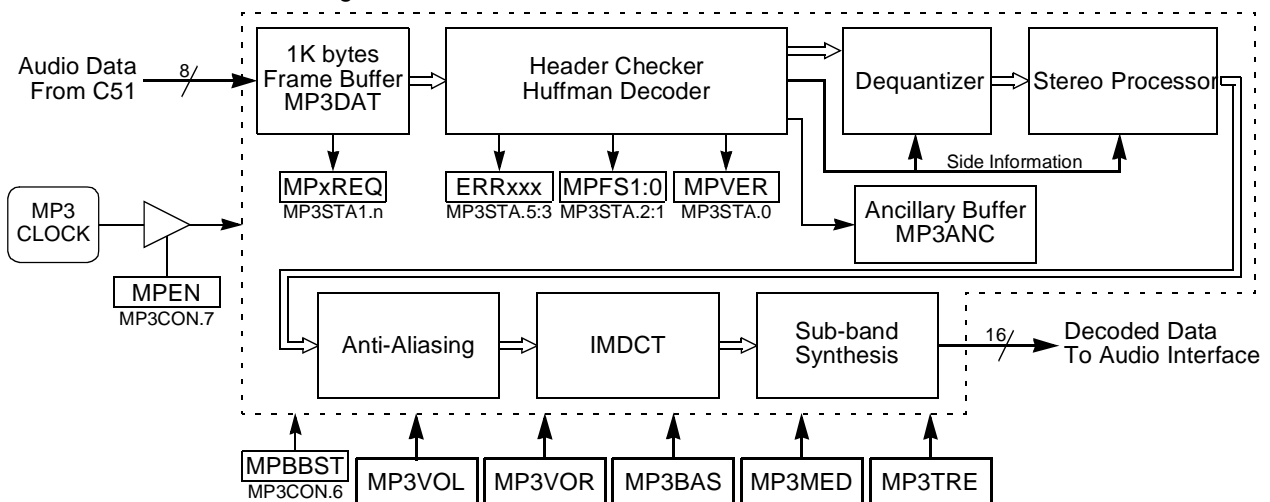
Decoder

Description

The C51 core interfaces to the MP3 decoder through nine special function registers: MP3CON, the MP3 Control register (see Table 57); MP3STA, the MP3 Status register (see Table 58); MP3DAT, the MP3 Data register (see Table 59); MP3ANC, the Ancillary Data register (see Table 60); MP3VOL and MP3VOR, the MP3 Volume Left and Right Control registers (see Table 61 and Table 62); MP3BAS, MP3MED, and MP3TRE, the MP3 Bass, Medium, and Treble Control registers (see Table 63, Table 64, and Table 65); and MPCLK, the MP3 Clock Divider register (see Table 66).

Figure 27 shows the MP3 decoder block diagram.

Figure 27. MP3 Decoder Block Diagram



MPEG I Limitations

In order to optimize the MP3 decoder, in MPEG I version some bit rates are not achievable due to frame size for such bit rates. Table 52 shows the available decoded bit rates depending on the sampling frequency. All the available bit rates are achievable in MPEG II version.

Table 52. MPEG I Decoding Bit Rates

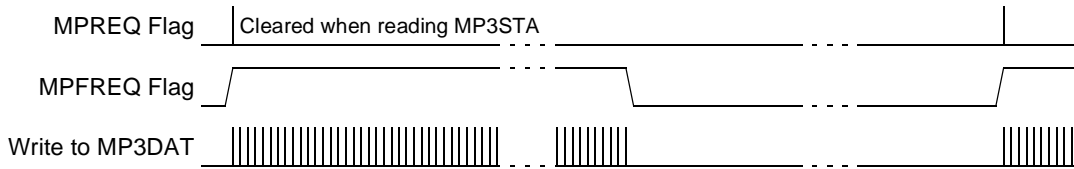
Description	Bit Rate (kHz)													
	32	40	48	56	64	80	96	112	128	160	192	224	256	320
Sample Frequency (kHz)														
32	X	X	X	X	X	X	X	X	X	X	X	X		
44.1	X	X	X	X	X	X	X	X	X	X	X	X	X	
48	X	X	X	X	X	X	X	X	X	X	X	X	X	X

MP3 Data

The MP3 decoder does not start any frame decoding before having a complete frame in its input buffer⁽¹⁾. In order to manage the load of MP3 data in the frame buffer, a hardware handshake consisting of data request and data acknowledgment is implemented. Each time the MP3 decoder needs MP3 data, it sets the MPREQ and MPFREQ flags respectively in MP3STA and MP3STA1 registers. MPREQ flag can generate an interrupt if enabled as explained in Section . The CPU must then load data in the buffer by writing it through MP3DAT register thus acknowledging the previous request. As shown in Figure 28, the MPFREQ flag remains set while data is requested by the decoder. It is cleared when no more data is requested and set again when new data are requested.

Note: 1. The first request after enable, consists in 1024 bytes of data to fill in the input buffer.

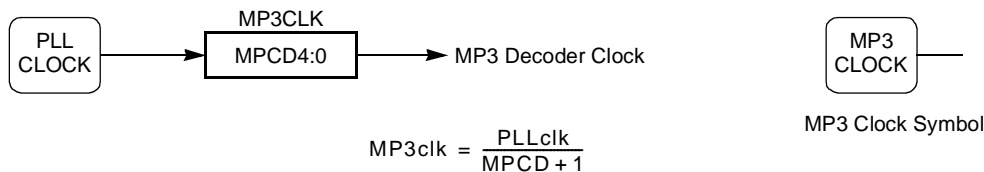
Figure 28. Data Timing Diagram



MP3 Clock

The MP3 decoder clock is generated by division of the PLL clock. The division factor is given by MPCD4:0 bits in MP3CLK register. Figure 29 shows the MP3 decoder clock generator and its calculation formula. The MP3 decoder clock frequency depends only on the incoming MP3 frames.

Figure 29. MP3 Clock Generator and Symbol



As soon as the frame header has been decoded and the MPEG version extracted, the minimum MP3 input frequency must be programmed according to Table 53.

Table 53. MP3 Clock Frequency

MPEG Version	Minimum MP3 Clock (MHz)
I	21
II	10.5

Audio Controls

Volume Control

The MP3 decoder implements volume control on both right and left channels. The MP3VOR and MP3VOL registers allow a 32-step volume control according to Table 54.

Table 54. Volume Control

VOL4:0 or VOR4:0	Volume Gain (dB)
00000	Mute
00001	-33
00010	-27
11110	-1.5
11111	0

Equalization Control

Sound can be adjusted using a 3-band equalizer: a bass band under 680 Hz, a medium band from 680 Hz to 4080 Hz and a treble band over 4080 kHz. The MP3BAS, MP3MED, and MP3TRE registers allow a 32-step gain control in each band according to Table 55.

Table 55. Bass, Medium, Treble Control

BAS4:0 or MED4:0 or TRE4:0	Gain (dB)
00000	-∞
00001	-14
00010	-10
11110	+1
11111	+1.5

Special Effect

The MPBBST bit in MP3CON register allows enabling of a bass boost effect with the following characteristics: gain increase of +15 dB in the frequency under 120 Hz and gain increase of +6 dB in the frequency range 120 to 240 Hz.

Decoding Errors

The three different errors that can appear during frame processing are detailed in the following sections. All these errors can trigger an interrupt as explained in Section "Interrupt", page 60.

Layer Error

The ERRSYN flag in MP3STA is set when a non-supported layer is decoded in the header of the frame that has been sent to the decoder.

Synchronization Error

The ERRSYN flag in MP3STA is set when no synchronization pattern is found in the data that have been sent to the decoder.

CRC Error

When the CRC of a frame does not match the one calculated, the flag ERRCRC in MP3STA is set. In this case, depending on the CRCEN bit in MP3CON, the frame is played or rejected. In both cases, noise may appear at audio output.

Frame Information

The MP3 frame header contains information on the audio data contained in the frame. These informations are made available in the MP3STA register for you information. MPVER and MPFS1:0 bits allow decoding of the sampling frequency according to Table 56. MPVER bit gives the MPEG version (2 or 1).

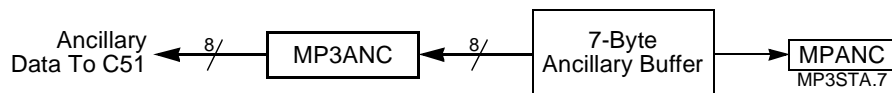
Table 56. MP3 Frame Frequency Sampling

MPVER	MPFS1	MPFS0	Fs (kHz)
0	0	0	22.05 (MPEG II)
0	0	1	24 (MPEG II)
0	1	0	16 (MPEG II)
0	1	1	Reserved
1	0	0	44.1 (MPEG I)
1	0	1	48 (MPEG I)
1	1	0	32 (MPEG I)
1	1	1	Reserved

Ancillary Data

MP3 frames also contain data bits called ancillary data. These data are made available in the MP3ANC register for each frame. As shown in Figure 13, the ancillary data are available by bytes when MPANC flag in MP3STA register is set. MPANC flag is set when the ancillary buffer is not empty (at least one ancillary data is available) and is cleared only when there is no more ancillary data in the buffer. This flag can generate an interrupt as explained in Section "Interrupt", page 60. When set, software must read all bytes to empty the ancillary buffer.

Figure 13. Ancillary Data Block Diagram

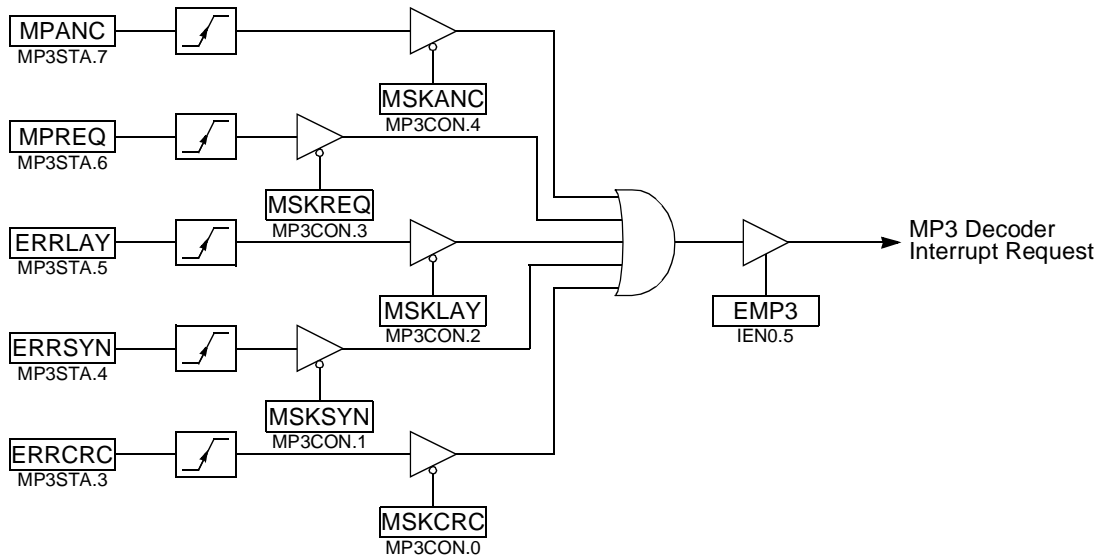


Interrupt

Description

As shown in Figure 30, the MP3 decoder implements five interrupt sources reported in ERRCRC, ERRSYN, ERRLAY, MPREQ, and MPANC flags in MP3STA register. All these sources are maskable separately using MSKCRC, MSKSYN, MSKLAY, MSKREQ, and MSKANC mask bits respectively in MP3CON register. The MP3 interrupt is enabled by setting ESMP3 bit in IEN0 register. This assumes interrupts are globally enabled by setting EA bit in IEN0 register. All interrupt flags but MPREQ and MPANC are cleared when reading MP3STA register. The MPREQ flag is cleared by hardware when no more data is requested (see Figure 28) and MPANC flag is cleared by hardware when the ancillary buffer becomes empty.

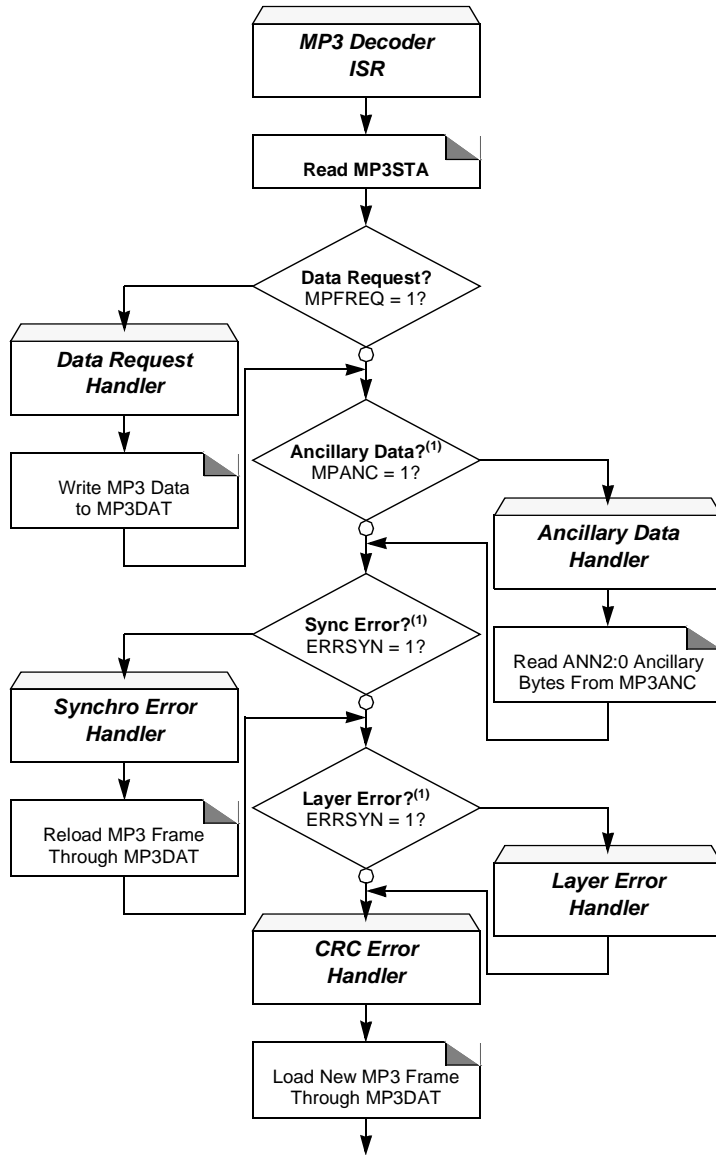
Figure 30. MP3 Decoder Interrupt System



Management

Reading the MP3STA register automatically clears the interrupt flags (acknowledgment) except the MPREQ and MPANC flags. This implies that register content must be saved and tested, interrupt flag by interrupt flag to be sure not to forget any interrupts.

Figure 31. MP3 Interrupt Service Routine Flow



Note: 1. Test these bits only if needed (unmasked interrupt).

Registers

Table 57. MP3CON Register

MP3CON (S:AAh) – MP3 Decoder Control Register

7	6	5	4	3	2	1	0
MPEN	MPBBST	CRCEN	MSKANC	MSKREQ	MSKLAY	MSKSYN	MSKCRC
Bit Number	Bit Mnemonic	Description					
7	MPEN	MP3 Decoder Enable Bit Set to enable the MP3 decoder. Clear to disable the MP3 decoder.					
6	MPBBST	Bass Boost Bit Set to enable the bass boost sound effect. Clear to disable the bass boost sound effect.					
5	CRCEN	CRC Check Enable Bit Set to enable processing of frame that contains CRC error. Frame is played whatever the error. Clear to disable processing of frame that contains CRC error. Frame is skipped.					
4	MSKANC	MPANC Flag Mask Bit Set to prevent the MPANC flag from generating a MP3 interrupt. Clear to allow the MPANC flag to generate a MP3 interrupt.					
3	MSKREQ	MPREQ Flag Mask Bit Set to prevent the MPREQ flag from generating a MP3 interrupt. Clear to allow the MPREQ flag to generate a MP3 interrupt.					
2	MSKLAY	ERRLAY Flag Mask Bit Set to prevent the ERRLAY flag from generating a MP3 interrupt. Clear to allow the ERRLAY flag to generate a MP3 interrupt.					
1	MSKSYN	ERRSYN Flag Mask Bit Set to prevent the ERRSYN flag from generating a MP3 interrupt. Clear to allow the ERRSYN flag to generate a MP3 interrupt.					
0	MSKCRC	ERRCRC Flag Mask Bit Set to prevent the ERRCRC flag from generating a MP3 interrupt. Clear to allow the ERRCRC flag to generate a MP3 interrupt.					

Reset Value = 0011 1111b

Table 58. MP3STA Register

MP3STA (S:C8h Read Only) – MP3 Decoder Status Register

	7	6	5	4	3	2	1	0
	MPANC	MPREQ	ERRLAY	ERRSYN	ERRCRC	MPFS1	MPFS0	MPVER

Bit Number	Bit Mnemonic	Description
7	MPANC	Ancillary Data Available Flag Set by hardware as soon as one ancillary data is available (buffer not empty). Cleared by hardware when no more ancillary data is available (buffer empty).
6	MPREQ	MP3 Data Request Flag Set by hardware when MP3 decoder request data. Cleared when reading MP3STA.
5	ERRLAY	Invalid Layer Error Flag Set by hardware when an invalid layer is encountered. Cleared when reading MP3STA.
4	ERRSYN	Frame Synchronization Error Flag Set by hardware when no synchronization pattern is encountered in a frame. Cleared when reading MP3STA.
3	ERRCRC	CRC Error Flag Set by hardware when a frame handling CRC is corrupted. Cleared when reading MP3STA.
2-1	MPFS1:0	Frequency Sampling Bits Refer to Table 56 for bits description.
0	MPVER	MPEG Version Bit Set by the MP3 decoder when the loaded frame is a MPEG-I frame. Cleared by the MP3 decoder when the loaded frame is a MPEG-II frame.

Reset Value = 0000 0001b

Table 59. MP3DAT Register

MP3DAT (S:ACh) – MP3 Data Register

	7	6	5	4	3	2	1	0
	MPD7	MPD6	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0

Bit Number	Bit Mnemonic	Description
7 - 0	MPD7:0	Input Stream Data Buffer 8-bit MP3 stream data input buffer.

Reset Value = 0000 0000b



Table 60. MP3ANC Register

MP3ANC (S:ADh Read Only) – MP3 Ancillary Data Register

7	6	5	4	3	2	1	0
AND7	AND6	AND5	AND4	AND3	AND2	AND1	AND0
Bit Number	Bit Mnemonic	Description					
7 - 0	AND7:0	Ancillary Data Buffer MP3 ancillary data byte buffer.					

Reset Value = 0000 0000b

Table 61. MP3VOL Register

MP3VOL (S:9Eh) – MP3 Volume Left Control Register

7	6	5	4	3	2	1	0
-	-	-	VOL4	VOL3	VOL2	VOL1	VOL0
Bit Number	Bit Mnemonic	Description					
7-5	-	Reserved The value read from these bits is always 0. Do not set these bits.					
4-0	VOL4:0	Volume Left Value Refer to Table 54 for the left channel volume control description.					

Reset Value = 0000 0000b

Table 62. MP3VOR Register

MP3VOR (S:9Fh) – MP3 Volume Right Control Register

7	6	5	4	3	2	1	0
-	-	-	VOR4	VOR3	VOR2	VOR1	VOR0
Bit Number	Bit Mnemonic	Description					
7-5	-	Reserved The value read from these bits is always 0. Do not set these bits.					
4-0	VOR4:0	Volume Right Value Refer to Table 54 for the right channel volume control description.					

Reset Value = 0000 0000b

Table 63. MP3BAS Register

MP3BAS (S:B4h) – MP3 Bass Control Register

7	6	5	4	3	2	1	0
-	-	-	BAS4	BAS3	BAS2	BAS1	BAS0

Bit Number	Bit Mnemonic	Description
7-5	-	Reserved The value read from these bits is always 0. Do not set these bits.
4-0	BAS4:0	Bass Gain Value Refer to Table 55 for the bass control description.

Reset Value = 0000 0000b

Table 64. MP3MED Register

MP3MED (S:B5h) – MP3 Medium Control Register

7	6	5	4	3	2	1	0
-	-	MED5	MED4	MED3	MED2	MED1	MED0

Bit Number	Bit Mnemonic	Description
7-6	-	Reserved The value read from these bits is always 0. Do not set these bits.
5-0	MED5:0	Medium Gain Value Refer to Table 55 for the medium control description.

Reset Value = 0000 0000b

Table 65. MP3TRE Register

MP3TRE (S:B6h) – MP3 Treble Control Register

7	6	5	4	3	2	1	0
-	-	TRE5	TRE4	TRE3	TRE2	TRE1	TRE0

Bit Number	Bit Mnemonic	Description
7-6	-	Reserved The value read from these bits is always 0. Do not set these bits.
5-0	TRE5:0	Treble Gain Value Refer to Table 55 for the treble control description.

Reset Value = 0000 0000b



Table 66. MP3CLK Register

MP3CLK (S:EBh) – MP3 Clock Divider Register

7	6	5	4	3	2	1	0
-	-	-	MPCD4	MPCD3	MPCD2	MPCD1	MPCD0
Bit Number	Bit Mnemonic	Description					
7-5	-	Reserved The value read from these bits is always 0. Do not set these bits.					
4-0	MPCD4:0	MP3 Decoder Clock Divider 5-bit divider for MP3 decoder clock generation.					

Reset Value = 0000 0000b

Audio Output Interface

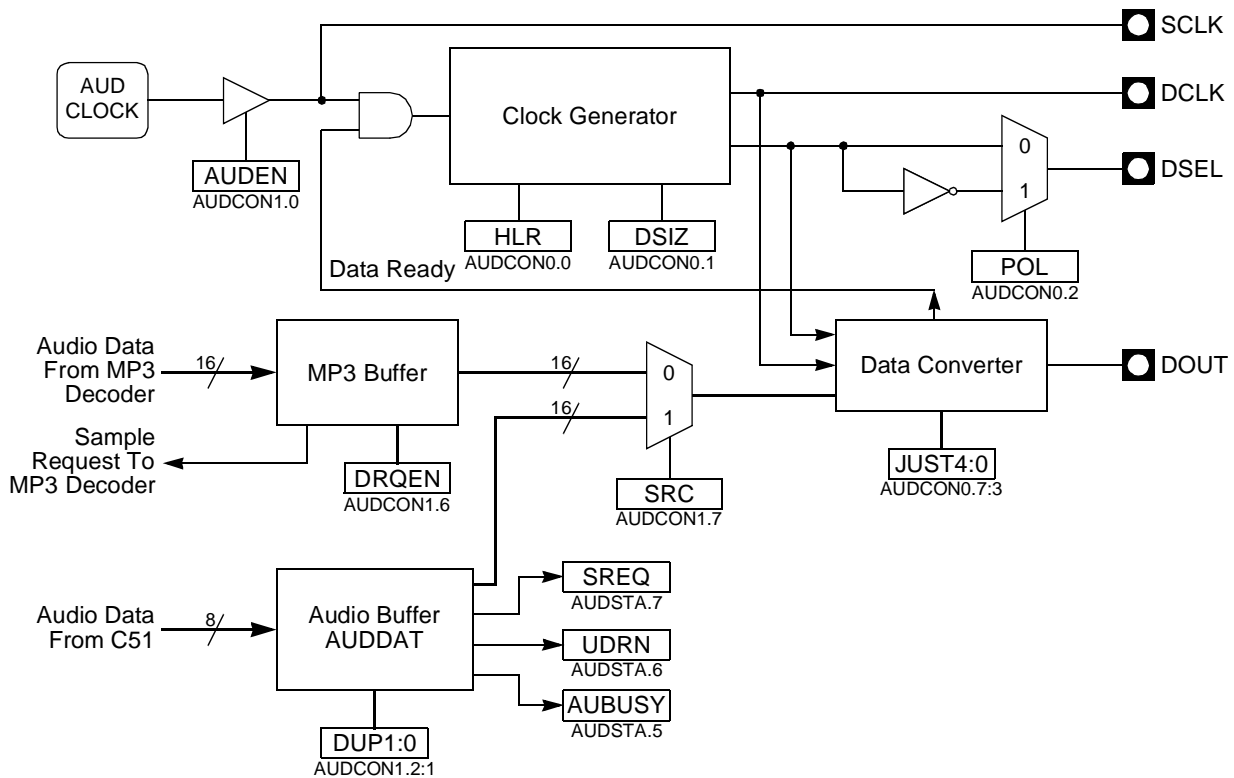
The T8xC51SND1 implements an audio output interface allowing the audio bitstream to be output in various formats. It is compatible with right and left justification PCM and I²S formats and thanks to the on-chip PLL (see Section “Clock Controller”, page 4) allows connection of almost all of the commercial audio DAC families available on the market. The audio bitstream can be from two different types:

- The MP3 decoded bitstream coming from the MP3 decoder for playing songs.
- The audio bitstream coming from the MCU for outputting voice or sounds.

Description

The C51 core interfaces to the audio interface through five special function registers: AUDCON0 and AUDCON1, the Audio Control registers (see Table 68 and Table 69); AUDSTA, the Audio Status register (see Table 70); AUDDAT, the Audio Data register (see Table 71); and AUDCLK, the Audio Clock Divider register (see Table 72). Figure 32 shows the audio interface block diagram, blocks are detailed in the following sections.

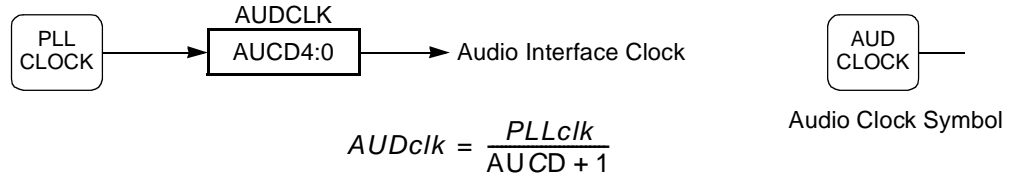
Figure 32. Audio Interface Block Diagram



Clock Generator

The audio interface clock is generated by division of the PLL clock. The division factor is given by AUCD4:0 bits in CLKAUD register. Figure 14 shows the audio interface clock generator and its calculation formula. The audio interface clock frequency depends on the incoming MP3 frames and the audio DAC used.

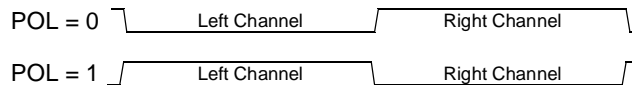
Figure 14. Audio Clock Generator and Symbol



As soon as audio interface is enabled by setting AUDEN bit in AUDCON1 register, the master clock generated by the PLL is output on the SCLK pin which is the DAC system clock. This clock is output at 256 or 384 times the sampling frequency depending on the DAC capabilities. HLR bit in AUDCON0 register must be set according to this rate for properly generating the audio bit clock on the DCLK pin and the word selection clock on the DSEL pin. These clocks are not generated when no data is available at the data converter input.

For DAC compatibility, the bit clock frequency is programmable for outputting 16 bits or 32 bits per channel using the DSIZ bit in AUDCON0 register (see Section "Data Converter", page 68), and the word selection signal is programmable for outputting left channel on low or high level according to POL bit in AUDCON0 register as shown in Figure 15.

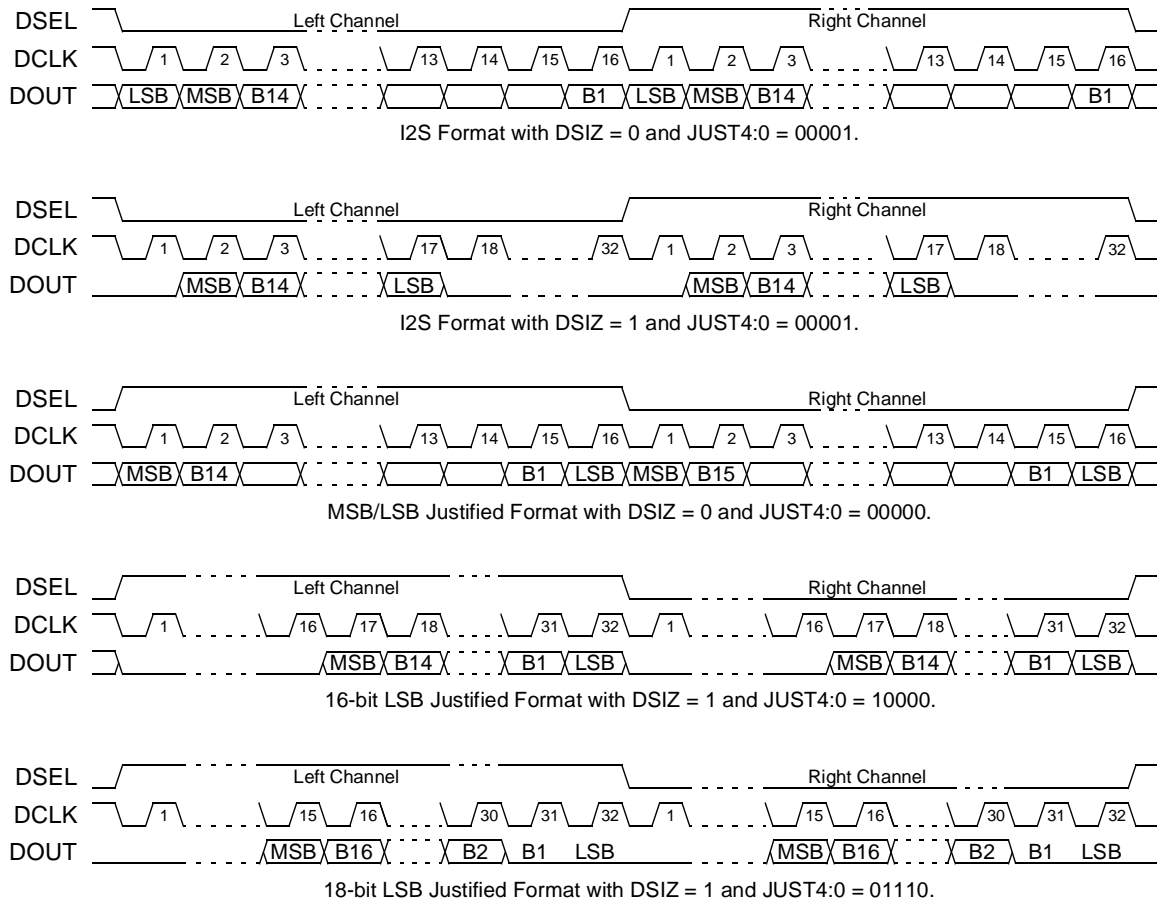
Figure 15. DSEL Output Polarity



Data Converter

The data converter block converts the audio stream input from the 16-bit parallel format to a serial format. For accepting all PCM formats and I²S format, JUST4:0 bits in AUDCON0 register are used to shift the data output point. As shown in Figure 33, these bits allow MSB justification by setting JUST4:0 = 00000, LSB justification by setting JUST4:0 = 10000, I²S Justification by setting JUST4:0 = 00001, and more than 16-bit LSB justification by filling the low significant bits with logic 0.

Figure 33. Audio Output Format



The data converter receives its audio stream from two sources selected by the SRC bit in AUDCON1 register. When cleared, the audio stream comes from the MP3 decoder (see Section “MP3 Decoder”, page 56) for song playing. When set, the audio stream is coming from the C51 core for voice or sound playing. As soon as first audio data is input to the data converter, it enables the clock generator for generating the bit and word clocks.

Audio Buffer

In voice or sound playing mode, the audio stream comes from the C51 core through an audio buffer. The data is 8-bit format and is sampled at 8 kHz. The audio buffer adapts the sample format and rate. The sample format is extended to 16 bits by filling the LSB to 00h. Rate is adapted to the DAC rate by duplicating the data using DUP1:0 bits in AUDCON1 register according to Table 67.

The audio buffer interfaces to the C51 core through three flags: the sample request flag (SREQ in AUDSTA register), the under-run flag (UNDR in AUDSTA register) and the busy flag (AUBUSY in AUDSTA register). SREQ and UNDR can generate an interrupt request as explained in Section "Interrupt Request", page 70. The buffer size is 8 bytes large. SREQ is set when the samples number switches from 4 to 3 and reset when the samples number switches from 4 to 5; UNDR is set when the buffer becomes empty signaling that the audio interface ran out of samples; and AUBUSY is set when the buffer is full.

Table 67. Sample Duplication Factor

DUP1	DUP0	Factor
0	0	No sample duplication, DAC rate = 8 kHz (C51 rate).
0	1	One sample duplication, DAC rate = 16 kHz (2 x C51 rate).
1	0	Two samples duplication, DAC rate = 32 kHz (4 x C51 rate).
1	1	Three samples duplication, DAC rate = 48 kHz (6 x C51 rate).

MP3 Buffer

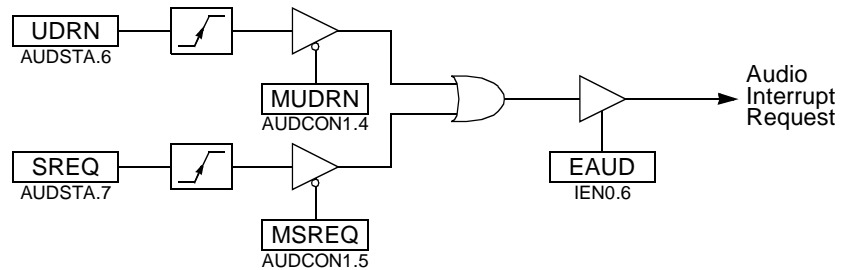
In song playing mode, the audio stream comes from the MP3 decoder through a buffer. The MP3 buffer is used to store the decoded MP3 data and interfaces to the decoder through a 16-bit data input and data request signal. This signal asks for data when the buffer has enough space to receive new ones. Data request is conditioned by the DREQEN bit in AUDCON1 register. When set, the buffer requests data to the MP3 decoder. When cleared no more data is requested but data are output until the buffer becomes empty. This bit can be used to suspend the audio generation (pause mode).

Interrupt Request

The audio interrupt request can be generated by two sources when in C51 audio mode: a sample request when SREQ flag in AUDSTA register is set to logic 1, and an under-run condition when UDRN flag in AUDSTA register is set to logic 1. Both sources can be enabled separately by masking one of them using the MSREQ and MUDRN bits in AUDCON1 register. A global enable of the audio interface is provided by setting the EAUD bit in IEN0 register.

The interrupt is requested each time one of the two sources is set to one. The source flags are cleared by writing some data in the audio buffer through AUDDAT, but the global audio interrupt flag is cleared by hardware when the interrupt service routine is executed.

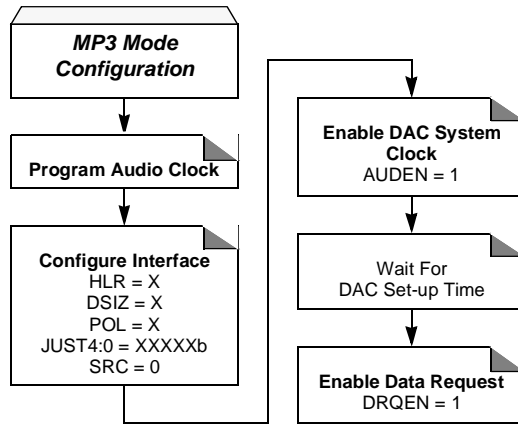
Figure 16. Audio Interface Interrupt System



MP3 Song Playing

In MP3 song playing mode, the operations to do are to configure the PLL and the audio interface according to the DAC selected. The audio clock is programmed to generate the 256-Fs or 384-Fs as explained in Section "Clock Generator", page 68. Figure 34 shows the configuration flow of the audio interface when in MP3 song mode.

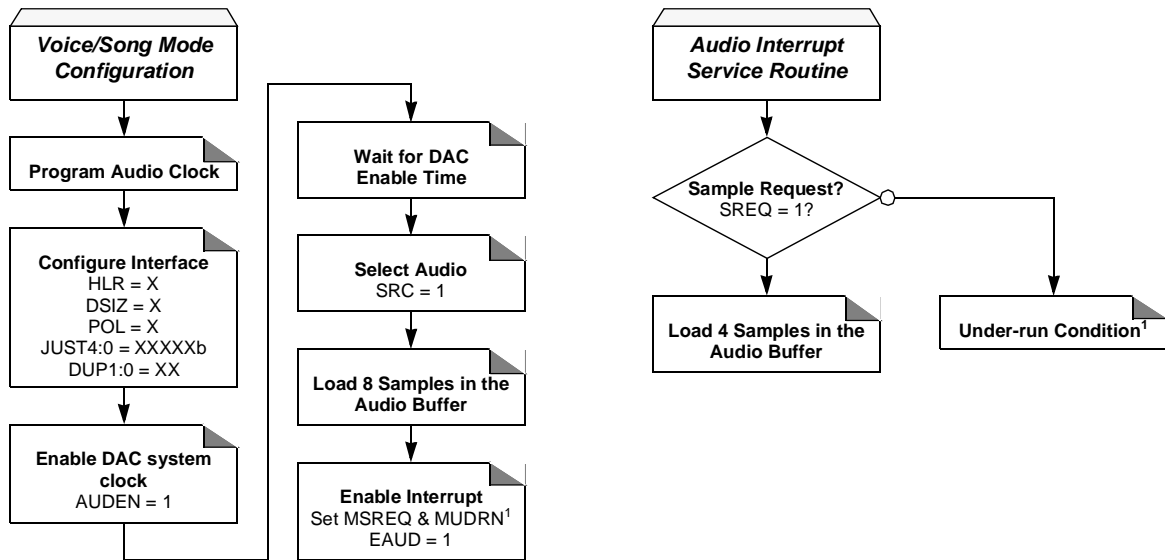
Figure 34. MP3 Mode Audio Configuration Flow



Voice or Sound Playing

In voice or sound playing mode, the operations required are to configure the PLL and the audio interface according to the DAC selected. The audio clock is programmed to generate the 256-Fs or 384-Fs as for the MP3 playing mode. The data flow sent by the C51 is then regulated by interrupt and data is loaded 4 bytes by 4 bytes. Figure 35 shows the configuration flow of the audio interface when in voice or sound mode.

Figure 35. Voice or Sound Mode Audio Flows



Note: 1. An under-run occurrence signifies that C51 core did not respond to the previous sample request interrupt. It may never occur for a correct voice/sound generation. It is your responsibility to mask it or not.

Registers

Table 68. AUDCON0 Register

AUDCON0 (S:9Ah) – Audio Interface Control Register 0

7	6	5	4	3	2	1	0
JUST4	JUST3	JUST2	JUST1	JUST0	POL	DSIZ	HLR
Bit Number	Bit Mnemonic	Description					
7-3	JUST4:0	Audio Stream Justification Bits Refer to Section "Data Converter", page 68 for bits description.					
2	POL	DSEL Signal Output Polarity Set to output the left channel on high level of DSEL output (PCM mode). Clear to output the left channel on the low level of DSEL output (I ² S mode).					
1	DSIZ	Audio Data Size Set to select 32-bit data output format. Clear to select 16-bit data output format.					
0	HLR	High/Low Rate Bit Set by software when the PLL clock frequency is 384-Fs. Clear by software when the PLL clock frequency is 256-Fs.					

Reset Value = 0000 1000b

Table 69. AUDCON1 Register

AUDCON1 (S:9Bh) – Audio Interface Control Register 1

7	6	5	4	3	2	1	0
SRC	DRQEN	MSREQ	MUDRN	-	DUP1	DUP0	AUDEN
Bit Number	Bit Mnemonic	Description					
7	SRC	Audio Source Bit Set to select C51 as audio source for voice or sound playing. Clear to select the MP3 decoder output as audio source for song playing.					
6	DRQEN	MP3 Decoded Data Request Enable Bit Set to enable data request to the MP3 decoder and to start playing song. Clear to disable data request to the MP3 decoder.					
5	MSREQ	Audio Sample Request Flag Mask Bit Set to prevent the SREQ flag from generating an audio interrupt. Clear to allow the SREQ flag to generate an audio interrupt.					
4	MUDRN	Audio Sample Under-run Flag Mask Bit Set to prevent the UDRN flag from generating an audio interrupt. Clear to allow the UDRN flag to generate an audio interrupt.					
3	-	Reserved The value read from this bit is always 0. Do not set this bit.					
2-1	DUP1:0	Audio Duplication Factor Refer to Table 67 for bits description.					
0	AUDEN	Audio Interface Enable Bit Set to enable the audio interface. Clear to disable the audio interface.					

Reset Value = 1011 0010b

Table 70. AUDSTA Register
AUDSTA (S:9Ch Read Only) – Audio Interface Status Register

7	6	5	4	3	2	1	0
SREQ	UDRN	AUBUSY	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
7	SREQ	Audio Sample Request Flag Set in C51 audio source mode when the audio interface request samples (buffer half empty). This bit generates an interrupt if not masked and if enabled in IEN0. Cleared by hardware when samples are loaded in AUDDAT.
6	UDRN	Audio Sample Under-run Flag Set in C51 audio source mode when the audio interface runs out of samples (buffer empty). This bit generates an interrupt if not masked and if enabled in IEN0. Cleared by hardware when samples are loaded in AUDDAT.
5	AUBUSY	Audio Interface Busy Bit Set in C51 audio source mode when the audio interface can not accept more sample (buffer full). Cleared by hardware when buffer is no more full.
4-0	-	Reserved The value read from these bits is always 0. Do not set these bits.

Reset Value = 1100 0000b

Table 71. AUDDAT Register
AUDDAT (S:9Dh) – Audio Interface Data Register

7	6	5	4	3	2	1	0
AUD7	AUD6	AUD5	AUD4	AUD3	AUD2	AUD1	AUD0

Bit Number	Bit Mnemonic	Description
7 - 0	AUD7:0	Audio Data 8-bit sampling data for voice or sound playing.

Reset Value = 1111 1111b

Table 72. AUDCLK Register
AUDCLK (S:ECh) – Audio Clock Divider Register

7	6	5	4	3	2	1	0
-	-	-	AUCD4	AUCD3	AUCD2	AUCD1	AUCD0

Bit Number	Bit Mnemonic	Description
7-5	-	Reserved The value read from these bits is always 0. Do not set these bits.
4-0	AUCD4:0	Audio Clock Divider 5-bit divider for audio clock generation.

Reset Value = 0000 0000b



Universal Serial Bus

The AT8xC51SND1A implements an Universal Serial Bus (USB) device controller supporting Full-speed data transfer. In addition to the default control endpoint 0, it provides 3 other endpoints, which can be configured in Control, Bulk, Interrupt or Isochronous types.

This allows to develop firmware conforming to most USB device classes, for example the AT8xC51SND1A supports:

- USB Mass Storage Class Control/Bulk/Interrupt (CBI) Transport, Revision 1.0 – December 14, 1998
- USB Mass Storage Class Bulk-Only Transport, Revision 1.0 – September 31, 1999
- USB Device Firmware Upgrade Class, Revision 1.0 – May 13, 1999

USB Mass Storage Class CBI Transport

Within the CBI framework, the Control endpoint is used to transport command blocks as well as to transport standard USB requests. One Bulk Out endpoint is used to transport data from the host to the device. One Bulk In endpoint is used to transport data from the device to the host. And one interrupt endpoint may also be used to signal command completion (protocol 0) but it is optional and may not be used (protocol 1).

The following AT8xC51SND1A configuration adheres to that requirements:

- Endpoint 0: 32 bytes, Control In-Out
- Endpoint 1: 64 bytes, Bulk Out
- Endpoint 2: 64 bytes, Bulk In
- Endpoint 3: 8 bytes, Interrupt In

USB Mass Storage Class Bulk-Only Transport

Within the Bulk-only framework, the Control endpoint is only used to transport class-specific and standard USB requests for device set-up and configuration. One Bulk-out endpoint is used to transport commands and data from the host to the device. One Bulk in endpoint is used to transport status and data from the device to the host. No interrupt endpoint is needed.

The following AT8xC51SND1A configuration adheres to that requirements:

- Endpoint 0: 32 bytes, Control In-Out
- Endpoint 1: 64 bytes, Bulk Out
- Endpoint 2: 64 bytes, Bulk In
- Endpoint 3: not used

USB Device Firmware Upgrade (DFU)

The USB Device Firmware Update (DFU) protocol can be used to upgrade the on-chip Flash memory of the AT89C51SND1A. This allows installing product enhancements and patches to devices that are already in the field. Two different configurations and descriptor sets are used to support DFU functions. The Run-Time configuration co-exist with the usual functions of the device, which shall be USB Mass Storage for AT89C51SND1A. It is used to initiate DFU from the normal operating mode. The DFU configuration is used to perform the firmware update after device re-configuration and USB reset. It excludes any other function. Only the default control pipe (endpoint 0) is used to support DFU services in both configurations.

The only possible value for the MaxPacketSize in the DFU configuration is 32 bytes, which is the size of the FIFO implemented for endpoint 0.

Description

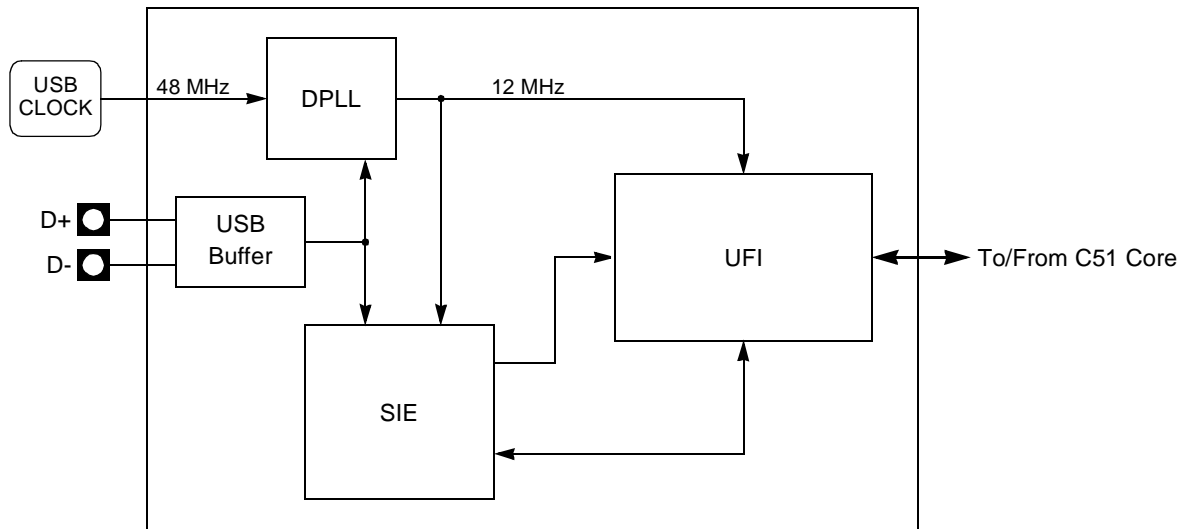
The USB device controller provides the hardware that the AT8xC51SND1A needs to interface a USB link to a data flow stored in a double port memory.

It requires a 48 MHz reference clock provided by the clock controller as detailed in Section "Clock Controller", page 75. This clock is used to generate a 12 MHz Full Speed bit clock from the received USB differential data flow and to transmit data according to full speed USB device tolerance. Clock recovery is done by a Digital Phase Locked Loop (DPLL) block.

The Serial Interface Engine (SIE) block performs NRZI encoding and decoding, bit stuffing, CRC generation and checking, and the serial-parallel data conversion.

The Universal Function Interface (UFI) controls the interface between the data flow and the Dual Port Ram, but also the interface with the C51 core itself.

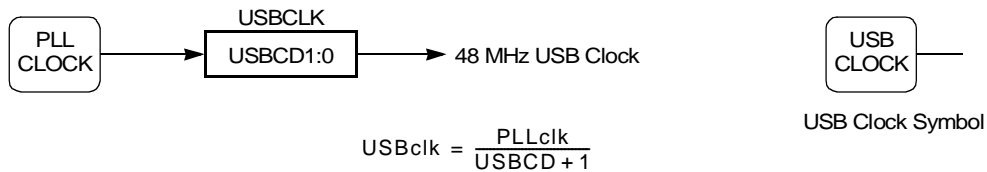
Figure 36. USB Device Controller Block Diagram



Clock Controller

The USB controller clock is generated by division of the PLL clock. The division factor is given by USBCD1:0 bits in USBCLK register (see Table 87). Figure 37 shows the USB controller clock generator and its calculation formula. The USB controller clock frequency must always be 48 MHz.

Figure 37. USB Clock Generator and Symbol

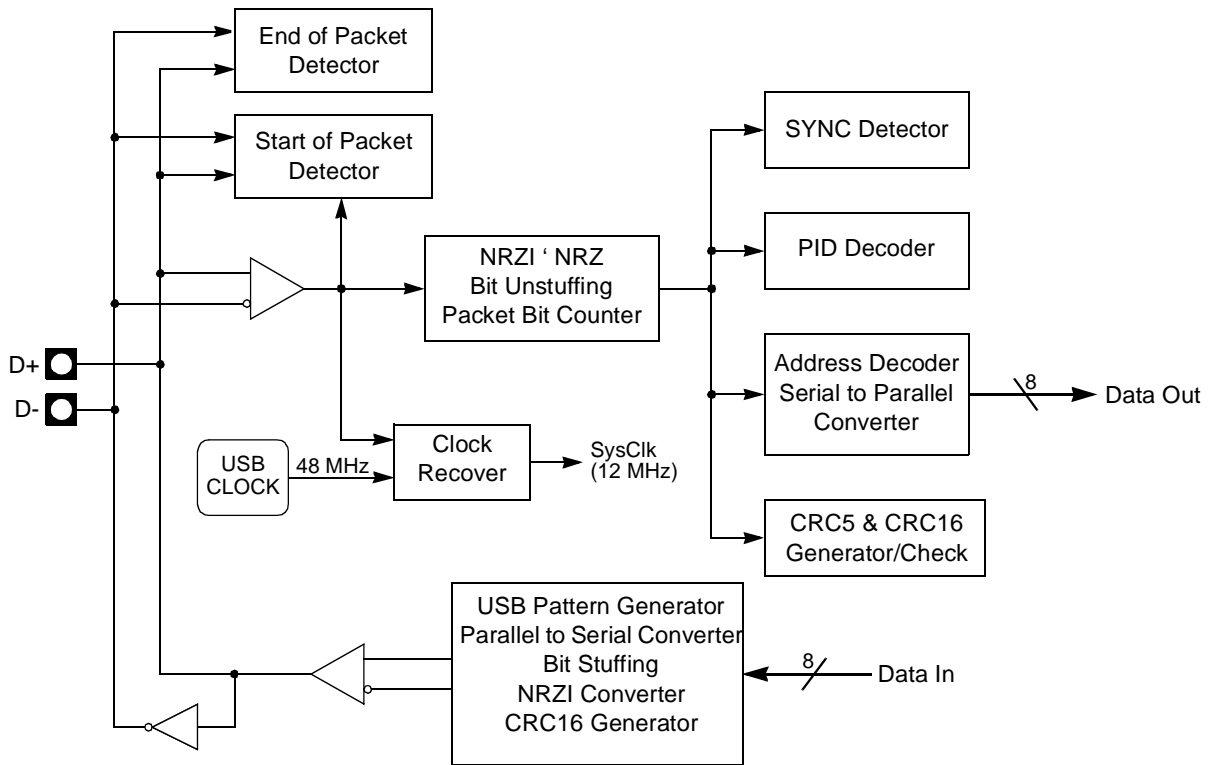


Serial Interface Engine (SIE)

The SIE performs the following functions:

- NRZI data encoding and decoding.
- Bit stuffing and unstuffing.
- CRC generation and checking.
- ACKs and NACKs automatic generation.
- TOKEN type identifying.
- Address checking.
- Clock recovery (using DPLL).

Figure 38. SIE Block Diagram



Function Interface Unit (UFI)

The Function Interface Unit provides the interface between the AT8xC51SND1A and the SIE. It manages transactions at the packet level with minimal intervention from the device firmware, which reads and writes the endpoint FIFOs.

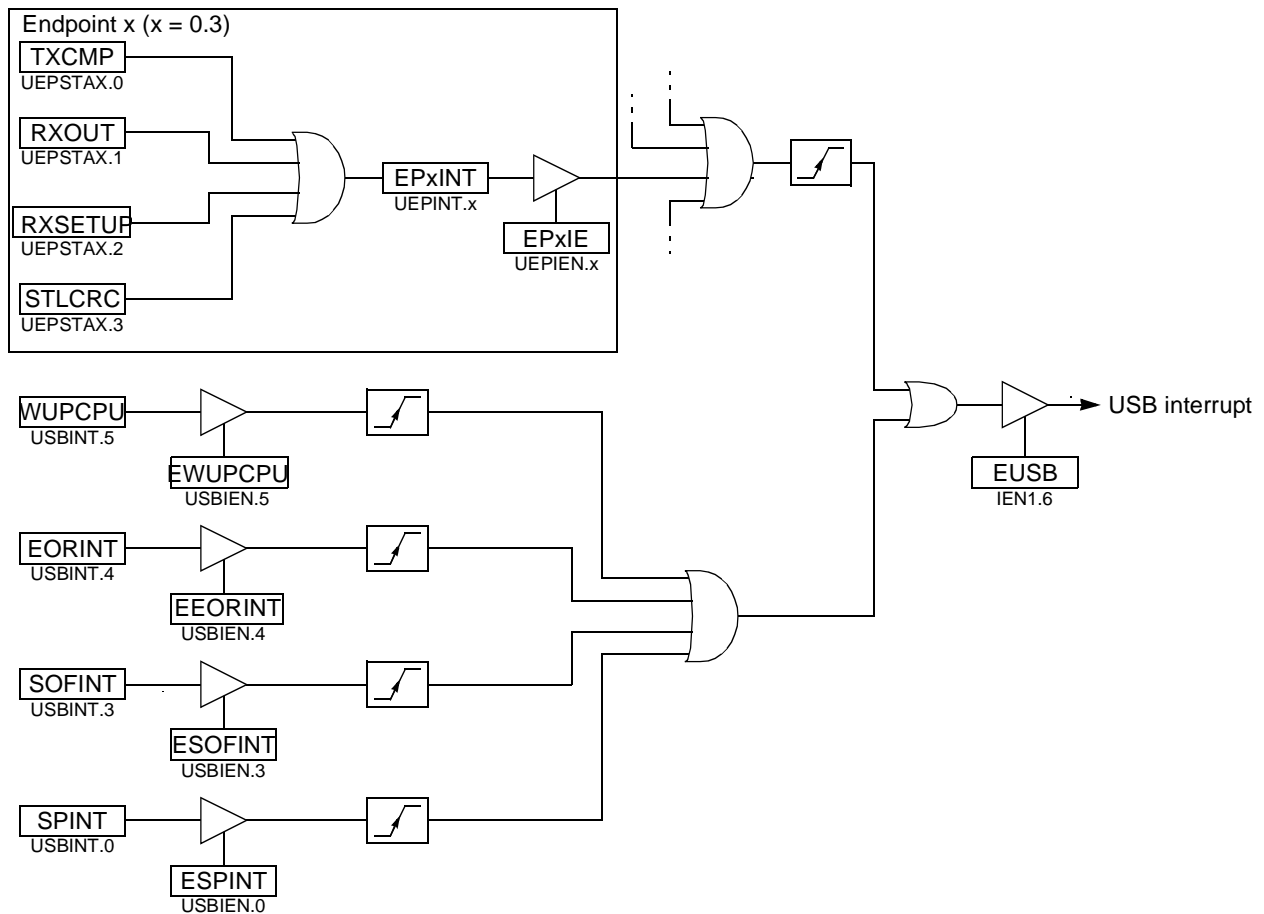
Figure 40 shows typical USB IN and OUT transactions reporting the split in the hardware (UFI) and software (C51) load.

Endpoint Interrupt Sources

Each endpoint supports four interrupt sources reported in UEPSTAX and combined together to appear as a single endpoint interrupt source in UEPINT. Each endpoint interrupt can be enabled separately in UEPIEN.

- **TXCMP:** Transmitted In Data Interrupt Flag.
This flag triggers an interrupt after an IN packet has been transmitted for Isochronous endpoints or after it has been accepted (ACK'ed) by the host for Control, Bulk and Interrupt endpoints.
- **RXOUT:** Received Out Data Interrupt Flag.
This flag triggers an interrupt after a new packet has been received.
- **RXSETUP:** Receive Setup Interrupt Flag.
This flag triggers an interrupt when a valid SETUP packet has been received from the host.
- **STLCRC:** Stall Sent Interrupt Flag/CRC Error Interrupt Flag.
This flag triggers an interrupt after a STALL handshake has been sent on the bus, for Control, Bulk and Interrupt endpoints.
This flag triggers an interrupt when the last data received is corrupted for Isochronous endpoints.

Figure 41. USB Interrupt Control Block Diagram



Registers

Table 73. USBCON Register

USBCON (S:BCh) – USB Global Control Register

7	6	5	4	3	2	1	0
USBE	SUSPCLK	SDRMWUP	-	UPRSM	RMWUPE	CONFIG	FADDEN
Bit Number	Bit Mnemonic	Description					
7	USBE	USB Enable Bit Set to enable the USB controller. Clear to disable and reset the USB controller.					
6	SUSPCLK	Suspend USB Clock Bit Set to disable the 48 MHz clock input (Resume Detection is still active). Clear to enable the 48 MHz clock input.					
5	SDRMWUP	Send Remote Wake-Up Bit Set to force an external interrupt on the USB controller for Remote Wake UP purpose. An upstream resume is send only if the bit RMWUPE is set, all USB clocks are enabled AND the USB bus was in SUSPEND state for at least 5 ms. See UPRSM below. Cleared by software.					
4	-	Reserved The value read from this bit is always 0. Do not set this bit.					
3	UPRSM	Upstream Resume Bit (read only) Set by hardware when SDRMWUP has been set and if RMWUPE is enabled. Cleared by hardware after the upstream resume has been sent.					
2	RMWUPE	Remote Wake-Up Enable Bit Set to enabled request an upstream resume signaling to the host. Clear after the upstream resume has been indicated by RSMINPR. Note: Do not set this bit if the host has not set the DEVICE_REMOTE_WAKEUP feature for the device.					
1	CONFIG	Configuration Bit Set after a SET_CONFIGURATION request with a non-zero value has been correctly processed. Clear by software when a SET_CONFIGURATION request with a zero value is received. Cleared by hardware on hardware reset or when an USB reset is detected on the bus.					
0	FADDEN	Function Address Enable Bit Set by the device firmware after a successful status phase of a SET_ADDRESS transaction. It shall not be cleared afterwards by the device firmware. Cleared by hardware on hardware reset or when an USB reset is received. When this bit is cleared, the default function address is used (0).					

Reset Value = 0000 0000b

Table 74. USBADDR Register

USBADDR (S:C6h) – USB Address Register

	7	6	5	4	3	2	1	0
	FEN	UADD6	UADD5	UADD4	UADD3	UADD2	UADD1	UADD0

Bit Number	Bit Mnemonic	Description
7	FEN	<p>Function Enable Bit Set to enable the function. The device firmware shall set this bit after it has received a USB reset and participate in the following configuration process with the default address (FEN is reset to 0). Cleared by hardware at power-up, should not be cleared by the device firmware once set.</p>
6-0	UADD6:0	<p>USB Address Bits This field contains the default address (0) after power-up or USB bus reset. It shall be written with the value set by a SET_ADDRESS request received by the device firmware.</p>

Reset Value = 0000 0000b

Table 75. USBINT Register

USBINT (S:BDh) – USB Global Interrupt Register

	7	6	5	4	3	2	1	0
	-	-	WUPCPU	EORINT	SOFINT	-	-	SPINT

Bit Number	Bit Mnemonic	Description
7-6	-	<p>Reserved The value read from these bits is always 0. Do not set these bits.</p>
5	WUPCPU	<p>Wake Up CPU Interrupt Flag Set by hardware when the USB controller is in SUSPEND state and is re-activated by a non-idle signal from USB line (not by an upstream resume). This triggers a USB interrupt when EWUPCPU is set in the USBIEN. Cleared by software after re-enabling all USB clocks.</p>
4	EORINT	<p>End of Reset Interrupt Flag Set by hardware when a End of Reset has been detected by the USB controller. This triggers a USB interrupt when EEORINT is set in USBIEN. Cleared by software.</p>
3	SOFINT	<p>Start of Frame Interrupt Flag Set by hardware when an USB Start of Frame packet (SOF) has been properly received. This triggers a USB interrupt when ESOFINT is set in USBIEN. Cleared by software.</p>
2-1	-	<p>Reserved The value read from these bits is always 0. Do not set these bits.</p>
0	SPINT	<p>Suspend Interrupt Flag Set by hardware when a USB Suspend (Idle bus for three frame periods: a J state for 3 ms) is detected. This triggers a USB interrupt when ESPINT is set in USBIEN. Cleared by software.</p>

Reset Value = 0000 0000b

Table 76. USBIEN Register

USBIEN (S:BEh) – USB Global Interrupt Enable Register

7	6	5	4	3	2	1	0
-	-	EWUPCPU	EORINT	ESOFINT	-	-	ESPINT
Bit Number	Bit Mnemonic	Description					
7-6	-	Reserved The value read from these bits is always 0. Do not set these bits.					
5	EWUPCPU	Wake Up CPU Interrupt Enable Bit Set to enable the Wake Up CPU interrupt. Clear to disable the Wake Up CPU interrupt.					
4	EEOFINT	End Of Reset Interrupt Enable Bit Set to enable the End Of Reset interrupt. This bit is set after reset. Clear to disable End Of Reset interrupt.					
3	ESOFINT	Start Of Frame Interrupt Enable Bit Set to enable the SOF interrupt. Clear to disable the SOF interrupt.					
2-1	-	Reserved The value read from these bits is always 0. Do not set these bits.					
0	ESPINT	Suspend Interrupt Enable Bit Set to enable Suspend interrupt. Clear to disable Suspend interrupt.					

Reset Value = 0001 0000b

Table 77. UEPNUM Register

UEPNUM (S:C7h) – USB Endpoint Number

7	6	5	4	3	2	1	0
-	-	-	-	-	-	EPNUM1	EPNUM0
Bit Number	Bit Mnemonic	Description					
7-2	-	Reserved The value read from these bits is always 0. Do not set these bits.					
1-0	EPNUM1: 0	Endpoint Number Bits Set this field with the number of the endpoint which shall be accessed when reading or writing to registers UEPSTAX, UEPDATX, UBYCTLX or UEPCONX.					

Reset Value = 0000 0000b

Table 78. UEPCONX Register

UEPCONX (S:D4h) – USB Endpoint X Control Register (X = EPNUM set in UEPNUM)

	7	6	5	4	3	2	1	0
	EPEN	-	-	-	DTGL	EPDIR	EPTYPE1	EPTYPE0

Bit Number	Bit Mnemonic	Description
7	EPEN	<p>Endpoint Enable Bit Set to enable the endpoint according to the device configuration. Endpoint 0 shall always be enabled after a hardware or USB bus reset and participate in the device configuration. Clear to disable the endpoint according to the device configuration.</p>
6-4	-	<p>Reserved The value read from this bit is always 0. Do not set this bit.</p>
3	DTGL	<p>Data Toggle Status Bit (Read-only) Set by hardware when a DATA1 packet is received. Cleared by hardware when a DATA0 packet is received. Note: When a new data packet is received without DTGL toggling from 1 to 0 or 0 to 1, a packet may have been lost. When this occurs for a Bulk endpoint, the device firmware shall consider the host has retried transmitting a properly received packet because the host has not received a valid ACK, then the firmware shall discard the new packet (N.B. The endpoint resets to DATA0 only upon configuration). For interrupt endpoints, data toggling is managed as for Bulk endpoints when used. For Control endpoints, each SETUP transaction starts with a DATA0 and data toggling is then used as for Bulk endpoints until the end of the Data stage (for a control write transfer); the Status stage completes the data transfer with a DATA1 (for a control read transfer). For Isochronous endpoints, the device firmware shall retrieve every new data packet and may ignore this bit.</p>
2	EPDIR	<p>Endpoint Direction Bit Set to configure IN direction for Bulk, Interrupt and Isochronous endpoints. Clear to configure OUT direction for Bulk, Interrupt and Isochronous endpoints. This bit has no effect for Control endpoints.</p>
1-0	EPTYPE1: 0	<p>Endpoint Type Bits Set this field according to the endpoint configuration (Endpoint 0 shall always be configured as Control): 00Control endpoint 01Isochronous endpoint 10Bulk endpoint 11Interrupt endpoint</p>

Reset Value = 0000 0000b

Table 79. UEPSTAX Register

UEPSTAX (Soh) – USB Endpoint X Status and Control Register (X = EPNUM set in UEPNUM)

7	6	5	4	3	2	1	0
DIR	-	STALLRQ	TXRDY	STLCRC	RXSETUP	RXOUT	TXCMP
Bit Number	Bit Mnemonic	Description					
7	DIR	<p>Control Endpoint Direction Bit This bit is relevant only if the endpoint is configured in Control type. Set for the data stage. Clear otherwise. Note: This bit shall be configured on RXSETUP interrupt before any other bit is changed. This also determines the status phase (IN for a control write and OUT for a control read). This bit shall be cleared for status stage of a Control Out transaction.</p>					
6	-	<p>Reserved The value read from this bits is always 0. Do not set this bit.</p>					
5	STALLRQ	<p>Stall Handshake Request Bit Set to send a STALL answer to the host for the next handshake. Clear otherwise.</p>					
4	TXRDY	<p>TX Packet Ready Control Bit Set after a packet has been written into the endpoint FIFO for IN data transfers. Data shall be written into the endpoint FIFO only after this bit has been cleared. Set this bit without writing data to the endpoint FIFO to send a Zero Length Packet, which is generally recommended and may be required to terminate a transfer when the length of the last data packet is equal to MaxPacketSize (e.g. for control read transfers). Cleared by hardware, as soon as the packet has been sent for Isochronous endpoints, or after the host has acknowledged the packet for Control, Bulk and Interrupt endpoints.</p>					
3	STLCRC	<p>Stall Sent Interrupt Flag/CRC Error Interrupt Flag For Control, Bulk and Interrupt Endpoints: Set by hardware after a STALL handshake has been sent as requested by STALLRQ. Then, the endpoint interrupt is triggered if enabled in UEPIEN. Cleared by hardware when a SETUP packet is received (see RXSETUP). For Isochronous Endpoints: Set by hardware if the last data received is corrupted (CRC error on data). Then, the endpoint interrupt is triggered if enabled in UEPIEN. Cleared by hardware when a non corrupted data is received.</p>					
2	RXSETUP	<p>Received SETUP Interrupt Flag Set by hardware when a valid SETUP packet has been received from the host. Then, all the other bits of the register are cleared by hardware and the endpoint interrupt is triggered if enabled in UEPIEN. Clear by software after reading the SETUP data from the endpoint FIFO.</p>					
1	RXOUT	<p>Received OUT Data Interrupt Flag Set by hardware after an OUT packet has been received. Then, the endpoint interrupt is triggered if enabled in UEPIEN and all the following OUT packets to the endpoint are rejected (NACK'ed) until this bit is cleared. However, for Control endpoints, an early SETUP transaction may overwrite the content of the endpoint FIFO, even if its Data packet is received while this bit is set. Clear by software after reading the OUT data from the endpoint FIFO.</p>					
0	TXCMP	<p>Transmitted IN Data Complete Interrupt Flag Set by hardware after an IN packet has been transmitted for Isochronous endpoints and after it has been accepted (ACK'ed) by the host for Control, Bulk and Interrupt endpoints. Then, the endpoint interrupt is triggered if enabled in UEPIEN. Clear by software before setting again TXRDY.</p>					

Reset Value = 0000 0000b



Table 80. UEPRST Register

UEPRST (S:D5h) – USB Endpoint FIFO Reset Register

	7	6	5	4	3	2	1	0
	-	-	-	-	EP3RST	EP2RST	EP1RST	EP0RST

Bit Number	Bit Mnemonic	Description
7-4	-	Reserved The value read from these bits is always 0. Do not set these bits.
3	EP3RST	Endpoint 3 FIFO Reset Set and clear to reset the endpoint 3 FIFO prior to any other operation, upon hardware reset or when an USB bus reset has been received.
2	EP2RST	Endpoint 2 FIFO Reset Set and clear to reset the endpoint 2 FIFO prior to any other operation, upon hardware reset or when an USB bus reset has been received.
1	EP1RST	Endpoint 1 FIFO Reset Set and clear to reset the endpoint 1 FIFO prior to any other operation, upon hardware reset or when an USB bus reset has been received.
0	EP0RST	Endpoint 0 FIFO Reset Set and clear to reset the endpoint 0 FIFO prior to any other operation, upon hardware reset or when an USB bus reset has been received.

Reset Value = 0000 0000b

Table 81. UEPINT Register

UEPINT (S:F8h Read-only) – USB Endpoint Interrupt Register

	7	6	5	4	3	2	1	0
	-	-	-	-	EP3INT	EP2INT	EP1INT	EP0INT

Bit Number	Bit Mnemonic	Description
7-4	-	Reserved The value read from these bits is always 0. Do not set these bits.
3	EP3INT	Endpoint 3 Interrupt Flag Set by hardware when an interrupt is triggered in UEPSTAX and the endpoint 3 interrupt is enabled in UEPIEN. Must be cleared by software.
2	EP2INT	Endpoint 2 Interrupt Flag Set by hardware when an interrupt is triggered in UEPSTAX and the endpoint 2 interrupt is enabled in UEPIEN. Must be cleared by software.
1	EP1INT	Endpoint 1 Interrupt Flag Set by hardware when an interrupt is triggered in UEPSTAX and the endpoint 1 interrupt is enabled in UEPIEN. Must be cleared by software.
0	EP0INT	Endpoint 0 Interrupt Flag Set by hardware when an interrupt is triggered in UEPSTAX and the endpoint 0 interrupt is enabled in UEPIEN. Must be cleared by software.

Reset Value = 0000 0000b

Table 82. UEPIEN Register

UEPIEN (S:C2h) – USB Endpoint Interrupt Enable Register

7	6	5	4	3	2	1	0
-	-	-	-	EP3INTE	EP2INTE	EP1INTE	EPOINTE

Bit Number	Bit Mnemonic	Description
7-4	-	Reserved The value read from these bits is always 0. Do not set these bits.
3	EP3INTE	Endpoint 3 Interrupt Enable Bit Set to enable the interrupts for endpoint 3. Clear to disable the interrupts for endpoint 3.
2	EP2INTE	Endpoint 2 Interrupt Enable Bit Set to enable the interrupts for endpoint 2. Clear this bit to disable the interrupts for endpoint 2.
1	EP1INTE	Endpoint 1 Interrupt Enable Bit Set to enable the interrupts for the endpoint 1. Clear to disable the interrupts for the endpoint 1.
0	EPOINTE	Endpoint 0 Interrupt Enable Bit Set to enable the interrupts for the endpoint 0. Clear to disable the interrupts for the endpoint 0.

Reset Value = 0000 0000b

Table 83. UEPDATX Register

UEPDATX (S:CFh) – USB Endpoint X FIFO Data Register (X = EPNUM set in UEPNUM)

7	6	5	4	3	2	1	0
FDAT7	FDAT6	FDAT5	FDAT4	FDAT3	FDAT2	FDAT1	FDAT0

Bit Number	Bit Mnemonic	Description
7 - 0	FDAT7:0	Endpoint X Fifo Data Data byte to be written to Fifo or data byte to be read from the Fifo, for the Endpoint X (see EPNUM).

Reset Value = XXh



Table 84. UBYCTLX Register
 UBYCTX (S:E2h) – USB Endpoint X Byte Count Register (X = EPNUM set in UEPNUM)

	7	6	5	4	3	2	1	0
	-	BYCT6	BYCT5	BYCT4	BYCT3	BYCT2	BYCT1	BYCT0

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bits is always 0. Do not set this bit.
6-0	BYCT7:0	Byte Count Byte count of a received data packet. This byte count is equal to the number of data bytes received after the Data PID.

Reset Value = 0000 0000b

Table 85. UFNUML Register
 UFNUML (S:BAh, Read-only) – USB Frame Number Low Register

	7	6	5	4	3	2	1	0
	FNUM7	FNUM6	FNUM5	FNUM4	FNUM3	FNUM2	FNUM1	FNUM0

Bit Number	Bit Mnemonic	Description
7 - 0	FNUM7:0	Frame Number Lower 8 bits of the 11-bit Frame Number.

Reset Value = 00h

Table 86. UFNUMH Register

UFNUMH (S:BBh, Read-only) – USB Frame Number High Register

7	6	5	4	3	2	1	0
-	-	CRCOK	CRCERR	-	FNUM10	FNUM9	FNUM8
Bit Number	Bit Mnemonic	Description					
7-3	-	Reserved The value read from these bits is always 0. Do not set these bits.					
5	CRCOK	Frame Number CRC OK Bit Set by hardware after a non corrupted Frame Number in Start of Frame Packet is received. Updated after every Start Of Frame packet reception. Note: The Start Of Frame interrupt is generated just after the PID receipt.					
4	CRCERR	Frame Number CRC Error Bit Set by hardware after a corrupted Frame Number in Start of Frame Packet is received. Updated after every Start Of Frame packet reception. Note: The Start Of Frame interrupt is generated just after the PID receipt.					
3	-	Reserved The value read from this bits is always 0. Do not set this bit.					
2-0	FNUM10:8	Frame Number Upper 3 bits of the 11-bit Frame Number. It is provided in the last received SOF packet. FNUM does not change if a corrupted SOF is received.					

Reset Value = 00h

Table 87. USBCLK Register

USBCLK (S:EAh) – USB Clock Divider Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	USBCD1	USBCD0
Bit Number	Bit Mnemonic	Description					
7-2	-	Reserved The value read from these bits is always 0. Do not set these bits.					
1-0	USBCD1:0	USB Controller Clock Divider 2-bit divider for USB controller clock generation.					

Reset Value = 0000 0000b

MultiMediaCard Controller

The AT8xC51SND1A implements a MultiMediaCard (MMC) controller. The MMC is used to store MP3 encoded audio files in removable flash memory cards that can be easily plugged or removed from the application.

Card Concept

The basic MultiMediaCard concept is based on transferring data via a minimal number of signals.

Card Signals

The communication signals are:

- CLK: with each cycle of this signal an one bit transfer on the command and data lines is done. The frequency may vary from zero to the maximum clock frequency.
- CMD: is a bidirectional command channel used for card initialization and data transfer commands. The CMD signal has two operation modes: open-drain for initialization mode and push-pull for fast command transfer. Commands are sent from the MultiMediaCard bus master to the card and responses from the cards to the host.
- DAT: is a bidirectional data channel. The DAT signal operates in push-pull mode. Only one card or the host is driving this signal at a time.

Card Registers

Within the card interface five registers are defined: OCR, CID, CSD, RCA and DSR. These can be accessed only by corresponding commands.

The 32-bit Operation Conditions Register (OCR) stores the V_{DD} voltage profile of the card. The register is optional and can be read only.

The 128-bit wide CID register carries the card identification information (Card ID) used during the card identification procedure.

The 128-bit wide Card-Specific Data register (CSD) provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, and whether the DSR register can be used. The 16-bit Relative Card Address register (RCA) carries the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the card identification procedure.

The 16-bit Driver Stage Register (DSR) can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of cards).

Bus Concept

The MultiMediaCard bus is designed to connect either solid-state mass-storage memory or I/O-devices in a card format to multimedia applications. The bus implementation allows the coverage of application fields from low-cost systems to systems with a fast data transfer rate. It is a single master bus with a variable number of slaves. The MultiMediaCard bus master is the bus controller and each slave is either a single mass storage card (with possibly different technologies such as ROM, OTP, Flash etc.) or an I/O-card with its own controlling unit (on card) to perform the data transfer.

The MultiMediaCard bus also includes power connections to supply the cards.

The bus communication uses a special protocol (MultiMediaCard bus protocol) which is applicable for all devices. Therefore, the payload data transfer between the host and the cards can be bidirectional.

Bus Lines

The MultiMediaCard bus architecture requires all cards to be connected to the same set of lines. No card has an individual connection to the host or other devices, which reduces the connection costs of the MultiMediaCard system.

The bus lines can be divided into three groups:

- Power supply: V_{SS1} and V_{SS2} , V_{DD} – used to supply the cards.
- Data transfer: MCMD, MDAT – used for bidirectional communication.
- Clock: MCLK – used to synchronize data transfer across the bus.

Bus Protocol

After a power-on reset, the host must initialize the cards by a special message-based MultiMediaCard bus protocol. Each message is represented by one of the following tokens:

- Command: a command is a token which starts an operation. A command is transferred serially from the host to the card on the MCMD line.
- Response: a response is a token which is sent from an addressed card (or all connected cards) to the host as an answer to a previously received command. It is transferred serially on the MCMD line.
- Data: data can be transferred from the card to the host or vice-versa. Data is transferred serially on the MDAT line.

Card addressing is implemented using a session address assigned during the initialization phase, by the bus controller to all currently connected cards. Individual cards are identified by their CID number. This method requires that every card will have an unique CID number. To ensure uniqueness of CIDs the CID register contains 24 bits (MID and OID fields) which are defined by the MMCA. Every card manufacturers is required to apply for an unique MID (and optionally OID) number.

MultiMediaCard bus data transfers are composed of these tokens. One data transfer is a bus operation. There are different types of operations. Addressed operations always contain a command and a response token. In addition, some operations have a data token, the others transfer their information directly within the command or response structure. In this case no data token is present in an operation. The bits on the MDAT and the MCMD lines are transferred synchronous to the host clock.

Two types of data transfer commands are defined:

- Sequential commands: These commands initiate a continuous data stream, they are terminated only when a stop command follows on the MCMD line. This mode reduces the command overhead to an absolute minimum.
- Block-oriented commands: These commands send a data block succeeded by CRC bits. Both read and write operations allow either single or multiple block transmission. A multiple block transmission is terminated when a stop command follows on the MCMD line similarly to the stream read.

Figure 17 to Figure 45 show the different types of operations, on these figures, grayed tokens are from host to card(s) while white tokens are from card(s) to host.

Figure 17. Sequential Read Operation

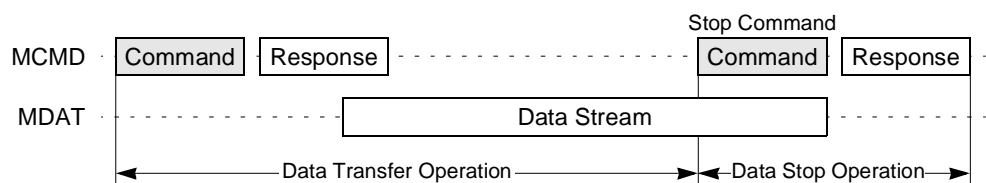
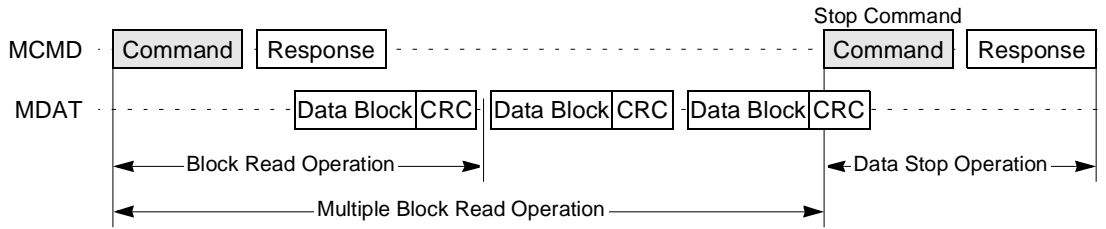


Figure 42. (Multiple) Block Read Operation



As shown in Figure 43 and Figure 44 the data write operation uses a simple busy signaling of the write operation duration on the data line (MDAT).

Figure 43. Sequential Write Operation

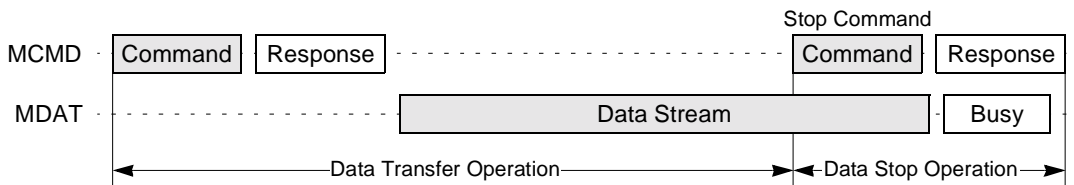


Figure 44. (Multiple) Block Write Operation

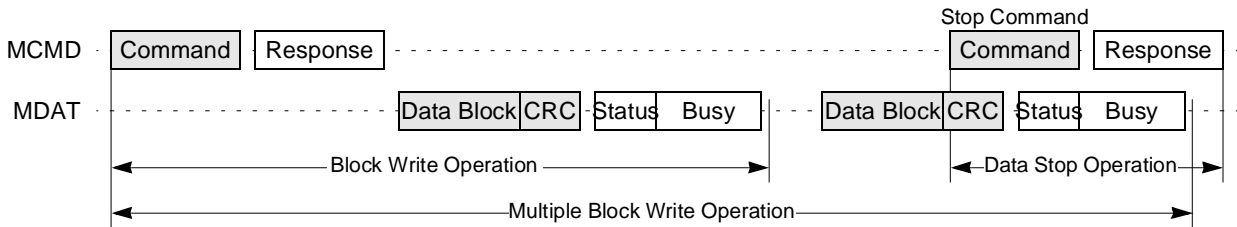
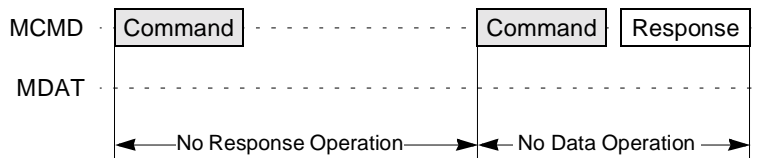


Figure 45. No Response and No Data Operation



Command Token Format

As shown in Figure 46, commands have a fixed code length of 48 bits. Each command token is preceded by a Start bit: a low level on MCMD line and succeeded by an End bit: a high level on MCMD line. The command content is preceded by a Transmission bit: a high level on MCMD line for a command token (host to card) and succeeded by a 7-bit CRC so that transmission errors can be detected and the operation may be repeated. Command content contains the command index and address information or parameters.

Figure 46. Command Token Format

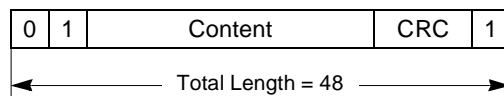


Table 88. Command Token Format

Bit Position	47	46	45:40	39:8	7:1	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'1'	-	-	-	'1'
Description	Start bit	Transmission bit	Command Index	Argument	CRC7	End bit

Response Token Format

There are five types of response tokens (R1 to R5). As shown in Figure 18, responses have a code length of 48 bits or 136 bits. A response token is preceded by a Start bit: a low level on MCMD line and succeeded by an End bit: a high level on MCMD line. The command content is preceded by a Transmission bit: a low level on MCMD line for a response token (card to host) and succeeded (R1,R2,R4,R5) or not (R3) by a 7-bit CRC.

Response content contains mirrored command and status information (R1 response), CID register or CSD register (R2 response), OCR register (R3 response), or RCA register (R4 and R5 response).

Figure 18. Response Token Format

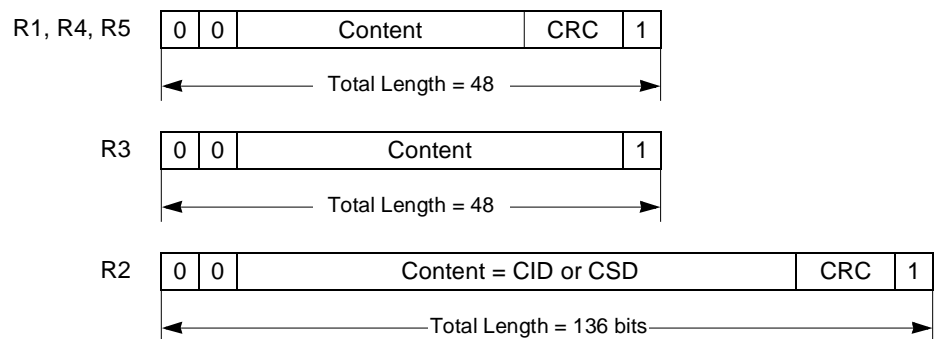


Table 89. R1 Response Format (Normal Response)

Bit Position	47	46	45:40	39:8	7:1	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	-	-	-	'1'
Description	Start bit	Transmission bit	Command Index	Card Status	CRC7	End bit

Table 90. R2 Response Format (CID and CSD registers)

Bit Position	135	134	[133:128]	[127:1]	0
Width (bits)	1	1	6	32	1
Value	'0'	'0'	'111111'	-	'1'
Description	Start bit	Transmission bit	Reserved	Argument	End bit

Table 91. R3 Response Format (OCR Register)

Bit Position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'111111'	-	'1111111'	'1'
Description	Start bit	Transmission bit	Reserved	OCR register	Reserved	End bit

Table 92. R4 Response Format (Fast I/O)

Bit Position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'100111'	-	-	'1'
Description	Start bit	Transmission bit	Command Index	Argument	CRC7	End bit

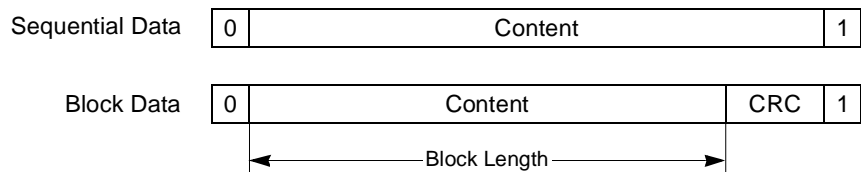
Table 93. R5 Response Format

Bit Position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'101000'	-	-	'1'
Description	Start bit	Transmission bit	Command Index	Argument	CRC7	End bit

Data Packet Format

There are two types of data packets: stream and block. As shown in Figure 19, stream data packets have an indeterminate length while block packets have a fixed length depending on the block length. Each data packet is preceded by a Start bit: a low level on MCMD line and succeeded by an End bit: a high level on MCMD line. Due to the fact that there is no predefined end in stream packets, CRC protection is not included in this case. The CRC protection algorithm for block data is a 16-bit CCITT polynomial.

Figure 19. Data Token Format



Clock Control

The MMC bus clock signal can be used by the host to turn the cards into energy saving mode or to control the data flow (to avoid under-run or over-run conditions) on the bus. The host is allowed to lower the clock frequency or shut it down.

There are a few restrictions the host must follow:

- The bus frequency can be changed at any time (under the restrictions of maximum data transfer frequency, defined by the cards, and the identification frequency defined by the specification document).
- It is an obvious requirement that the clock must be running for the card to output data or response tokens. After the last MultiMediaCard bus transaction, the host is

required, to provide 8 (eight) clock cycles for the card to complete the operation before shutting down the clock. Following is a list of the various bus transactions:

- A command with no response. 8 clocks after the host command End bit.
- A command with response. 8 clocks after the card command End bit.
- A read data transaction. 8 clocks after the End bit of the last data block.
- A write data transaction. 8 clocks after the CRC status token.
- The host is allowed to shut down the clock of a “busy” card. The card will complete the programming operation regardless of the host clock. However, the host must provide a clock edge for the card to turn off its busy signal. Without a clock edge the card (unless previously disconnected by a deselect command-CMD7) will force the MDAT line down, forever.

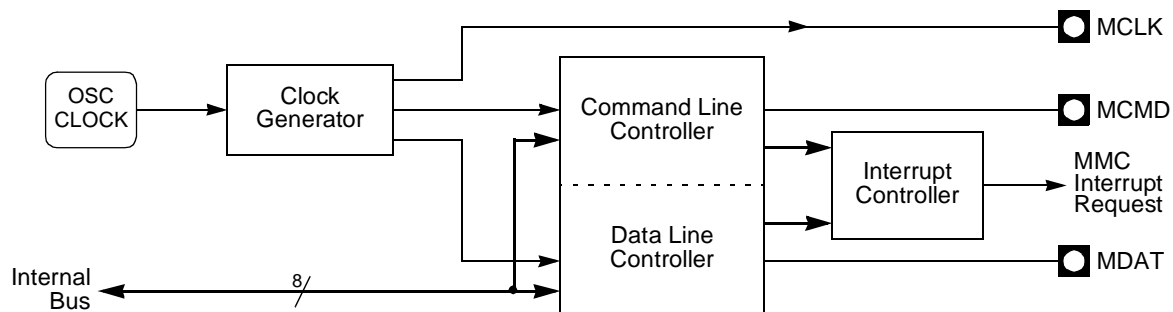
Description

The MMC controller interfaces to the C51 core through the following eight special function registers:

MMCON0, MMCON1, MMCON2, the three MMC control registers (see Figure 95 to Figure); MMSTA, the MMC status register (see Figure 98); MMINT, the MMC interrupt register (see Figure); MMMSK, the MMC interrupt mask register (see Figure 100); MMCMD, the MMC command register (see Figure 101); MMDAT, the MMC data register (see Figure); and MMCLK, the MMC clock register (see Figure 103).

As shown in Figure 47, the MMC controller is divided in four blocks: the clock generator that handles the MCLK (formally the MMC CLK) output to the card, the command line controller that handles the MCMD (formally the MMC CMD) line traffic to or from the card, the data line controller that handles the MDAT (formally the MMC DAT) line traffic to or from the card, and the interrupt controller that handles the MMC controller interrupt sources. These blocks are detailed in the following sections.

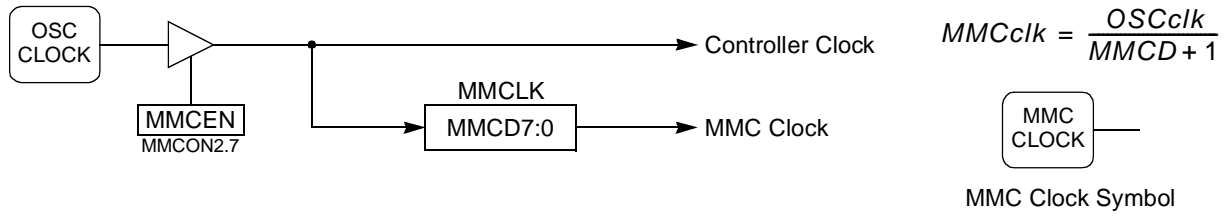
Figure 47. MMC Controller Block Diagram



Clock Generator

The MMC clock is generated by division of the oscillator clock (F_{OSC}) issued from the Clock Controller block as detailed in Section "Oscillator", page 4. The division factor is given by MMCD7:0 bits in MMCLK register. Figure 48 shows the MMC clock generator and its output clock calculation formula.

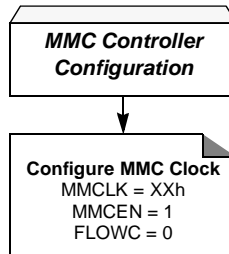
Figure 48. MMC Clock Generator and Symbol



As soon as MMCEN bit in MMCON2 is set, the MMC controller receives its system clock. The MMC command and data clock is generated on MCLK output and sent to the command line and data line controllers. Figure 49 shows the MMC controller configuration flow.

As exposed in Section , MMCD7:0 bits can be used to dynamically increase or reduce the MMC clock.

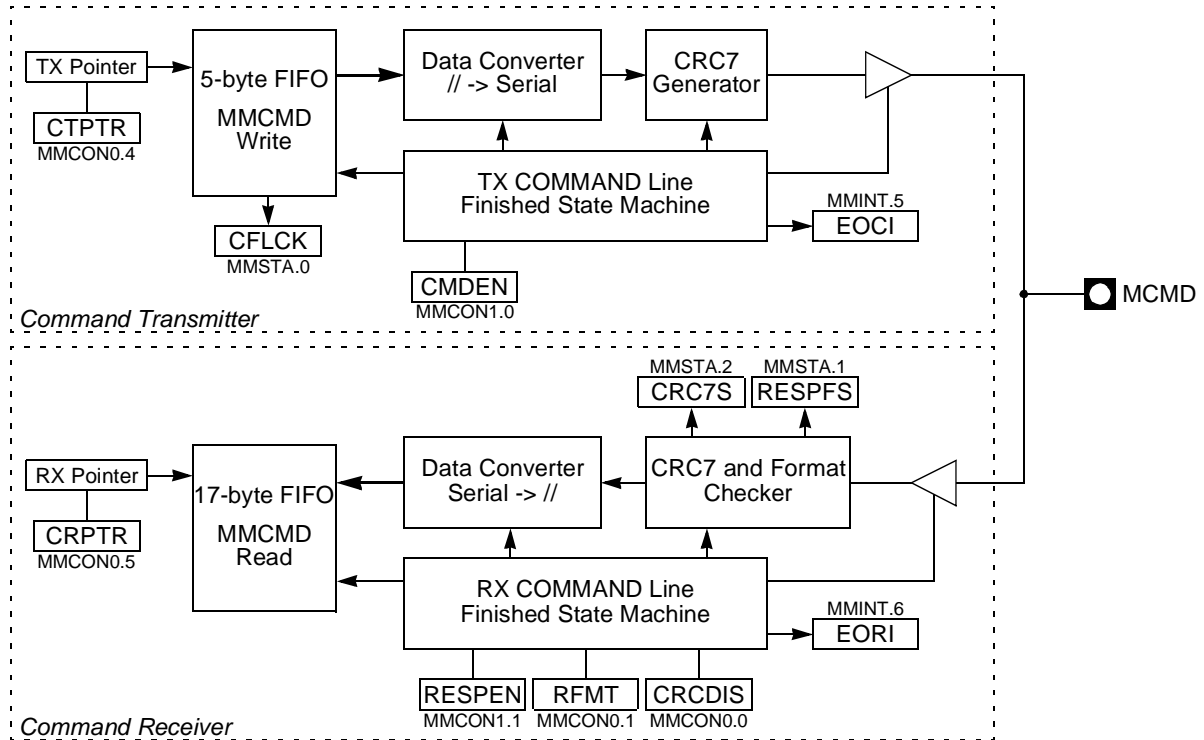
Figure 49. Configuration Flow



Command Line Controller

As shown in Figure 50, the command line controller is divided in two channels: the command transmitter channel that handles the command transmission to the card through the MCMD line and the command receiver channel that handles the response reception from the card through the MCMD line. These channels are detailed in the following sections.

Figure 50. Command Line Controller Block Diagram



Command Transmitter

For sending a command to the card, user must load the command index (1 byte) and argument (4 bytes) in the command transmit FIFO using the MMCMD register. Before starting transmission by setting and clearing the CMDEN bit in MMCON1 register, user must first configure:

- RESPEN bit in MMCON1 register to indicate whether a response is expected or not.
- RFMT bit in MMCON0 register to indicate the response size expected.
- CRCDIS bit in MMCON0 register to indicate whether the CRC7 included in the response will be computed or not. In order to avoid CRC error, CRCDIS may be set for response that do not include CRC7.

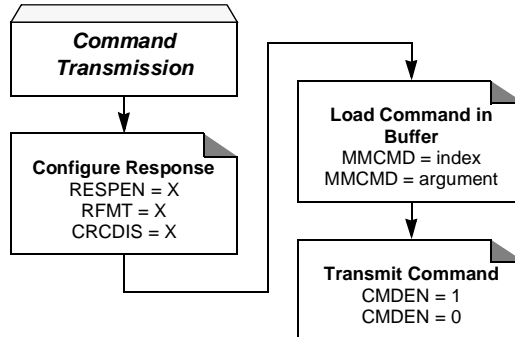
Figure 20 summarizes the command transmission flow.

As soon as command transmission is enabled, the CFLCK flag in MMSTA is set indicating that write to the FIFO is locked. This mechanism is implemented to avoid command overrun.

The end of the command transmission is signalled to you by the EOCI flag in MMINT register becoming set. This flag may generate an MMC interrupt request as detailed in Section "Interrupt", page 103. The end of the command transmission also resets the CFLCK flag.

User may abort command loading by setting and clearing the CTPTR bit in MMCON0 register which resets the write pointer to the transmit FIFO.

Figure 20. Command Transmission Flow



Command Receiver

The end of the response reception is signalled to you by the EORI flag in MMINT register. This flag may generate an MMC interrupt request as detailed in Section "Interrupt", page 103. When this flag is set, two other flags in MMSTA register: RESPFS and CRC7S give a status on the response received. RESPFS indicates if the response format is correct or not: the size is the one expected (48 bits or 136 bits) and a valid End bit has been received, and CRC7S indicates if the CRC7 computation is correct or not. These Flags are cleared when a command is sent to the card and updated when the response has been received.

User may abort response reading by setting and clearing the CRPTR bit in MMCON0 register which resets the read pointer to the receive FIFO.

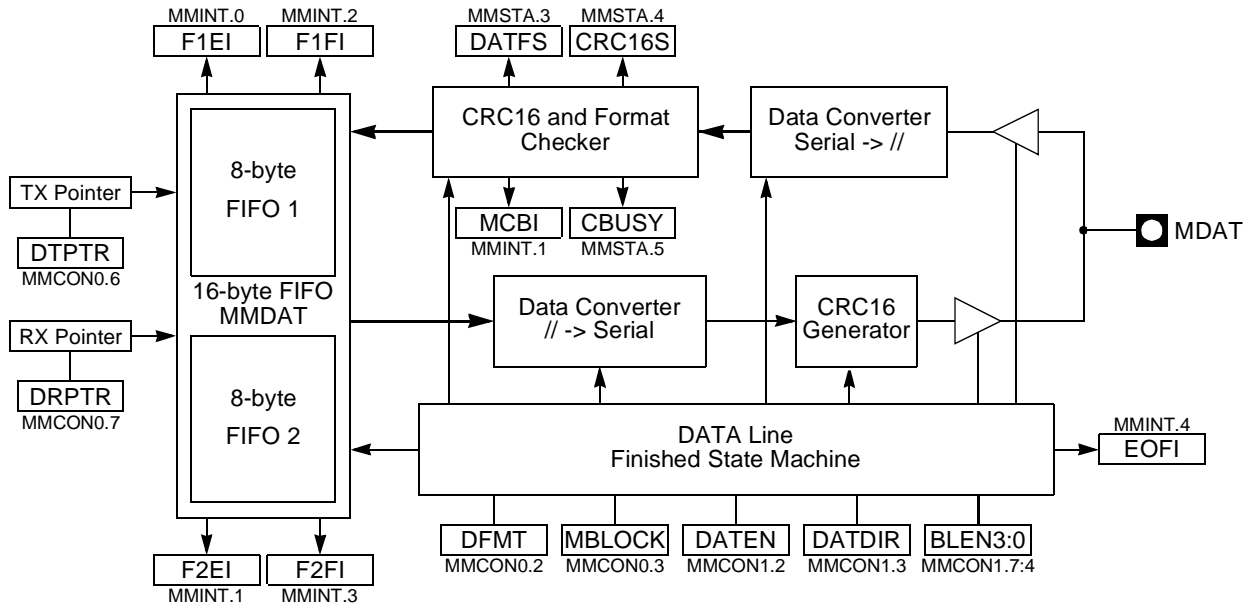
According to the MMC specification delay between a command and a response (formally N_{CR} parameter) can not exceed 64 MMC clock periods. To avoid any locking of the MMC controller when card does not send its response (e.g. physically removed from the bus), user must launch a time-out period to exit from such situation. In case of time-out user may reset the command controller and its internal state machine by setting and clearing the CCR bit in MMCON2 register.

This time-out may be disarmed when receiving the response.

Data Line Controller

The data line controller is based on a 16-byte FIFO used both by the data transmitter channel and by the data receiver channel.

Figure 51. Data Line Controller Block Diagram



FIFO Implementation

The 16-byte FIFO is based on a dual 8-byte FIFOs managed using two pointers and four flags indicating the status full and empty of each FIFO.

Pointers are not accessible to user but can be reset at any time by setting and clearing DRPTR and DTPTR bits in MMCON0 register. Resetting the pointers is equivalent to abort the writing or reading of data.

F1EI and F2EI flags in MMINT register signal when set that respectively FIFO1 and FIFO2 are empty. F1FI and F2FI flags in MMINT register signal when set that respectively FIFO1 and FIFO2 are full. These flags may generate an MMC interrupt request as detailed in Section .

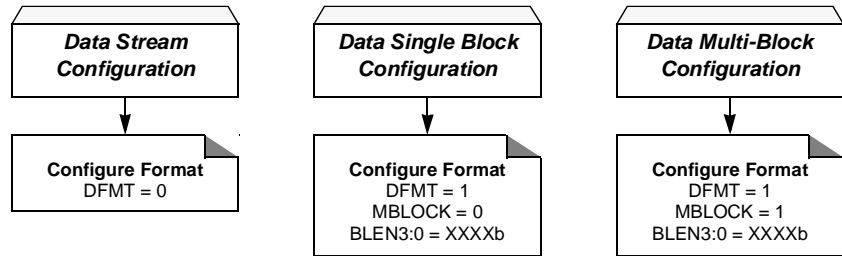
Data Configuration

Before sending or receiving any data, the data line controller must be configured according to the type of the data transfer considered. This is achieved using the Data Format bit: DFMT in MMCON0 register. Clearing DFMT bit enables the data stream format while setting DFMT bit enables the data block format. In data block format, user must also configure the single or multi-block mode by clearing or setting the MBLOCK bit in MMCON0 register and the block length using BLEN3:0 bits in MMCON1 according to Table 94. Figure 21 summarizes the data modes configuration flows.

Table 94. Block Length Programming

BLEN3:0	Block Length (Byte)
BLEN = 0000 to 1011	Length = 2^{BLEN} : 1 to 2048
> 1011	Reserved: do not program BLEN3:0 > 1011

Figure 21. Data Controller Configuration Flows



Data Transmitter

Configuration

For transmitting data to the card user must first configure the data controller in transmission mode by setting the DATDIR bit in MMCON1 register.

Figure 52 summarizes the data stream transmission flows in both polling and interrupt modes while Figure 53 summarizes the data block transmission flows in both polling and interrupt modes, these flows assume that block length is greater than 16 data.

Data Loading

Data is loaded in the FIFO by writing to MMDAT register. Number of data loaded may vary from 1 to 16 bytes. Then if necessary (more than 16 bytes to send) user must wait that one FIFO becomes empty (F1EI or F2EI set) before loading 8 new data.

Data Transmission

Transmission is enabled by setting and clearing DATEN bit in MMCON1 register. Data is transmitted immediately if the response has already been received, or is delayed after the response reception if its status is correct. In both cases transmission is delayed if a card sends a busy state on the data line until the end of this busy condition.

According to the MMC specification, the data transfer from the host to the card may not start sooner than 2 MMC clock periods after the card response was received (formally N_{WR} parameter). To address all card types, this delay can be programmed using DATD1:0 bits in MMCON2 register from 2 MMC clock periods when DATD1:0 bits are cleared to 8 MMC clock periods when DATD2:0 bits are set, by step of 2 MMC clock periods.

End of Transmission

The end of a data frame (block or stream) transmission is signalled to you by the EOFI flag in MMINT register. This flag may generate an MMC interrupt request as detailed in Section "Interrupt", page 103.

In data stream mode, EOFI flag is set, after reception of the End bit. This assumes user has previously sent the STOP command to the card, which is the only way to stop stream transfer.

In data block mode, EOFI flag is set, after reception of the CRC status token (see Figure 44). Two other flags in MMSTA register: DATFS and CRC16S report a status on the frame sent. DATFS indicates if the CRC status token format is correct or not, and CRC16S indicates if the card has found the CRC16 of the block correct or not.

Busy Status

As shown in Figure 44 the card uses a busy token during a block write operation. This busy status is reported to you by the CBUSY flag in MMSTA register and by the MCBI flag in MMINT which is set every time CBUSY toggles, i.e. when the card enters and exits its busy state. This flag may generate an MMC interrupt request as detailed in Section "Interrupt", page 103.

Figure 52. Data Stream Transmission Flows

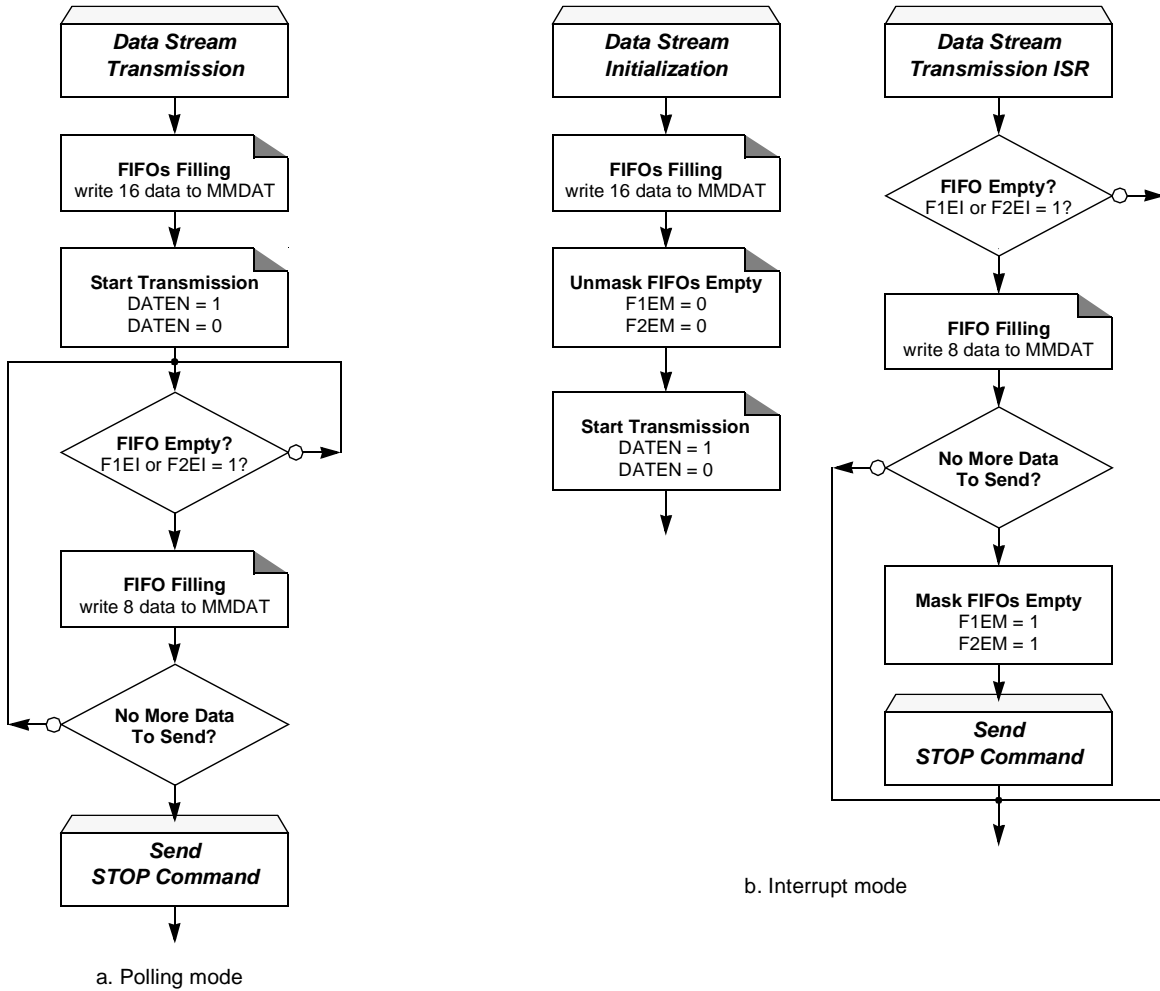
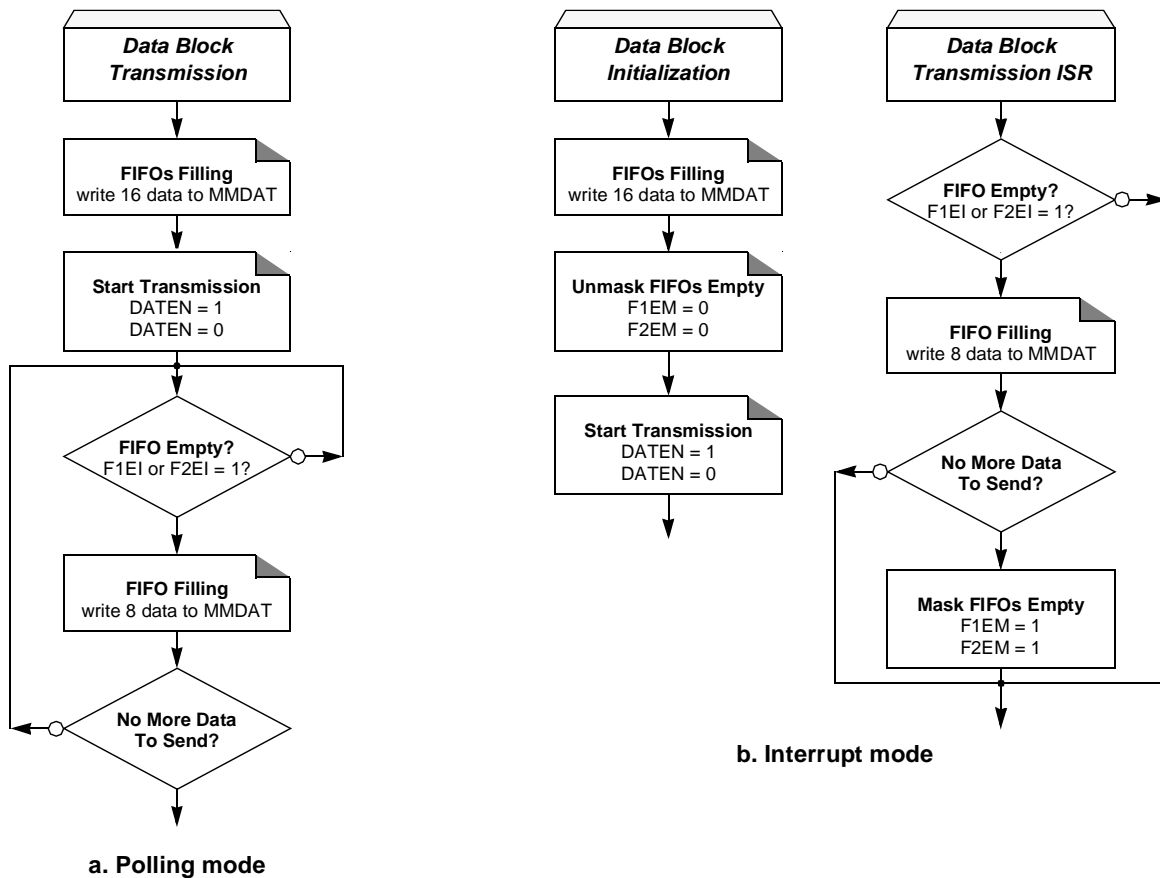


Figure 53. Data Block Transmission Flows



Data Receiver

Configuration

To receive data from the card you must first configure the data controller in reception mode by clearing the DATDIR bit in MMCON1 register.

Figure 54 summarizes the data stream reception flows in both polling and interrupt modes while Figure 55 summarizes the data block reception flows in both polling and interrupt modes, these flows assume that block length is greater than 16 bytes.

Data Reception

The end of a data frame (block or stream) reception is signalled to you by the EOFI flag in MMINT register. This flag may generate an MMC interrupt request as detailed in Section "Interrupt", page 103. When this flag is set, two other flags in MMSTA register: DATFS and CRC16S give a status on the frame received. DATFS indicates if the frame format is correct or not: a valid End bit has been received, and CRC16S indicates if the CRC16 computation is correct or not. In case of data stream CRC16S has no meaning and stays cleared.

According to the MMC specification data transmission from the card starts after the access time delay (formally N_{AC} parameter) beginning from the End bit of the read command. To avoid any locking of the MMC controller when card does not send its data (e.g. physically removed from the bus), you must launch a time-out period to exit from such situation. In case of time-out you may reset the data controller and its internal state machine by setting and clearing the DCR bit in MMCON2 register.

This time-out may be disarmed after receiving 8 data (F1FI flag set) or after receiving end of frame (EOFI flag set) in case of block length less than 8 data (1, 2 or 4).

Data Reading

Data is read from the FIFO by reading to MMDAT register. Each time one FIFO becomes full (F1FI or F2FI set), user is requested to flush this FIFO by reading 8 data.

Figure 54. Data Stream Reception Flows

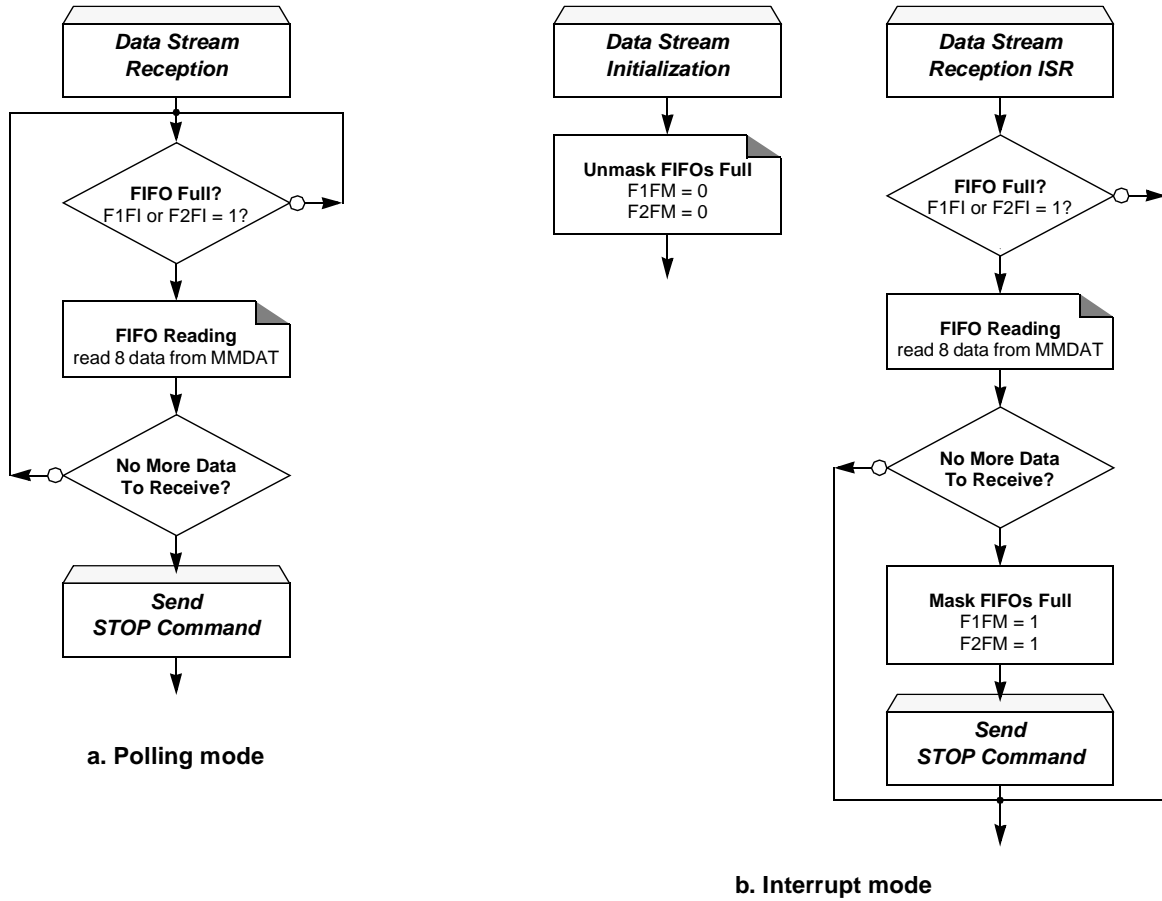
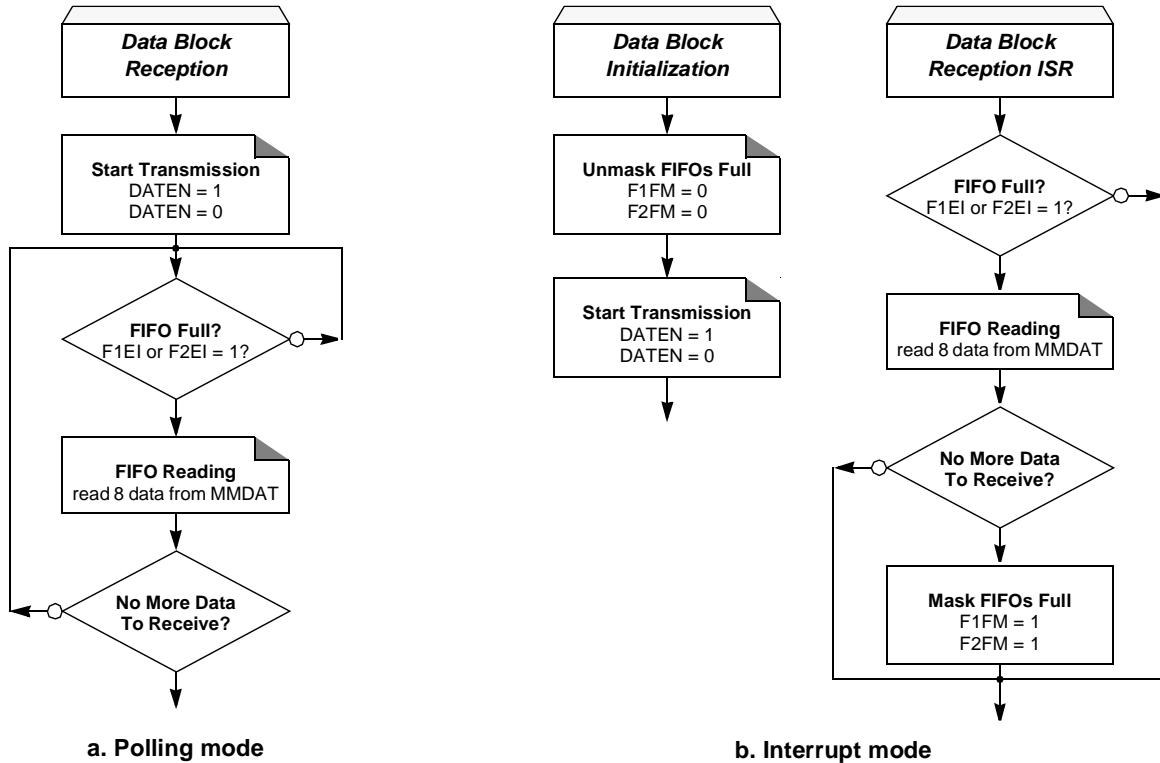


Figure 55. Data Block Reception Flows



Flow Control

To allow transfer at high speed without taking care of CPU oscillator frequency, the FLOWC bit in MMCON2 allows control of the data flow in both transmission and reception.

During transmission, setting the FLOWC bit has the following effects:

- MMCLK is stopped when both FIFOs become empty: F1EI and F2EI set.
- MMCLK is restarted when one of the FIFOs becomes full: F1EI or F2EI cleared.

During reception, setting the FLOWC bit has the following effects:

- MMCLK is stopped when both FIFOs become full: F1FI and F2FI set.
- MMCLK is restarted when one of the FIFOs becomes empty: F1FI or F2FI cleared.

As soon as the clock is stopped, the MMC bus is frozen and remains in its state until the clock is restored by writing or reading data in MMDAT.

Interrupt

Description

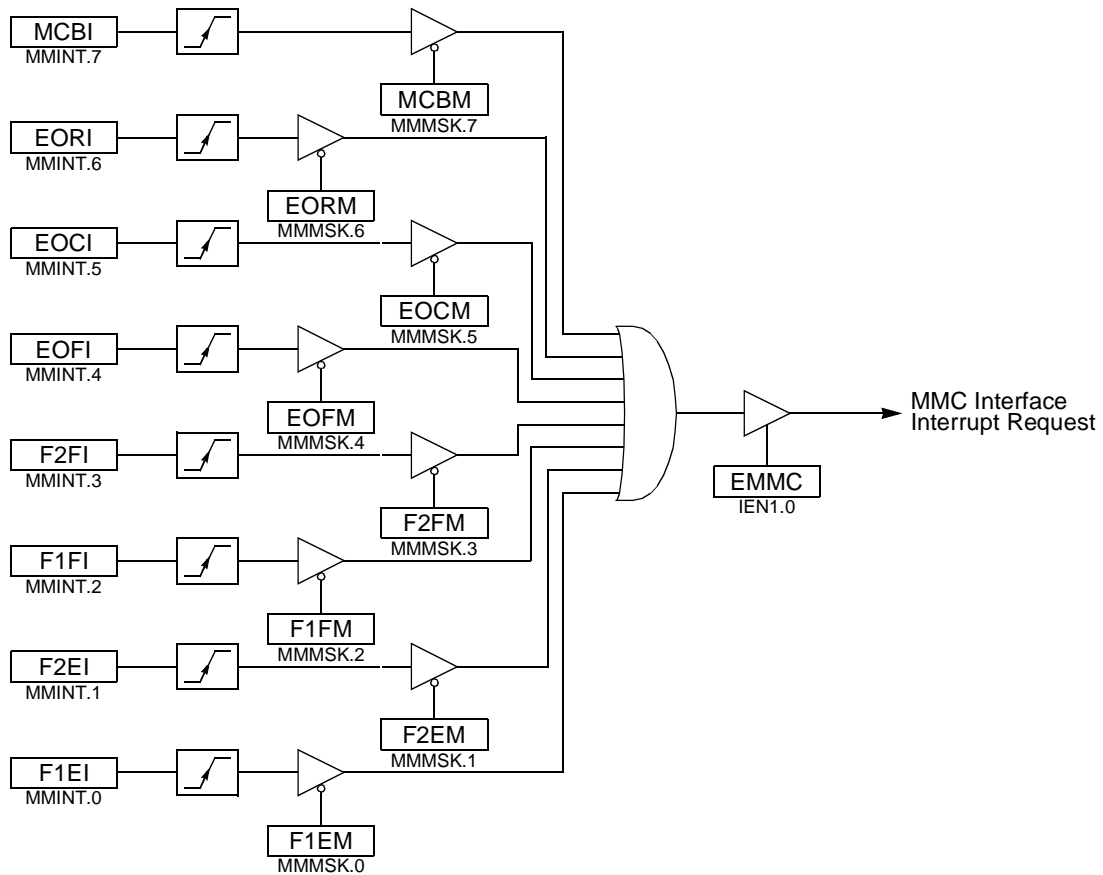
As shown in Figure 56, the MMC controller implements eight interrupt sources reported in MCBi, EORi, EOCi, EOFi, F2Fi, F1Fi, and F2Ei flags in MMCINT register. These flags are detailed in the previous sections.

All these sources are maskable separately using MCBM, EORM, EOCM, EOFM, F2FM, F1FM, and F2EM mask bits respectively in MMMSK register.

The interrupt request is generated each time an unmasked flag is set, and the global MMC controller interrupt enable bit is set (EMMC in IEN1 register).

Reading the MMINT register automatically clears the interrupt flags (acknowledgment). This implies that register content must be saved and tested interrupt flag by interrupt flag to be sure not to forget any interrupts.

Figure 56. MMC Controller Interrupt System



Registers

Table 95. MMCON0 Register

MMCON0 (S:E4h) – MMC Control Register 0

7	6	5	4	3	2	1	0
DRPTR	DTPTR	CRPTR	CTPTR	MBLOCK	DFMT	RFMT	CRCDIS
Bit Number	Bit Mnemonic	Description					
7	DRPTR	Data Receive Pointer Reset Bit Set to reset the read pointer of the data FIFO. Clear to release the read pointer of the data FIFO.					
6	DTPTR	Data Transmit Pointer Reset Bit Set to reset the write pointer of the data FIFO. Clear to release the write pointer of the data FIFO.					
5	CRPTR	Command Receive Pointer Reset Bit Set to reset the read pointer of the receive command FIFO. Clear to release the read pointer of the receive command FIFO.					
4	CTPTR	Command Transmit Pointer Reset Bit Set to reset the write pointer of the transmit command FIFO. Clear to release the read pointer of the transmit command FIFO.					
3	MBLOCK	Multi-block Enable Bit Set to select multi-block data format. Clear to select single block data format.					
2	DFMT	Data Format Bit Set to select the block-oriented data format. Clear to select the stream data format.					
1	RFMT	Response Format Bit Set to select the 48-bit response format. Clear to select the 136-bit response format.					
0	CRCDIS	CRC7 Disable Bit Set to disable the CRC7 computation when receiving a response. Clear to enable the CRC7 computation when receiving a response.					

Reset Value = 0000 0000b

Table 96. MMCON1 Register

MMCON1 (S:E5h) – MMC Control Register 1

	7	6	5	4	3	2	1	0
	BLEN3	BLEN2	BLEN1	BLEN0	DATDIR	DATEN	RESPEN	CMDEN

Bit Number	Bit Mnemonic	Description
7-4	BLEN3:0	Block Length Bits Refer to Table 94 for bits description. Do not program value > 1011b
3	DATDIR	Data Direction Bit Set to select data transfer from host to card (write mode). Clear to select data transfer from card to host (read mode).
2	DATEN	Data Transmission Enable Bit Set and clear to enable data transmission immediately or after response has been received.
1	RESPEN	Response Enable Bit Set and clear to enable the reception of a response following a command transmission.
0	CMDEN	Command Transmission Enable Bit Set and clear to enable transmission of the command FIFO to the card.

Reset Value = 0000 0000b

Table 97. MMCON2 Register

MMCON2 (S:E6h) – MMC Control Register 2

	7	6	5	4	3	2	1	0
	MMCEN	DCR	CCR	-	-	DATD1	DATD0	FLOWC

Bit Number	Bit Mnemonic	Description
7	MMCEN	MMC Clock Enable Bit Set to enable the MCLK clocks and activate the MMC controller. Clear to disable the MMC clocks and freeze the MMC controller.
6	DCR	Data Controller Reset Bit Set and clear to reset the data line controller in case of transfer abort.
5	CCR	Command Controller Reset Bit Set and clear to reset the command line controller in case of transfer abort.
4-3	-	Reserved The value read from these bits is always 0. Do not set these bits.
2-1	DATD1:0	Data Transmission Delay Bits Used to delay the data transmission after a response from 2 MMC clock periods (all bits cleared) to 8 MMC clock periods (all bits set) by step of 2 MMC clock periods.
0	FLOWC	MMC Flow Control Bit Set to enable the flow control during data transfers. Clear to disable the flow control during data transfers.

Reset Value = 0000 0000b



Table 98. MMSTA Register

MMSTA (S:DEh Read Only) – MMC Control and Status Register

7	6	5	4	3	2	1	0
-	-	CBUSY	CRC16S	DATFS	CRC7S	RESPFS	CFLCK
Bit Number	Bit Mnemonic	Description					
7-6	-	Reserved The value read from these bits is always 0. Do not set these bits.					
5	CBUSY	Card Busy Flag Set by hardware when the card sends a busy state on the data line. Cleared by hardware when the card no more sends a busy state on the data line.					
4	CRC16S	CRC16 Status Bit Transmission mode Set by hardware when the token response reports a good CRC. Cleared by hardware when the token response reports a bad CRC. Reception mode Set by hardware when the CRC16 received in the data block is correct. Cleared by hardware when the CRC16 received in the data block is not correct.					
3	DATFS	Data Format Status Bit Transmission mode Set by hardware when the format of the token response is correct. Cleared by hardware when the format of the token response is not correct. Reception mode Set by hardware when the format of the frame is correct. Cleared by hardware when the format of the frame is not correct.					
2	CRC7S	CRC7 Status Bit Set by hardware when the CRC7 computed in the response is correct. Cleared by hardware when the CRC7 computed in the response is not correct. This bit is not relevant when CRCDIS is set.					
1	RESPFS	Response Format Status Bit Set by hardware when the format of a response is correct. Cleared by hardware when the format of a response is not correct.					
0	CFLCK	Command FIFO Lock Bit Set by hardware to signal user not to write in the transmit command FIFO: busy state. Cleared by hardware to signal user the transmit command FIFO is available: idle state.					

Reset Value = 0000 0000b

Table 99. MMINT Register

MMINT (S:E7h Read Only) – MMC Interrupt Register

7	6	5	4	3	2	1	0
MCBI	EORI	EOCI	EOFI	F2FI	F1FI	F2EI	F1EI
Bit Number	Bit Mnemonic	Description					
7	MCBI	MMC Card Busy Interrupt Flag Set by hardware when the card enters or exits its busy state (when the busy signal is asserted or deasserted on the data line). Cleared when reading MMINT.					
6	EORI	End of Response Interrupt Flag Set by hardware at the end of response reception. Cleared when reading MMINT.					
5	EOCI	End of Command Interrupt Flag Set by hardware at the end of command transmission. Clear when reading MMINT.					
4	EOFI	End of Frame Interrupt Flag Set by hardware at the end of frame (stream or block) transfer. Clear when reading MMINT.					
3	F2FI	FIFO 2 Full Interrupt Flag Set by hardware when second FIFO becomes full. Cleared by hardware when second FIFO becomes empty.					
2	F1FI	FIFO 1 Full Interrupt Flag Set by hardware when first FIFO becomes full. Cleared by hardware when first FIFO becomes empty.					
1	F2EI	FIFO 2 Empty Interrupt Flag Set by hardware when second FIFO becomes empty. Cleared by hardware when second FIFO becomes full.					
0	F1EI	FIFO 1 Empty Interrupt Flag Set by hardware when first FIFO becomes empty. Cleared by hardware when first FIFO becomes full.					

Reset Value = 0000 0011b



Table 100. MMMSK Register

MMMSK (S:DFh) – MMC Interrupt Mask Register

	7	6	5	4	3	2	1	0
	MCBM	EORM	EOCM	EOFM	F2FM	F1FM	F2EM	F1EM

Bit Number	Bit Mnemonic	Description
7	MCBM	MMC Card Busy Interrupt Mask Bit Set to prevent MCBI flag from generating an MMC interrupt. Clear to allow MCBI flag to generate an MMC interrupt.
6	EORM	End Of Response Interrupt Mask Bit Set to prevent EORI flag from generating an MMC interrupt. Clear to allow EORI flag to generate an MMC interrupt.
5	EOCM	End Of Command Interrupt Mask Bit Set to prevent EOCI flag from generating an MMC interrupt. Clear to allow EOCI flag to generate an MMC interrupt.
4	EOFM	End Of Frame Interrupt Mask Bit Set to prevent EOFI flag from generating an MMC interrupt. Clear to allow EOFI flag to generate an MMC interrupt.
3	F2FM	FIFO 2 Full Interrupt Mask Bit Set to prevent F2FI flag from generating an MMC interrupt. Clear to allow F2FI flag to generate an MMC interrupt.
2	F1FM	FIFO 1 Full Interrupt Mask Bit Set to prevent F1FI flag from generating an MMC interrupt. Clear to allow F1FI flag to generate an MMC interrupt.
1	F2EM	FIFO 2 Empty Interrupt Mask Bit Set to prevent F2EI flag from generating an MMC interrupt. Clear to allow F2EI flag to generate an MMC interrupt.
0	F1EM	FIFO 1 Empty Interrupt Mask Bit Set to prevent F1EI flag from generating an MMC interrupt. Clear to allow F1EI flag to generate an MMC interrupt.

Reset Value = 1111 1111b

Table 101. MMCMD Register

MMCMD (S:DDh) – MMC Command Register

	7	6	5	4	3	2	1	0
	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0

Bit Number	Bit Mnemonic	Description
7 - 0	MC7:0	MMC Command Receive Byte Output (read) register of the response FIFO. MMC Command Transmit Byte Input (write) register of the command FIFO.

Reset Value = 1111 1111b

Table 102. MMDAT Register

MMDAT (S:DCh) – MMC Data Register

7	6	5	4	3	2	1	0
MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0
Bit Number	Bit Mnemonic	Description					
7 - 0	MD7:0	MMC Data Byte Input (write) or output (read) register of the data FIFO.					

Reset Value = 1111 1111b

Table 103. MMCLK Register

MMCLK (S:EDh) – MMC Clock Divider Register

7	6	5	4	3	2	1	0
MMCD7	MMCD6	MMCD5	MMCD4	MMCD3	MMCD2	MMCD1	MMCD0
Bit Number	Bit Mnemonic	Description					
7 - 0	MMCD7:0	MMC Clock Divider 8-bit divider for MMC clock generation.					

Reset Value = 0000 0000b

IDE/ATAPI Interface

The AT8xC51SND1A provides an IDE/ATAPI interface allowing connection of devices such as CD-ROM reader, CompactFlash cards, Hard Disk Drive, etc. It consists of a 16-bit data transfer (read or write) between the AT8xC51SND1A and the IDE device.

Description

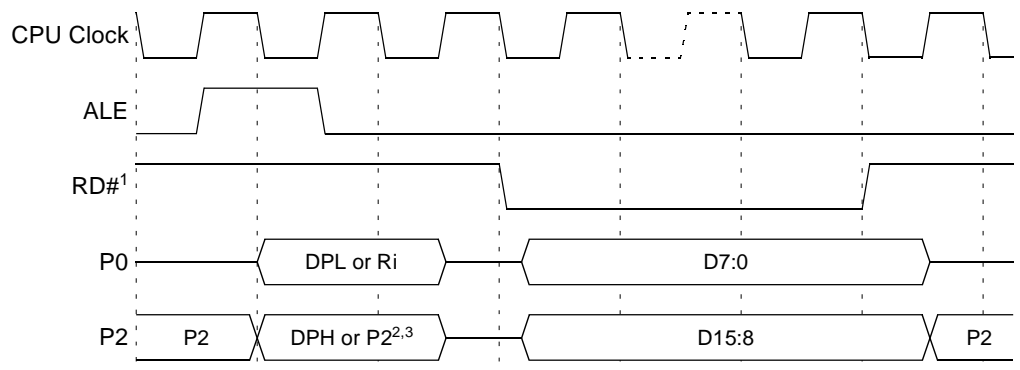
The IDE interface mode is enabled by setting the EXT16 bit in AUXR (see Figure 13, page 23). As soon as this bit is set, all MOVX instructions read or write are done in a 16-bit mode compare to the standard 8-bit mode. P0 carries the low order multiplexed address and data bus (A7:0, D7:0) while P2 carries the high order multiplexed address and data bus (A15:8, D15:8). When writing data in IDE mode, the ACC contains D7:0 data (as in 8-bit mode) while DAT16H register (see Table 105) contains D15:8 data. When reading data in IDE mode, D7:0 data is returned in ACC while D15:8 data is returned in DAT16H.

Figure 22 shows the IDE read bus cycle while Figure 23 shows the IDE write bus cycle. For simplicity, these figures depict the bus cycle waveforms in idealized form and do not provide precise timing information. For IDE bus cycle timing parameters refer to the Section “AC Characteristics” of the AT8xC51SND1A datasheet.

IDE cycle takes 6 CPU clock periods which is equivalent to 12 oscillator clock periods in standard mode or 6 oscillator clock periods in X2 mode. For further information on X2 mode, refer to the Section “X2 Feature”, page 4.

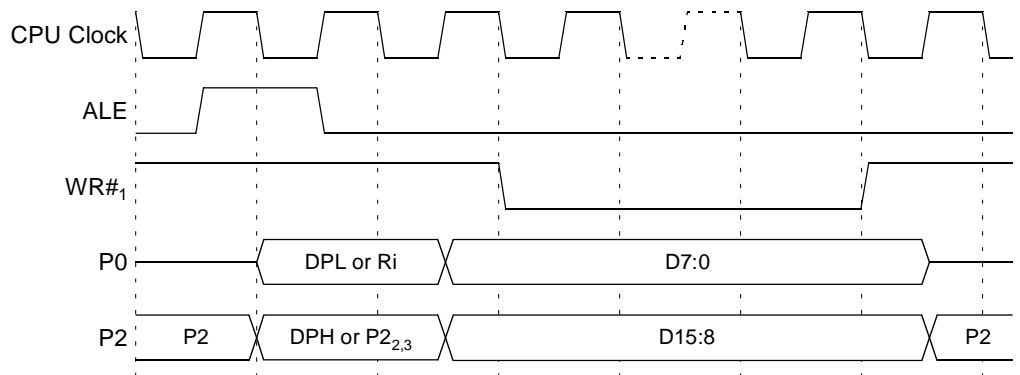
Slow IDE devices can be accessed by stretching the read and write cycles. This is done using the M0 bit in AUXR. Setting this bit changes the width of the RD# and WR# signals from 3 to 15 CPU clock periods.

Figure 22. IDE Read Waveforms



- Notes:
1. RD# signal may be stretched using M0 bit in AUXR register.
 2. When executing MOVX @Ri instruction, P2 outputs SFR content.
 3. When executing MOVX @DPTR instruction, if DPHDIS is set (Page Access Mode), P2 outputs SFR content instead of DPH.

Figure 23. IDE Write Waveforms



- Notes:
1. WR# signal may be stretched using M0 bit in AUXR register.
 2. When executing MOVX @Ri instruction, P2 outputs SFR content.
 3. When executing MOVX @DPTR instruction, if DPHDIS is set (Page Access Mode), P2 outputs SFR content instead of DPH.

IDE Device Connection

Figure 24 and Figure 25 show two examples on how to interface up to two IDE devices to the AT8xC51SND1A. In both examples P0 carries IDE low order data bits D7:0, P2 carries IDE high order data bits D15:8, while RD# and WR# signals are respectively connected to the IDE nIOR and nIOW signals. Other IDE control signals are generated by the address latch outputs in the first example while they are generated by some port I/Os in the second one.

Figure 24. IDE Device Connection Example 1

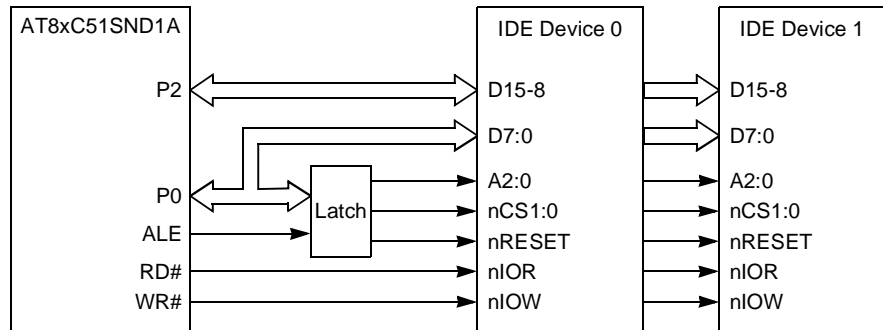


Figure 25. IDE Device Connection Example 2

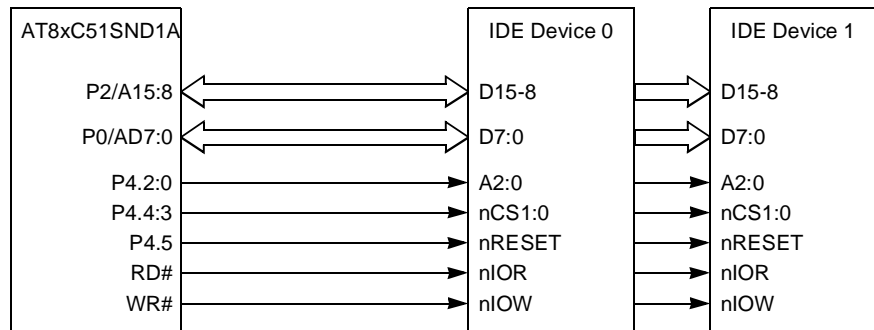


Table 104. External Data Memory Interface Signals

Signal Name	Type	Description	Alternate Function
A15:8	I/O	Address Lines Upper address lines for the external bus. Multiplexed higher address and data lines for the IDE interface.	P2.7:0
AD7:0	I/O	Address/Data Lines Multiplexed lower address and data lines for the IDE interface.	P0.7:0
ALE	O	Address Latch Enable ALE signals indicates that valid address information is available on lines AD7:0.	-
RD#	O	Read Read signal output to external data memory.	P3.7
WR#	O	Write Write signal output to external memory.	P3.6

Registers

Table 105. DAT16H Register

DAT16H (S:F9h) – Data 16 High Order Byte

7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8
Bit Number	Bit Mnemonic	Description					
7 - 0	D15:8	Data 16 High Order Byte When EXT16 bit is set, DAT16H is set by software with the high order data byte prior any MOVX write instruction. When EXT16 bit is set, DAT16H contains the high order data byte after any MOVX read instruction.					

Reset Value = 0000 0000b

Serial I/O Port

The serial I/O port in the AT8xC51SND1A provides both synchronous and asynchronous communication modes. It operates as a Synchronous Receiver and Transmitter in one single mode (Mode 0) and operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous modes support framing error detection and multiprocessor communication with automatic address recognition.

Mode Selection

SM0 and SM1 bits in SCON register (see Figure 108) are used to select a mode among the single synchronous and the three asynchronous modes according to Table 106.

Table 106. Serial I/O Port Mode Selection

SM0	SM1	Mode	Description	Baud Rate
0	0	0	Synchronous Shift Register	Fixed/Variable
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fixed
1	1	3	9-bit UART	Variable

Baud Rate Generator

Depending on the mode and the source selection, the baud rate can be generated from either the Timer 1 or the Internal Baud Rate Generator. The Timer 1 can be used in Modes 1 and 3 while the Internal Baud Rate Generator can be used in Modes 0, 1 and 3.

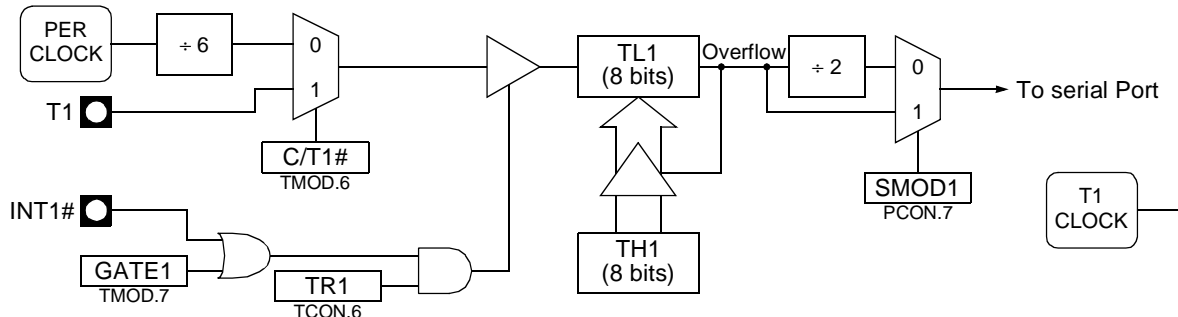
The addition of the Internal Baud Rate Generator allows freeing of the Timer 1 for other purposes in the application. It is highly recommended to use the Internal Baud Rate Generator as it allows higher and more accurate baud rates than Timer 1.

Baud rate formulas depend on the modes selected and are given in the following mode sections.

Timer 1

When using Timer 1, the Baud Rate is derived from the overflow of the timer. As shown in Figure 57 Timer 1 is used in its 8-bit auto-reload mode (detailed in Section "Mode 2 (8-bit Timer with Auto-Reload)", page 47). SMOD1 bit in PCON register allows doubling of the generated baud rate.

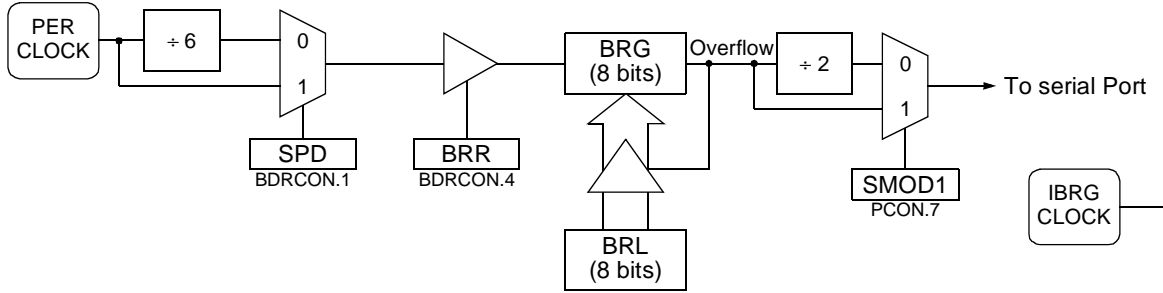
Figure 57. Timer 1 Baud Rate Generator Block Diagram



Internal Baud Rate Generator

When using the Internal Baud Rate Generator, the Baud Rate is derived from the overflow of the timer. As shown in Figure 58 the Internal Baud Rate Generator is an 8-bit auto-reload timer feed by the peripheral clock or by the peripheral clock divided by 6 depending on the SPD bit in BDRCON register (see Table 112). The Internal Baud Rate Generator is enabled by setting BBR bit in BDRCON register. SMOD1 bit in PCON register allows doubling of the generated baud rate.

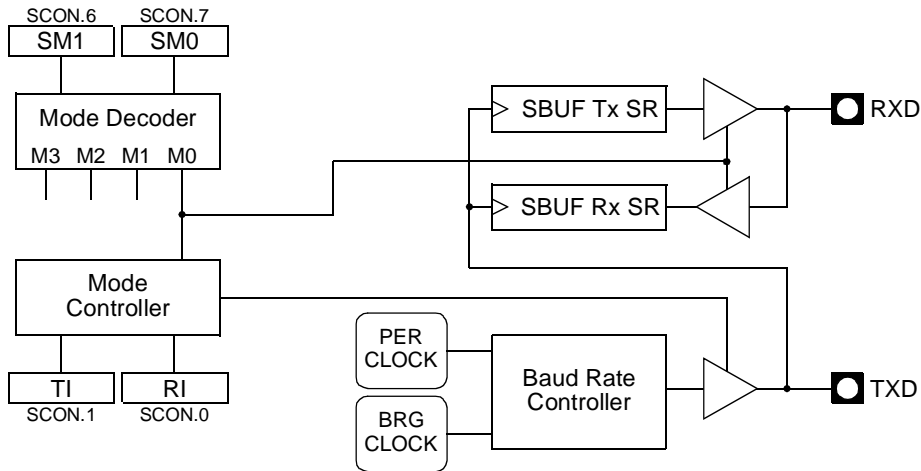
Figure 58. Internal Baud Rate Generator Block Diagram



Synchronous Mode (Mode 0)

Mode 0 is a half-duplex, synchronous mode, which is commonly used to expand the I/O capabilities of a device with shift registers. The transmit data (TXD) pin outputs a set of eight clock pulses while the receive data (RXD) pin transmits or receives a byte of data. The 8-bit data are transmitted and received least-significant bit (LSB) first. Shifts occur at a fixed Baud Rate (see Section "Baud Rate Selection (Mode 0)", page 115). Figure 59 shows the serial port block diagram in Mode 0.

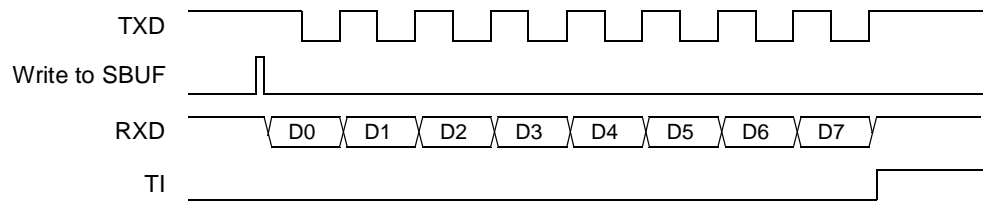
Figure 59. Serial I/O Port Block Diagram (Mode 0)



Transmission (Mode 0)

To start a transmission mode 0, write to SCON register clearing bits SM0, SM1. As shown in Figure 26, writing the byte to transmit to SBUF register starts the transmission. Hardware shifts the LSB (D0) onto the RXD pin during the first clock cycle composed of a high level then low level signal on TXD. During the eighth clock cycle the MSB (D7) is on the RXD pin. Then, hardware drives the RXD pin high and asserts TI to indicate the end of the transmission.

Figure 26. Transmission Waveforms (Mode 0)

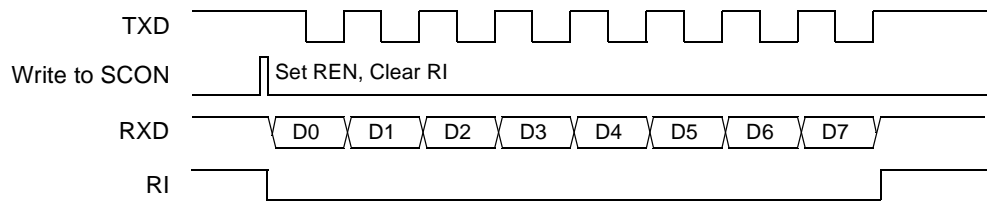


Reception (Mode 0)

To start a reception in mode 0, write to SCON register clearing SM0, SM1 and RI bits and setting the REN bit.

As shown in Figure 27, Clock is pulsed and the LSB (D0) is sampled on the RXD pin. The D0 bit is then shifted into the shift register. After eight sampling, the MSB (D7) is shifted into the shift register, and hardware asserts RI bit to indicate a completed reception. Software can then read the received byte from SBUF register.

Figure 27. Reception Waveforms (Mode 0)



Baud Rate Selection (Mode 0)

In mode 0, the baud rate can be either fixed or variable. As shown in Figure 28, the selection is done using M0SRC bit in BDRCON register. Figure 29 gives the baud rate calculation formulas for each baud rate source.

Figure 28. Baud Rate Source Selection (mode 0)

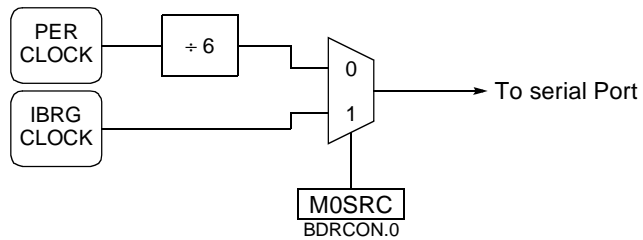


Figure 29. Baud Rate Formulas (Mode 0)

$$\text{Baud_Rate} = \frac{F_{\text{PER}}}{6}$$

a. Fixed Formula

$$\text{Baud_Rate} = \frac{2^{\text{SMOD}1} \cdot F_{\text{PER}}}{6^{(1-\text{SPD})} \cdot 32 \cdot (256 - \text{BRL})}$$

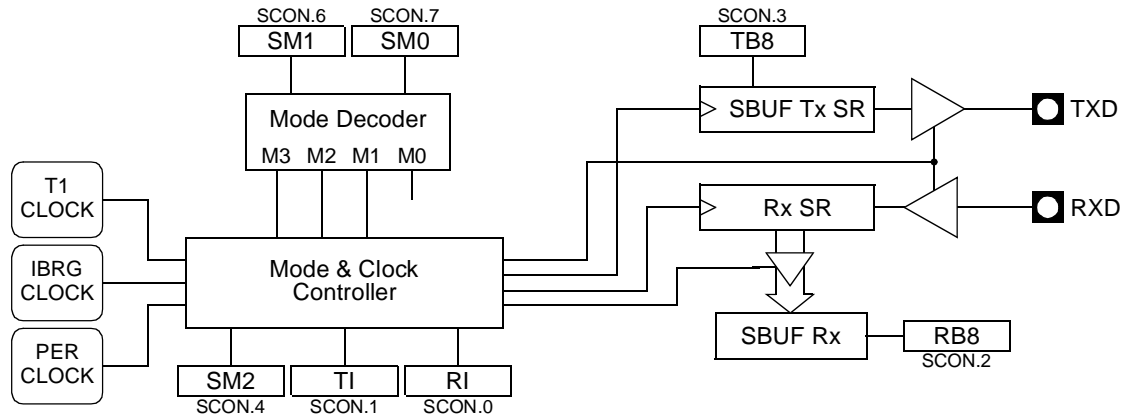
$$\text{BRL} = 256 - \frac{2^{\text{SMOD}1} \cdot F_{\text{PER}}}{6^{(1-\text{SPD})} \cdot 32 \cdot \text{Baud_Rate}}$$

b. Variable Formula

Asynchronous Modes (Modes 1, 2 and 3)

The Serial Port has one 8-bit and two 9-bit asynchronous modes of operation. Figure 60 shows the Serial Port block diagram in such asynchronous modes.

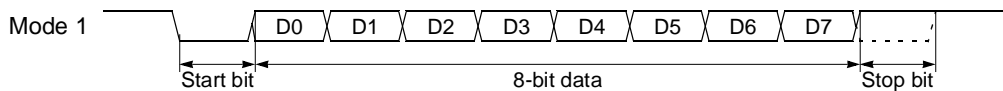
Figure 60. Serial I/O Port Block Diagram (Modes 1, 2 and 3)



Mode 1

Mode 1 is a full-duplex, asynchronous mode. The data frame (see Figure 61) consists of 10 bits: one start, eight data bits and one stop bit. Serial data is transmitted on the TXD pin and received on the RXD pin. When a data is received, the stop bit is read in the RB8 bit in SCON register.

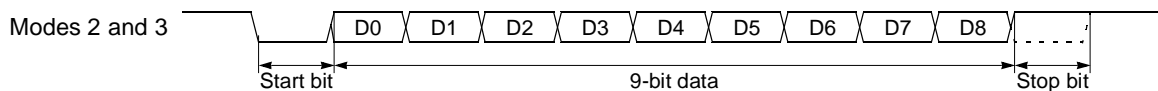
Figure 61. Data Frame Format (Mode 1)



Modes 2 and 3

Modes 2 and 3 are full-duplex, asynchronous modes. The data frame (see Figure 62) consists of 11 bits: one start bit, eight data bits (transmitted and received LSB first), one programmable ninth data bit and one stop bit. Serial data is transmitted on the TXD pin and received on the RXD pin. On receive, the ninth bit is read from RB8 bit in SCON register. On transmit, the ninth data bit is written to TB8 bit in SCON register. Alternatively, you can use the ninth bit as a command/data flag.

Figure 62. Data Frame Format (Modes 2 and 3)



Transmission (Modes 1, 2 and 3)

To initiate a transmission, write to SCON register, setting SM0 and SM1 bits according to Table 106, and setting the ninth bit by writing to TB8 bit. Then, writing the byte to be transmitted to SBUF register starts the transmission.

Reception (Modes 1, 2 and 3)

To prepare for reception, write to SCON register, setting SM0 and SM1 bits according to Table 106, and set the REN bit. The actual reception is then initiated by a detected high-to-low transition on the RXD pin.

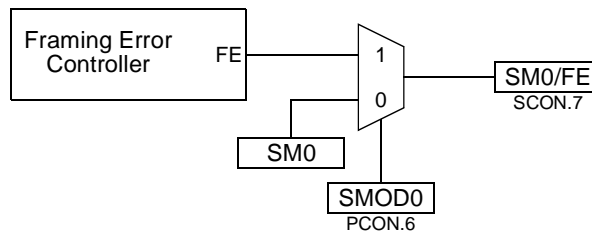
Framing Error Detection (Modes 1, 2 and 3)

Framing error detection is provided for the three asynchronous modes. To enable the framing bit error detection feature, set SMOD0 bit in PCON register as shown in Figure 63.

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two devices. If a valid stop bit is not found, the software sets FE bit in SCON register.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a chip reset clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When the framing error detection feature is enabled, RI rises on stop bit instead of the last data bit as detailed in Figure 67.

Figure 63. Framing Error Block Diagram



Baud Rate Selection (Modes 1 and 3)

In modes 1 and 3, the Baud Rate is derived either from the Timer 1 or the Internal Baud Rate Generator and allows different baud rate in reception and transmission. As shown in Figure 64 the selection is done using RBCK and TBCK bits in BDRCON register.

Figure 65 gives the baud rate calculation formulas for each baud rate source while Table 107 details Internal Baud Rate Generator configuration for different peripheral clock frequencies and giving baud rates closer to the standard baud rates.

Figure 64. Baud Rate Source Selection (Modes 1 and 3)

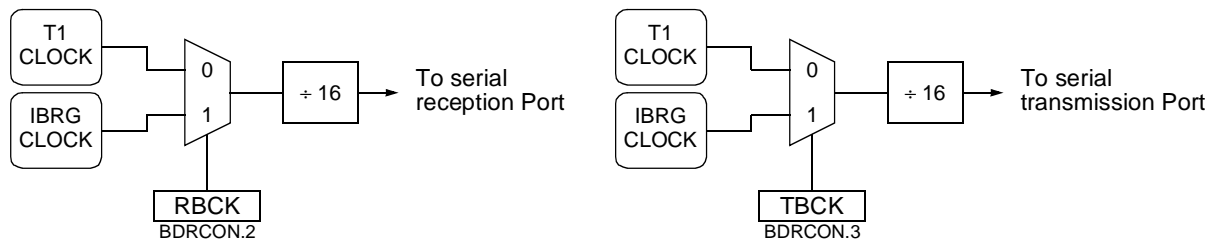


Figure 65. Baud Rate Formulas (Modes 1 and 3)

$$\text{Baud_Rate} = \frac{2^{\text{SMOD1}} \cdot \text{F}_{\text{PER}}}{6^{(1-\text{SPD})} \cdot 32 \cdot (256 - \text{BRL})}$$

$$\text{BRL} = 256 - \frac{2^{\text{SMOD1}} \cdot \text{F}_{\text{PER}}}{6^{(1-\text{SPD})} \cdot 32 \cdot \text{Baud_Rate}}$$

a. IBRG Formula

$$\text{Baud_Rate} = \frac{2^{\text{SMOD1}} \cdot \text{F}_{\text{PER}}}{6 \cdot 32 \cdot (256 - \text{TH1})}$$

$$\text{TH1} = 256 - \frac{2^{\text{SMOD1}} \cdot \text{F}_{\text{PER}}}{192 \cdot \text{Baud_Rate}}$$

b. T1 Formula

Table 107. Internal Baud Rate Generator Value

Baud Rate	$F_{PER} = 6 \text{ MHz}^{(1)}$				$F_{PER} = 8 \text{ MHz}^{(1)}$				$F_{PER} = 10 \text{ MHz}^{(1)}$			
	SPD	SMOD1	BRL	Error%	SPD	SMOD1	BRL	Error%	SPD	SMOD1	BRL	Error%
115200	-	-	-	-	-	-	-	-	-	-	-	-
57600	-	-	-	-	1	1	247	3.55	1	1	245	1.36
38400	1	1	246	2.34	1	1	243	0.16	1	1	240	1.73
19200	1	1	236	2.34	1	1	230	0.16	1	1	223	1.36
9600	1	1	217	0.16	1	1	204	0.16	1	1	191	0.16
4800	1	1	178	0.16	1	1	152	0.16	1	1	126	0.16

Baud Rate	$F_{PER} = 12 \text{ MHz}^{(2)}$				$F_{PER} = 16 \text{ MHz}^{(2)}$				$F_{PER} = 20 \text{ MHz}^{(2)}$			
	SPD	SMOD1	BRL	Error%	SPD	SMOD1	BRL	Error%	SPD	SMOD1	BRL	Error%
115200	-	-	-	-	1	1	247	3.55	1	1	245	1.36
57600	1	1	243	0.16	1	1	239	2.12	1	1	234	1.36
38400	1	1	236	2.34	1	1	230	0.16	1	1	223	1.36
19200	1	1	217	0.16	1	1	204	0.16	1	1	191	0.16
9600	1	1	178	0.16	1	1	152	0.16	1	1	126	0.16
4800	1	1	100	0.16	1	1	48	0.16	1	0	126	0.16

Notes: 1. These frequencies are achieved in X1 mode, $F_{PER} = F_{OSC} \div 2$.
 2. These frequencies are achieved in X2 mode, $F_{PER} = F_{OSC}$.

Baud Rate Selection (Mode 2) In mode 2, the baud rate can only be programmed to two fixed values: 1/16 or 1/32 of the peripheral clock frequency. As shown in Figure 30 the selection is done using SMOD1 bit in PCON register. Figure 31 gives the baud rate calculation formula depending on the selection.

Figure 30. Baud Rate Generator Selection (mode 2)

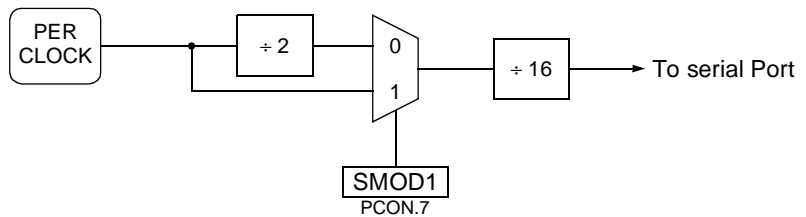


Figure 31. Baud Rate Formula (Mode 2)

$$\text{Baud_Rate} = \frac{2^{\text{SMOD1}} \cdot \text{F}_{\text{PER}}}{32}$$

Multiprocessor Communication (Modes 2 and 3)

Modes 2 and 3 provide a ninth-bit mode to facilitate multiprocessor communication. To enable this feature, set SM2 bit in SCON register. When the multiprocessor communication feature is enabled, the Serial Port can differentiate between data frames (ninth bit clear) and address frames (ninth bit set). This allows the AT8xC51SND1A to function as a slave processor in an environment where multiple slave processors share a single serial line.

When the multiprocessor communication feature is enabled, the receiver ignores frames with the ninth bit clear. The receiver examines frames with the ninth bit set for an address match. If the received address matches the slaves address, the receiver hardware sets RB8 and RI bits in SCON register, generating an interrupt.

The addressed slave's software then clears SM2 bit in SCON register and prepares to receive the data bytes. The other slaves are unaffected by these data bytes because they are waiting to respond to their own addresses.

Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the Serial Port to examine the address of each incoming command frame. Only when the Serial Port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e., setting SM2 bit in SCON register in mode 0 has no effect).

Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be 1111 1111b.

For example:

```
SADDR = 0101 0110b
SADEN = 1111 1100b
Given = 0101 01XXb
```

The following is an example of how to use given addresses to address different slaves:

```
Slave A: SADDR = 1111 0001b
SADEN = 1111 1010b
```



```

Given = 1111 0X0Xb
Slave B:SADDR = 1111 0011b
SADEN = 1111 1001b
Given = 1111 0XX1b
Slave C:SADDR = 1111 0010b
SADEN = 1111 1101b
Given = 1111 00X1b

```

The SADEN byte is selected so that each slave may be addressed separately. For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000B). For slave A, bit 1 is a 0; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves A and B, but not slave C, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011B). To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001B).

Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

```

SADDR = 0101 0110b
SADEN = 1111 1100b
(SADDR | SADEN) = 1111 111Xb

```

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh.

The following is an example of using broadcast addresses:

```

Slave A:SADDR = 1111 0001b
SADEN = 1111 1010b
Given = 1111 1X11b,

Slave B:SADDR = 1111 0011b
SADEN = 1111 1001b
Given = 1111 1X11b,

Slave C:SADDR = 1111 0010b
SADEN = 1111 1101b
Given = 1111 1111b,

```

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send the address FFh.

To communicate with slaves A and B, but not slave C, the master must send the address FBh.

Reset Address

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the Serial Port is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

Interrupt

The Serial I/O Port handles two interrupt sources that are the “end of reception” (RI in SCON) and “end of transmission” (TI in SCON) flags. As shown in Figure 66 these flags are combined together to appear as a single interrupt source for the C51 core. Flags must be cleared by software when executing the serial interrupt service routine.

The serial interrupt is enabled by setting ES bit in IEN0 register. This assumes interrupts are globally enabled by setting EA bit in IEN0 register.

Depending on the selected mode and whether the framing error detection is enabled or not, RI flag is set during the stop bit or during the ninth bit as detailed in Figure 67.

Figure 66. Serial I/O Interrupt System

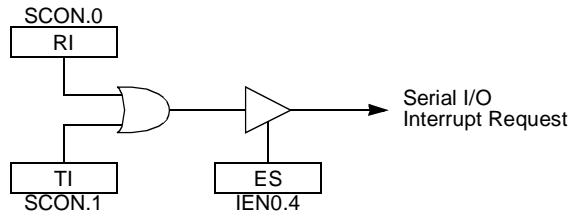
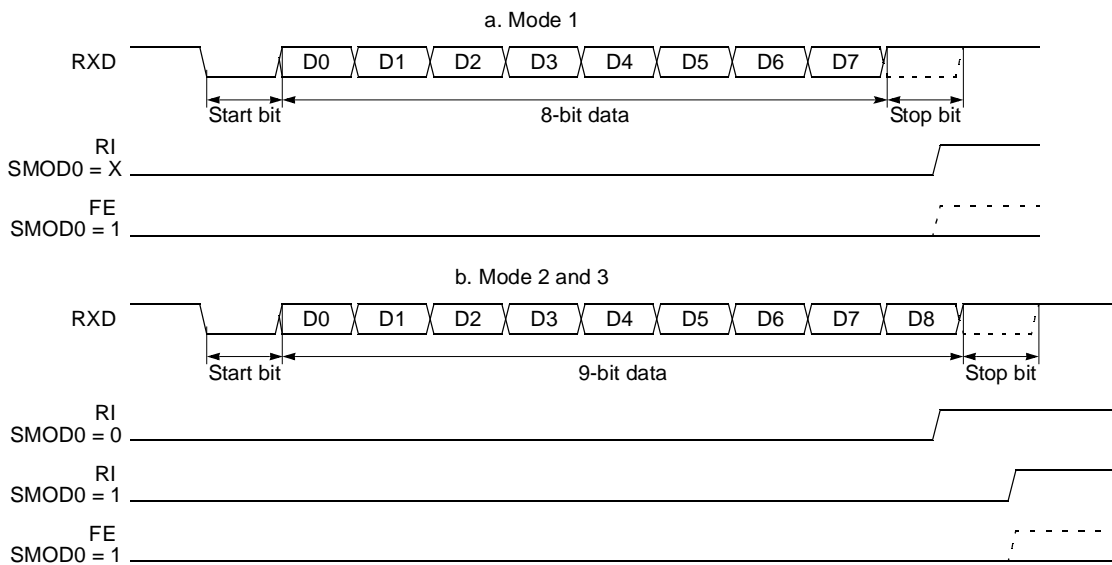


Figure 67. Interrupt Waveforms



Registers

Table 108. SCON Register

SCON (S:98h) – Serial Control Register

7	6	5	4	3	2	1	0	
FE/SM0	OVR/SM1	SM2	REN	TB8	RB8	TI	RI	
Bit Number	Bit Mnemonic	Description						
7	FE	Framing Error Bit To select this function, set SMOD0 bit in PCON register. Set by hardware to indicate an invalid stop bit. Must be cleared by software.						
	SM0	Serial Port Mode Bit 0 Refer to Table 106 for mode selection.						
6	SM1	Serial Port Mode Bit 1 Refer to Table 106 for mode selection.						
5	SM2	Serial Port Mode Bit 2 Set to enable the multiprocessor communication and automatic address recognition features. Clear to disable the multiprocessor communication and automatic address recognition features.						
4	REN	Receiver Enable Bit Set to enable reception. Clear to disable reception.						
3	TB8	Transmit Bit 8 Modes 0 and 1: Not used. Modes 2 and 3: Software writes the ninth data bit to be transmitted to TB8.						
2	RB8	Receiver Bit 8 Mode 0: Not used. Mode 1 (SM2 cleared): Set or cleared by hardware to reflect the stop bit received. Modes 2 and 3 (SM2 set): Set or cleared by hardware to reflect the ninth bit received.						
1	TI	Transmit Interrupt Flag Set by the transmitter after the last data bit is transmitted. Must be cleared by software.						
0	RI	Receive Interrupt Flag Set by the receiver after the stop bit of a frame has been received. Must be cleared by software.						

Reset Value = 0000 0000b

Table 109. SBUF Register

SBUF (S:99h) – Serial Buffer Register

7	6	5	4	3	2	1	0
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Bit Number	Bit Mnemonic	Description					
7 - 0	SD7:0	Serial Data Byte Read the last data received by the Serial I/O Port. Write the data to be transmitted by the Serial I/O Port.					

Reset value = XXXX XXXXb

Table 110. SADDR Register

SADDR (S:A9h) – Slave Individual Address Register

7	6	5	4	3	2	1	0
SAD7	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0
Bit Number	Bit Mnemonic	Description					
7 - 0	SAD7:0	Slave Individual Address.					

Reset Value = 0000 0000b

Table 111. SADEN Register

SADEN (S:B9h) – Slave Individual Address Mask Byte Register

7	6	5	4	3	2	1	0
SAE7	SAE6	SAE5	SAE4	SAE3	SAE2	SAE1	SAE0
Bit Number	Bit Mnemonic	Description					
7 - 0	SAE7:0	Slave Address Mask Byte.					

Reset Value = 0000 0000b



Table 112. BDRCON Register

BDRCON (S:92h) – Baud Rate Generator Control Register

	7	6	5	4	3	2	1	0
	-	-	-	BRR	TBCK	RBCK	SPD	M0SRC

Bit Number	Bit Mnemonic	Description
7-5	-	Reserved The value read from these bits are indeterminate. Do not set these bits.
4	BRR	Baud Rate Run Bit Set to enable the baud rate generator. Clear to disable the baud rate generator.
3	TBCK	Transmission Baud Rate Selection Bit Set to select the baud rate generator as transmission baud rate generator. Clear to select the Timer 1 as transmission baud rate generator.
2	RBCK	Reception Baud Rate Selection Bit Set to select the baud rate generator as reception baud rate generator. Clear to select the Timer 1 as reception baud rate generator.
1	SPD	Baud Rate Speed Bit Set to select high speed baud rate generation. Clear to select low speed baud rate generation.
0	M0SRC	Mode 0 Baud Rate Source Bit Set to select the variable baud rate generator in Mode 0. Clear to select fixed baud rate in Mode 0.

Reset Value = XXX0 0000b

Table 113. BRL Register

BRL (S:91h) – Baud Rate Generator Reload Register

	7	6	5	4	3	2	1	0
	BRL7	BRL6	BRL5	BRL4	BRL3	BRL2	BRL1	BRL0

Bit Number	Bit Mnemonic	Description
7 - 0	BRL7:0	Baud Rate Reload Value.

Reset Value = 0000 0000b

Synchronous Peripheral Interface

The AT8xC51SND1A implements a Synchronous Peripheral Interface with master and slave modes capability.

Figure 68 shows an SPI bus configuration using the AT8xC51SND1A as master connected to slave peripherals while Figure 69 shows an SPI bus configuration using the AT8xC51SND1A as slave of an other master.

The bus is made of three wires connecting all the devices together:

- Master Output Slave Input (MOSI): it is used to transfer data in series from the master to a slave. It is driven by the master.
- Master Input Slave Output (MISO): it is used to transfer data in series from a slave to the master. It is driven by the selected slave.
- Serial Clock (SCK): it is used to synchronize the data transmission both in and out the devices through their MOSI and MISO lines. It is driven by the master for eight clock cycles which allows to exchange one byte on the serial lines.

Each slave peripheral is selected by one Slave Select pin (SS#). If there is only one slave, it may be continuously selected with SS# tied to a low level. Otherwise, the AT8xC51SND1A may select each device by software through port pins (Pn.x). Special care should be taken not to select two slaves at the same time to avoid bus conflicts.

Figure 68. Typical Master SPI Bus Configuration

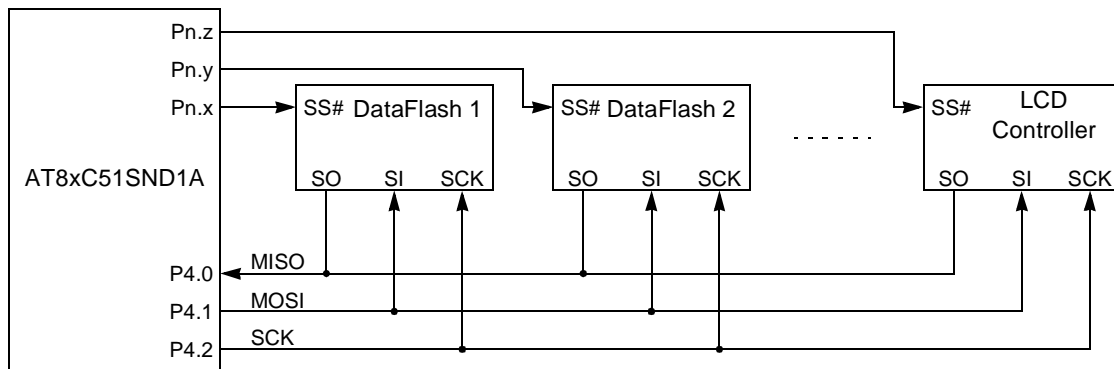
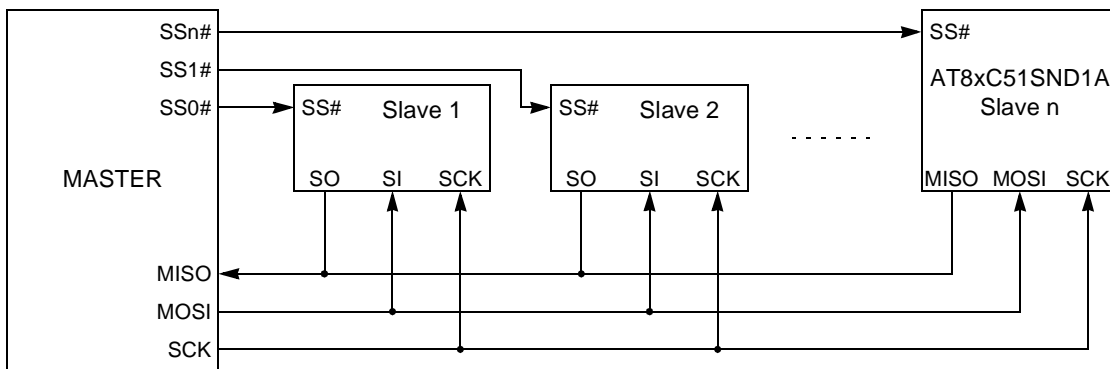


Figure 69. Typical Slave SPI Bus Configuration



Description

The SPI controller interfaces with the C51 core through three special function registers: SPCON, the SPI control register (see Table 115); SPSTA, the SPI status register (see Table 116); and SPDAT, the SPI data register (see Table 117).

Master Mode

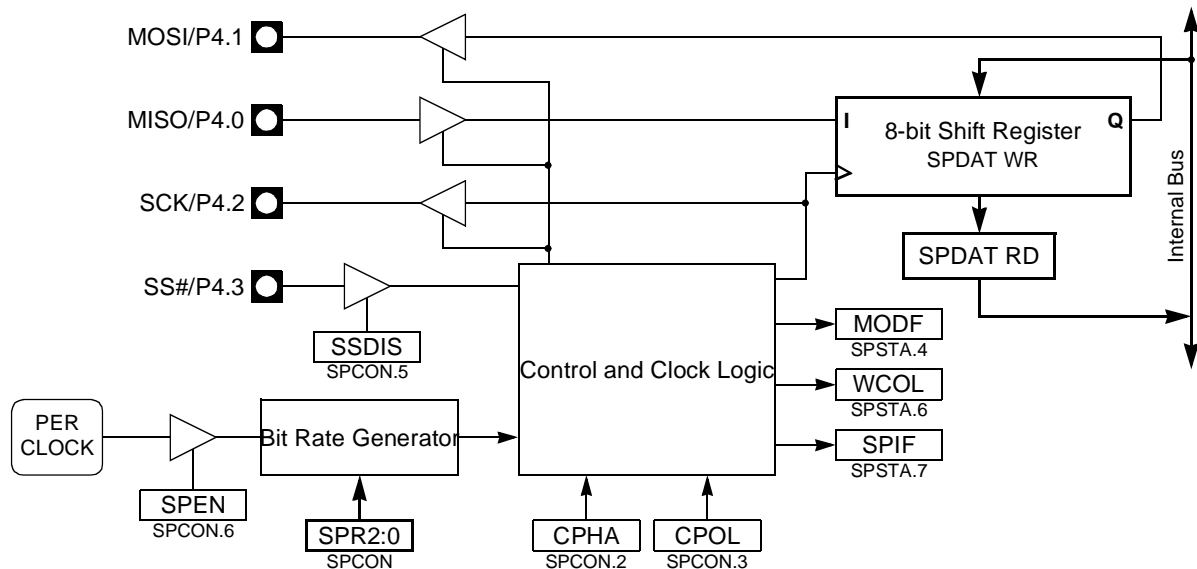
The SPI operates in master mode when the MSTR bit in SPCON is set.

Figure 70 shows the SPI block diagram in master mode. Only a master SPI module can initiate transmissions. Software begins the transmission by writing to SPDAT. Writing to SPDAT writes to the shift register while reading SPDAT reads an intermediate register updated at the end of each transfer.

The byte begins shifting out on the MOSI pin under the control of the bit rate generator. This generator also controls the shift register of the slave peripheral through the SCK output pin. As the byte shifts out, another byte shifts in from the slave peripheral on the MISO pin. The byte is transmitted most significant bit (MSB) first. The end of transfer is signaled by SPIF being set.

In case of the AT8xC51SND1A is the only master on the bus, it can be useful not to use SS# pin and get it back to I/O functionality. This is achieved by setting SSDIS bit in SPCON.

Figure 70. SPI Master Mode Block Diagram



Note: MSTR bit in SPCON is set to select master mode.

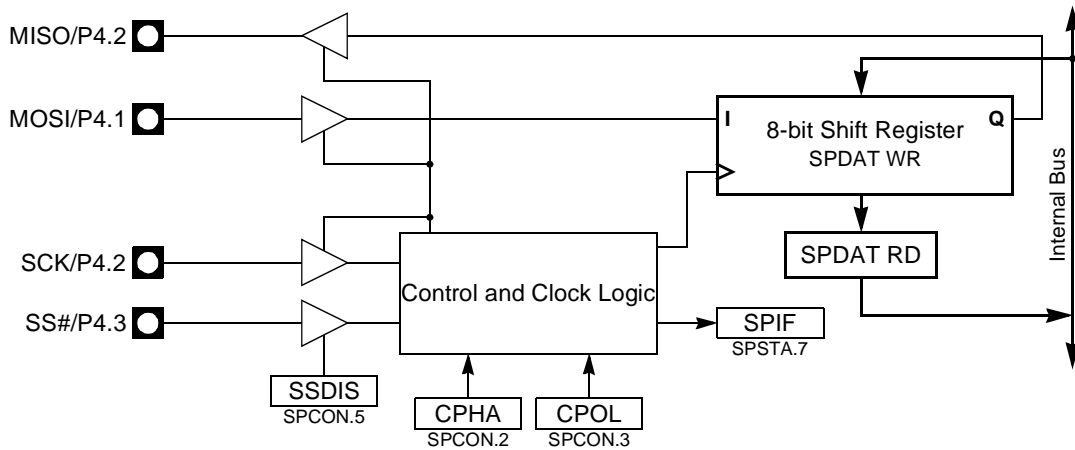
Slave Mode

The SPI operates in slave mode when the MSTR bit in SPCON is cleared and a data has been loaded in SPDAT.

Figure 71 shows the SPI block diagram in slave mode. In slave mode, before a data transmission occurs, the SS# pin of the slave SPI must be asserted to low level. SS# must remain low until the transmission of the byte is complete. In the slave SPI module, data enters the shift register through the MOSI pin under the control of the serial clock provided by the master SPI module on the SCK input pin. When the master starts a transmission, the data in the shift register begins shifting out on the MISO pin. The end of transfer is signaled by SPIF being set.

In case of the AT8xC51SND1A is the only slave on the bus, it can be useful not to use SS# pin and get it back to I/O functionality. This is achieved by setting SSDIS bit in SPCON. This bit has no effect when CPHA is cleared (see Section "SS# Management", page 128).

Figure 71. SPI Slave Mode Block Diagram



Note: MSTR bit in SPCON is cleared to select slave mode.

Bit Rate

The bit rate can be selected from seven predefined bit rates using the SPR2, SPR1 and SPR0 control bits in SPCON according to Table 114. These bit rates are derived from the peripheral clock (F_{PER}) issued from the Clock Controller block as detailed in Section , page 4.

Table 114. Serial Bit Rates

SPR2	SPR1	SPR0	Bit Rate (kHz) Vs F_{PER}						F_{PER} Divider
			6 MHz ¹	8 MHz ¹	10 MHz ¹	12 MHz ²	16 MHz ²	20 MHz ²	
0	0	0	3000	4000	5000	6000	8000	10000	2
0	0	1	1500	2000	2500	3000	4000	5000	4
0	1	0	750	1000	1250	1500	2000	2500	8
0	1	1	375	500	625	750	1000	1250	16
1	0	0	187.5	250	312.5	375	500	625	32
1	0	1	93.75	125	156.25	187.5	250	312.5	64
1	1	0	46.875	62.5	78.125	93.75	125	156.25	128
1	1	1	6000	8000	10000	12000	16000	20000	1

Notes: 1. These frequencies are achieved in X1 mode, $F_{PER} = F_{OSC} \div 2$.
 2. These frequencies are achieved in X2 mode, $F_{PER} = F_{OSC}$.

Data Transfer

The Clock Polarity bit (CPOL in SPCON) defines the default SCK line level in idle state¹ while the Clock Phase bit (CPHA in SPCON) defines the edges on which the input data are sampled and the edges on which the output data are shifted (see Figure 72 and Figure 73). The SI signal is output from the selected slave and the SO signal is the output from the master. The AT8xC51SND1A is capturing data from the SI line while the selected slave is capturing data from the SO line.

For simplicity, the accompanying figures depict the SPI waveforms in idealized form and do not provide precise timing information. For timing parameters refer to the Section “AC Characteristics” of the AT8xC51SND1A datasheet.

Note: 1. When the peripheral is disabled (SPEN = 0), default SCK line is high level.

Figure 72. Data Transmission Format (CPHA = 0)

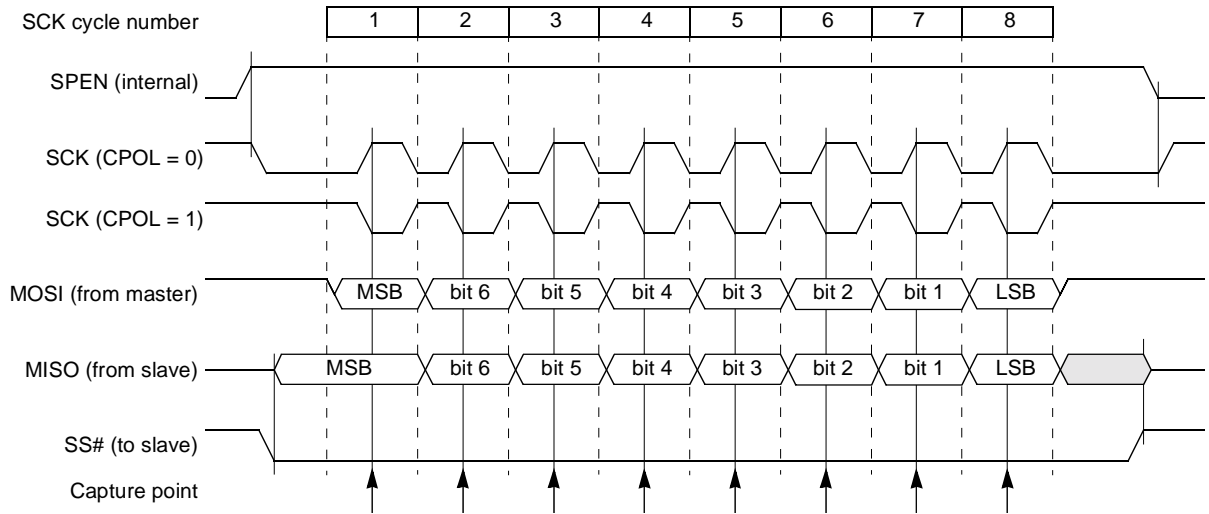
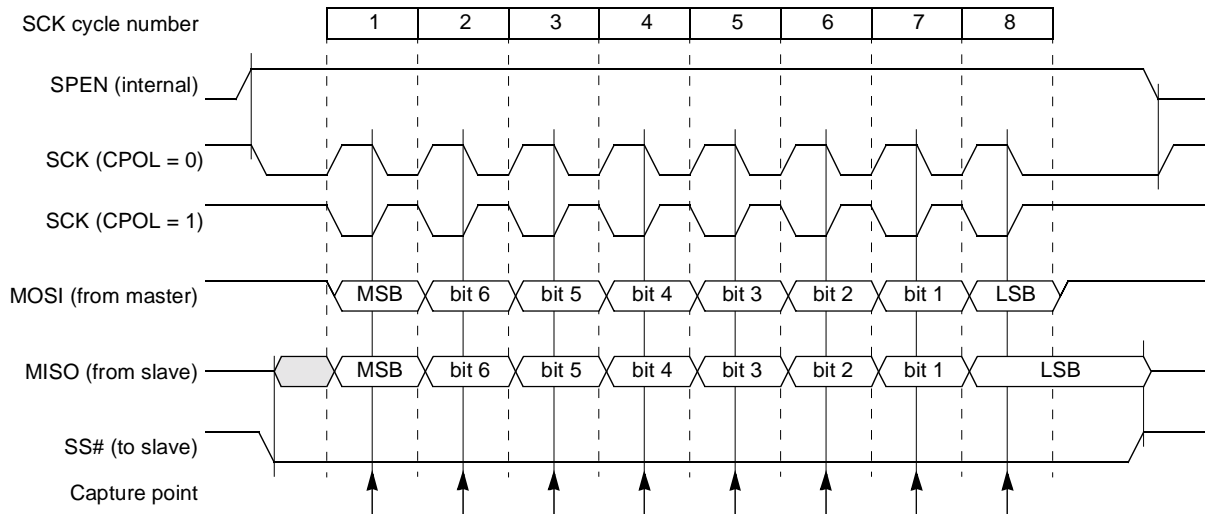


Figure 73. Data Transmission Format (CPHA = 1)

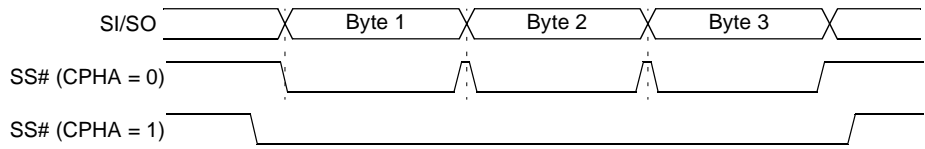


SS# Management

Figure 72 shows an SPI transmission with CPHA = 0, where the first SCK edge is the MSB capture point. Therefore the slave starts to output its MSB as soon as it is selected: SS# asserted to low level. SS# must then be deasserted between each byte transmission (see Figure 32). SPDAT must be loaded with a data before SS# is asserted again.

Figure 73 shows an SPI transmission with CPHA = 1, where the first SCK edge is used by the slave as a start of transmission signal. Therefore SS# may remain asserted between each byte transmission (see Figure 32).

Figure 32. SS# Timing Diagram



Error Conditions

The following flags signal the SPI error conditions:

- **MODF** in SPSTA signals a mode fault.
 MODF flag is relevant only in master mode when SS# usage is enabled (SSDIS bit cleared). It signals when set that an other master on the bus has asserted SS# pin and so, may create a conflict on the bus with two master sending data at the same time.
 A mode fault automatically disables the SPI (SPEN cleared) and configures the SPI in slave mode (MSTR cleared).
 MODF flag can trigger an interrupt as explained in Section "Interrupt", page 129.
 MODF flag is cleared by reading SPSTA and re-configuring SPI by writing to SPCON.
- **WCOL** in SPSTA signals a write collision.
 WCOL flag is set when SPDAT is loaded while a transfer is on-going. In this case data is not written to SPDAT and transfer continue uninterrupted. WCOL flag does not trigger any interrupt and is relevant jointly with SPIF flag.
 WCOL flag is cleared after reading SPSTA and writing new data to SPDAT while no transfer is on-going.

Interrupt

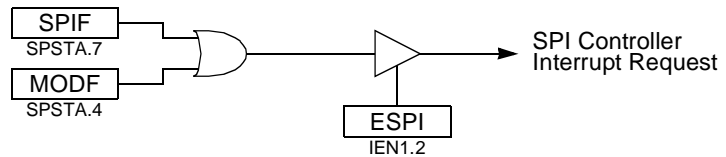
The SPI handles two interrupt sources that are the “end of transfer” and the “mode fault” flags.

As shown in Figure 33 these flags are combined together to appear as a single interrupt source for the C51 core. The SPIF flag is set at the end of an 8-bit shift in and out and is cleared by reading SPSTA and then reading from or writing to SPDAT.

The MODF flag is set in case of mode fault error and is cleared by reading SPSTA and then writing to SPCON.

The SPI interrupt is enabled by setting ESPI bit in IEN1 register. This assumes interrupts are globally enabled by setting EA bit in IEN0 register.

Figure 33. SPI Interrupt System



Configuration

The SPI configuration is made through SPCON.

Master Configuration

The SPI operates in master mode when the MSTR bit in SPCON is set.

Slave Configuration

The SPI operates in slave mode when the MSTR bit in SPCON is cleared and a data has been loaded is SPDAT.

Data Exchange

There are two possible Policies to exchange data in master and slave modes:

- polling
- interrupts

Master Mode with Polling Policy

Figure 34 shows the initialization phase and the transfer phase flows using the polling policy. Using this flow prevent any overrun error occurrence.

The bit rate is selected according to Table 114.

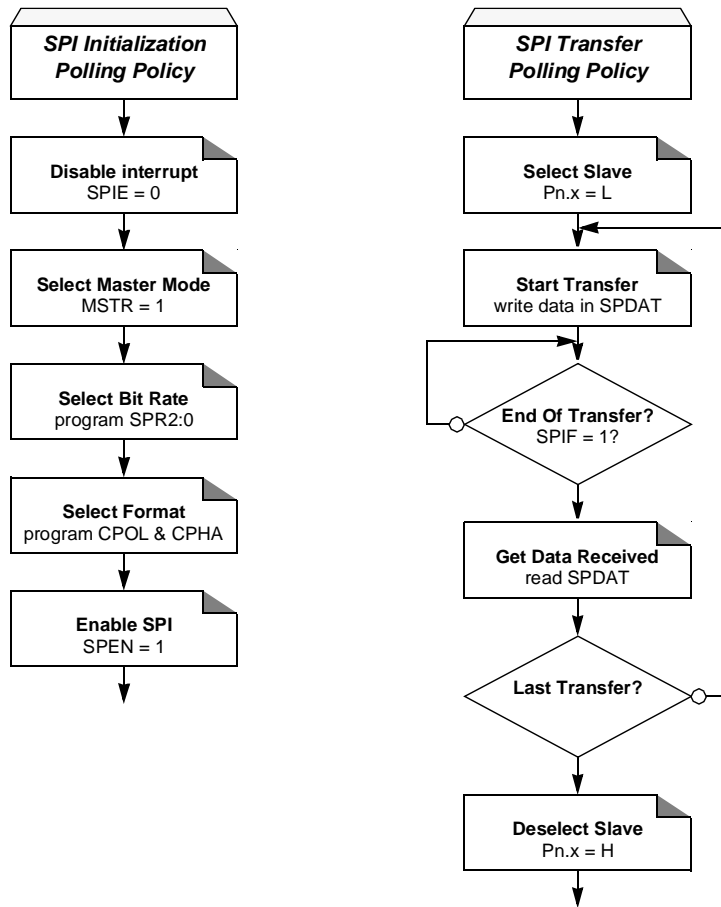
The transfer format depends on the slave peripheral.

SS# may be deasserted between transfers depending also on the slave peripheral.

SPIF flag is cleared when reading SPDAT (SPSTA has been read before by the “end of transfer” check).

This policy provides the fastest effective transmission and is well adapted when communicating at high speed with other Microcontrollers. However, the procedure may then be interrupted at any time by higher priority tasks.

Figure 34. Master SPI Polling Policy Flows



Master Mode with Interrupt Policy

Figure 35 shows the initialization phase and the transfer phase flows using the interrupt policy. Using this flow prevent any overrun error occurrence.

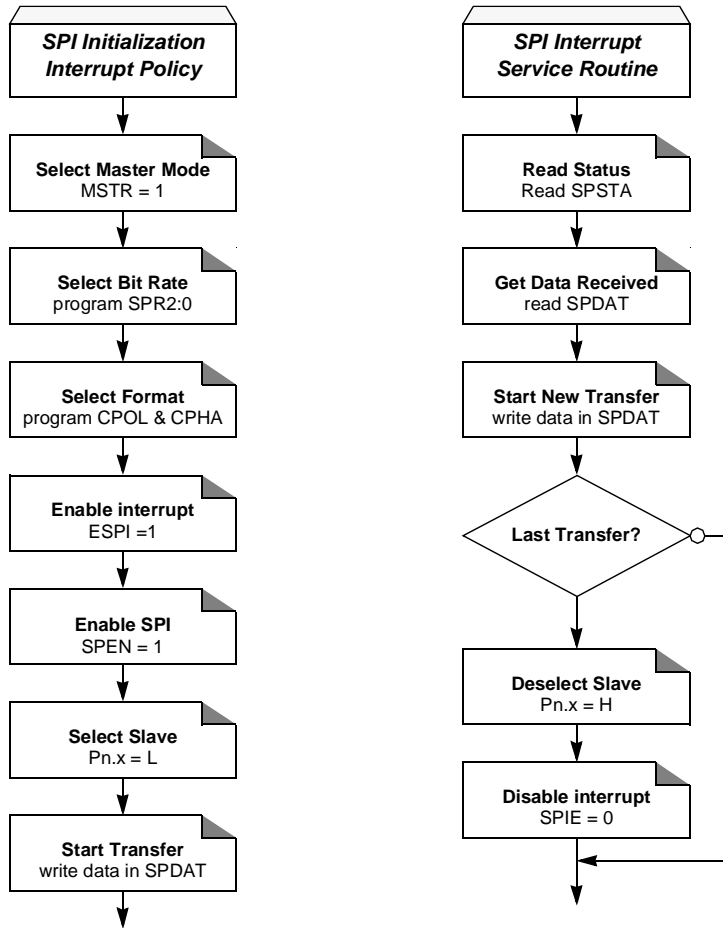
The bit rate is selected according to Table 114.

The transfer format depends on the slave peripheral.

SS# may be deasserted between transfers depending also on the slave peripheral.

Reading SPSTA at the beginning of the ISR is mandatory for clearing the SPIF flag. Clear is effective when reading SPDAT.

Figure 35. Master SPI Interrupt Policy Flows



Slave Mode with Polling Policy

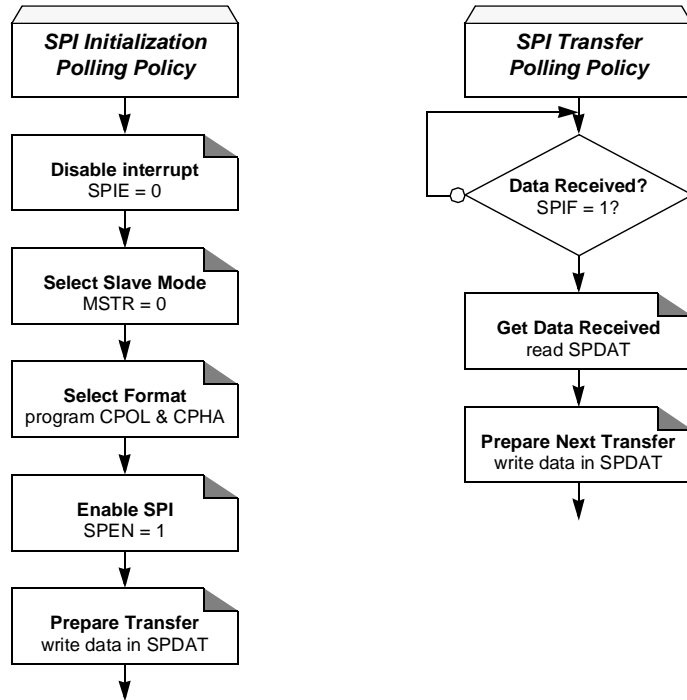
Figure 36 shows the initialization phase and the transfer phase flows using the polling policy.

The transfer format depends on the master controller.

SPIF flag is cleared when reading SPDAT (SPSTA has been read before by the “end of reception” check).

This policy provides the fastest effective transmission and is well adapted when communicating at high speed with other Microcontrollers. However, the procedure may then be interrupted at any time by higher priority tasks.

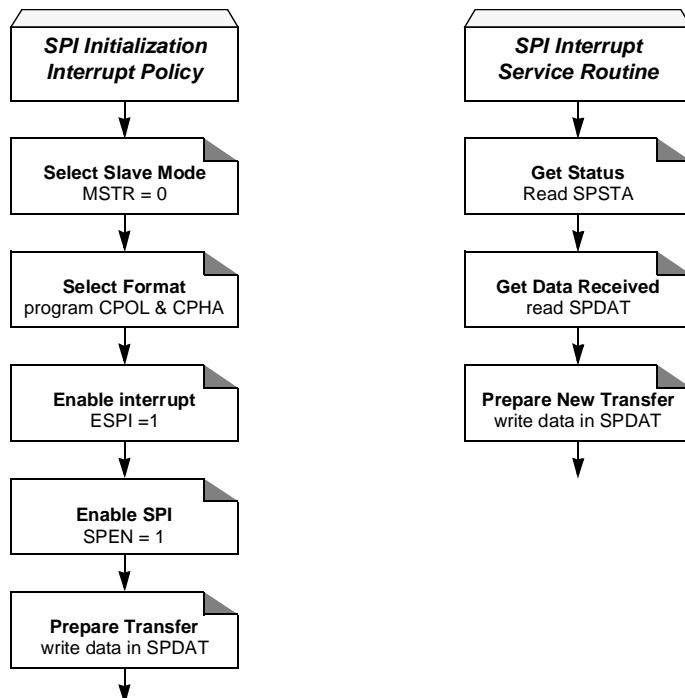
Figure 36. Slave SPI Polling Policy Flows



Slave Mode with Interrupt Policy

Figure 35 shows the initialization phase and the transfer phase flows using the interrupt policy. The transfer format depends on the master controller. Reading SPSTA at the beginning of the ISR is mandatory for clearing the SPIF flag. Clear is effective when reading SPDAT.

Figure 37. Slave SPI Interrupt Policy Flows



Registers

Table 115. SPCON Register

SPCON (S:C3h) – SPI Control Register

7	6	5	4	3	2	1	0
SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0
Bit Number	Bit Mnemonic	Description					
7	SPR2	SPI Rate Bit 2 Refer to Table 114 for bit rate description.					
6	SPEN	SPI Enable Bit Set to enable the SPI interface. Clear to disable the SPI interface.					
5	SSDIS	Slave Select Input Disable Bit Set to disable SS# in both master and slave modes. In slave mode this bit has no effect if CPHA = 0. Clear to enable SS# in both master and slave modes.					
4	MSTR	Master Mode Select Set to select the master mode. Clear to select the slave mode.					
3	CPOL	SPI Clock Polarity Bit⁽¹⁾ Set to have the clock output set to high level in idle state. Clear to have the clock output set to low level in idle state.					
2	CPHA	SPI Clock Phase Bit Set to have the data sampled when the clock returns to idle state (see CPOL). Clear to have the data sampled when the clock leaves the idle state (see CPOL).					
1-0	SPR1:0	SPI Rate Bits 0 and 1 Refer to Table 114 for bit rate description.					

Reset Value = 0001 0100b

Note: 1. When the SPI is disabled, SCK outputs high level.

Table 116. SPSTA Register

SPSTA (S:C4h) – SPI Status Register

	7	6	5	4	3	2	1	0
	SPIF	WCOL	-	MODF	-	-	-	-

Bit Number	Bit Mnemonic	Description
7	SPIF	SPI Interrupt Flag Set by hardware when an 8-bit shift is completed. Cleared by hardware when reading or writing SPDAT after reading SPSTA.
6	WCOL	Write Collision Flag Set by hardware to indicate that a collision has been detected. Cleared by hardware to indicate that no collision has been detected.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	MODF	Mode Fault Set by hardware to indicate that the SS# pin is at an appropriate level. Cleared by hardware to indicate that the SS# pin is at an inappropriate level.
3:0	-	Reserved The value read from these bits is indeterminate. Do not set these bits.

Reset Value = 00000 0000b

Table 117. SPDAT Register

SPDAT (S:C5h) – Synchronous Serial Data Register

	7	6	5	4	3	2	1	0
	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0

Bit Number	Bit Mnemonic	Description
7 - 0	SPD7:0	Synchronous Serial Data.

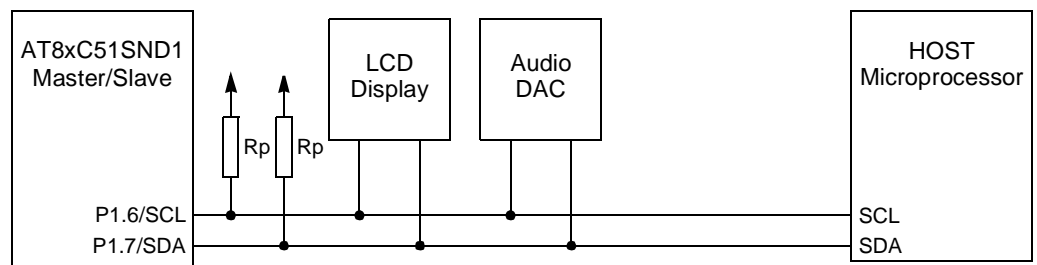
Reset Value = XXXX XXXXb

Two-wire Controller

The AT8xC51SND1A implements a two-wire controller supporting the four standard master and slave modes with multimaster capability. Thus it allows connection of slave devices like LCD controller, audio DAC... but also external master controlling where the AT8xC51SND1A is used as a peripheral of a host.

The two-wire bus is a bi-directional two-wire serial communication standard. It is designed primarily for simple but efficient integrated circuit control. The system is comprised of two lines, SCL (Serial Clock) and SDA (Serial Data) that carry information between the ICs connected to them. The serial data transfer is limited to 100 Kbit/s in low speed mode, however, some higher bit rates can be achieved depending on the oscillator frequency. Various communication configurations can be designed using this bus. Figure 38 shows a typical two-wire bus configuration using the AT8xC51SND1A in master and slave modes. All the devices connected to the bus can be master and slave.

Figure 38. Typical Two-wire Bus Configuration



Description

The CPU interfaces to the two-wire logic via the following four 8-bit special function registers: the Synchronous Serial Control register (SSCON SFR, see Table 125), the Synchronous Serial Data register (SSDAT SFR, see Table 127), the Synchronous Serial Status register (SSSTA SFR, see Table 126) and the Synchronous Serial Address register (SSADR SFR, see Table 128).

SSCON is used to enable the controller, to program the bit rate (see Table 125), to enable slave modes, to acknowledge or not a received data, to send a START or a STOP condition on the two-wire bus, and to acknowledge a serial interrupt. An hardware reset disables the two-wire controller.

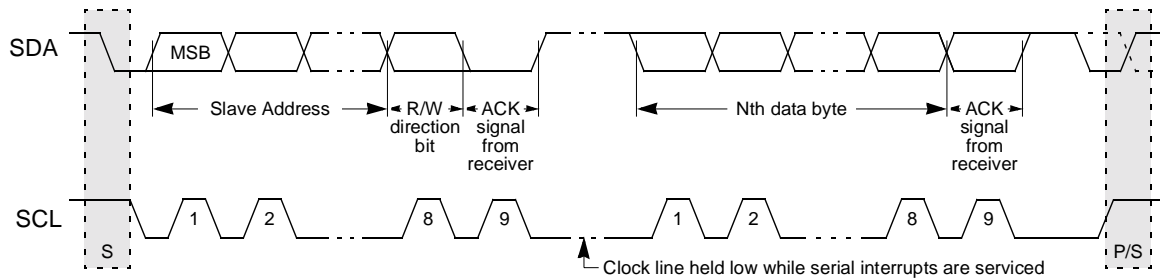
SSSTA contains a status code which reflects the status of the two-wire logic and the two-wire bus. The three least significant bits are always zero. The five most significant bits contains the status code. There are 26 possible status codes. When SSSTA contains F8h, no relevant state information is available and no serial interrupt is requested. A valid status code is available in SSSTA after SSI is set by hardware and is still present until SSI has been reset by software. Table 119 to Table 128 give the status for both master and slave modes and miscellaneous states.

SSDAT contains a byte of serial data to be transmitted or a byte which has just been received. It is addressable while it is not in process of shifting a byte. This occurs when two-wire logic is in a defined state and the serial interrupt flag is set. Data in SSDAT remains stable as long as SSI is set. While data is being shifted out, data on the bus is simultaneously shifted in; SSDAT always contains the last byte present on the bus.

SSADR may be loaded with the 7-bit slave address (7 most significant bits) to which the controller will respond when programmed as a slave transmitter or receiver. The LSB is used to enable general call address (00h) recognition.

Figure 74 shows how a data transfer is accomplished on the two-wire bus.

Figure 74. Complete Data Transfer on Two-wire Bus



The four operating modes are:

- Master Transmitter
- Master Receiver
- Slave transmitter
- Slave receiver

Data transfer in each mode of operation are shown in Figure 75 to Figure 78. These figures contain the following abbreviations:

- A Acknowledge bit (low level at SDA)
- \bar{A} Not acknowledge bit (high level on SDA)
- Data 8-bit data byte
- S START condition
- P STOP condition
- MR Master Receive
- MT Master Transmit
- SLA Slave Address
- GCA General Call Address (00h)
- R Read bit (high level at SDA)
- W Write bit (low level at SDA)

In Figure 75 to Figure 78, circles are used to indicate when the serial interrupt flag is set. The numbers in the circles show the status code held in SSSTA. At these points, a service routine must be executed to continue or complete the serial transfer. These service routines are not critical since the serial transfer is suspended until the serial interrupt flag is cleared by software.

When the serial interrupt routine is entered, the status code in SSSTA is used to branch to the appropriate service routine. For each status code, the required software action and details of the following serial transfer are given in Table 119 to Table 78.

Bit Rate

The bit rate can be selected from seven predefined bit rates or from a programmable bit rate generator using the SSCR2, SSCR1, and SSCR0 control bits in SSCON (see Table 125). The predefined bit rates are derived from the peripheral clock (F_{PER}) issued from the Clock Controller block as detailed in Section "Oscillator", page 4, while bit rate generator is based on timer 1 overflow output.

Table 118. Serial Clock Rates

SSCR2	SSCR1	SSCR0	Bit Frequency (kHz)			F_{PER} Divided By
			$F_{PER} = 6 \text{ MHz}$	$F_{PER} = 8 \text{ MHz}$	$F_{PER} = 10 \text{ MHz}$	
0	0	0	47	62.5	78.125	256
0	0	1	53.5	71.5	89.3	224
0	1	0	62.5	83	104.2 ⁽¹⁾	192
0	1	1	75	100	125 ⁽¹⁾	160
1	0	0	12.5	16.5	20.83	960
1	0	1	100	133.3 ⁽¹⁾	166.7 ⁽¹⁾	120
1	1	0	200 ⁽¹⁾	266.7 ⁽¹⁾	333.3 ⁽¹⁾	60
1	1	1	$0.5 < \cdot < 125^{(1)}$	$0.67 < \cdot < 166.7^{(1)}$	$0.81 < \cdot < 208.3^{(1)}$	$96 \cdot (256 - \text{reload value Timer 1})$

Note: These bit rates are outside of the low speed standard specification limited to 100 kHz but can be used with high speed two-wire components limited to 400 kHz.

Master Transmitter Mode

In the master transmitter mode, a number of data bytes are transmitted to a slave receiver (see Figure 75). Before the master transmitter mode can be entered, SSCON must be initialized as follows:

SSCR2	SSPE	SSSTA	SSSTO	SSI	SSAA	SSCR1	SSCR0
Bit Rate	1	0	0	0	X	Bit Rate	Bit Rate

SSCR2:0 define the serial bit rate (see Table 118). SSPE must be set to enable the controller. SSSTA, SSSTO and SSI must be cleared.

The master transmitter mode may now be entered by setting the SSSTA bit. The two-wire logic will now monitor the two-wire bus and generate a START condition as soon as the bus becomes free. When a START condition is transmitted, the serial interrupt flag (SSI bit in SSCON) is set, and the status code in SSSTA is 08h. This status must be used to vector to an interrupt routine that loads SSDAT with the slave address and the data direction bit (SLA+W). The serial interrupt flag (SSI) must then be cleared before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgment bit has been received, SSI is set again and a number of status code in SSSTA are possible. There are 18h, 20h or 38h for the master mode and also 68h, 78h or B0h if the slave mode was enabled (SSAA = logic 1). The appropriate action to be taken for each of these status code is detailed in Table 119. This scheme is repeated until a STOP condition is transmitted.

SSPE and SSCR2:0 are not affected by the serial transfer and are not referred to in Table 119. After a repeated START condition (state 10h) the controller may switch to the master receiver mode by loading SSDAT with SLA+R.

Master Receiver Mode

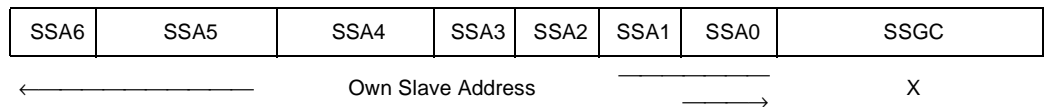
In the master receiver mode, a number of data bytes are received from a slave transmitter (see Figure 76). The transfer is initialized as in the master transmitter mode. When the START condition has been transmitted, the interrupt routine must load SSDAT with the 7-bit slave address and the data direction bit (SLA+R). The serial interrupt flag (SSI) must then be cleared before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgment bit has been received, the serial interrupt flag is set again and a number of status code in SSSTA are possible. There are 40h, 48h or 38h for the master mode and also 68h, 78h or B0h if the slave mode was enabled (SSAA = logic 1). The appropriate action to be taken for each of these status code is detailed in Table 78. This scheme is repeated until a STOP condition is transmitted.

SSPE and SSCR2:0 are not affected by the serial transfer and are not referred to in Table 78. After a repeated START condition (state 10h) the controller may switch to the master transmitter mode by loading SSDAT with SLA+W.

Slave Receiver Mode

In the slave receiver mode, a number of data bytes are received from a master transmitter (see Figure 77). To initiate the slave receiver mode, SSADR and SSCR0 must be loaded as follows:



The upper 7 bits are the addresses to which the controller will respond when addressed by a master. If the LSB (SSGC) is set the controller will respond to the general call address (00h); otherwise it ignores the general call address.

SSCR2	SSPE	SSSTA	SSSTO	SSI	SSAA	SSCR1	SSCR0
X	1	0	0	0	1	X	X

SSCR2:0 have no effect in the slave mode. SSPE must be set to enable the controller. The SSAA bit must be set to enable the own slave address or the general call address acknowledgment. SSSTA, SSSTO and SSI must be cleared.

When SSADR and SSCR0 have been initialized, the controller waits until it is addressed by its own slave address followed by the data direction bit which must be logic 0 (W) for operating in the slave receiver mode. After its own slave address and the W bit have been received, the serial interrupt flag is set and a valid status code can be read from SSSTA. This status code is used to vector to an interrupt service routine, and the appropriate action to be taken for each of these status code is detailed in Table 78 and Table 122. The slave receiver mode may also be entered if arbitration is lost while the controller is in the master mode (see states 68h and 78h).

If the SSAA bit is reset during a transfer, the controller will return a not acknowledge (logic 1) to SDA after the next received data byte. While SSAA is reset, the controller does not respond to its own slave address. However, the two-wire bus is still monitored and address recognition may be resumed at any time by setting SSAA. This means that the SSAA bit may be used to temporarily isolate the controller from the two-wire bus.

Slave Transmitter Mode

In the slave transmitter mode, a number of data bytes are transmitted to a master receiver (see Figure 78). Data transfer is initialized as in the slave receiver mode. When SSADR and SSSCON have been initialized, the controller waits until it is addressed by its own slave address followed by the data direction bit which must be logic 1 (R) for operating in the slave transmitter mode. After its own slave address and the R bit have been received, the serial interrupt flag is set and a valid status code can be read from SSSTA. This status code is used to vector to an interrupt service routine, and the appropriate action to be taken for each of these status code is detailed in Table 123. The slave transmitter mode may also be entered if arbitration is lost while the controller is in the master mode (see state B0h).

If the SSAA bit is reset during a transfer, the controller will transmit the last byte of the transfer and enter state C0h or C8h. The controller is switched to the not addressed slave mode and will ignore the master receiver if it continues the transfer. Thus the master receiver receives all 1's as serial data. While SSAA is reset, the controller does not respond to its own slave address. However, the two-wire bus is still monitored and address recognition may be resumed at any time by setting SSAA. This means that the SSAA bit may be used to temporarily isolate the controller from the two-wire bus.

Miscellaneous States

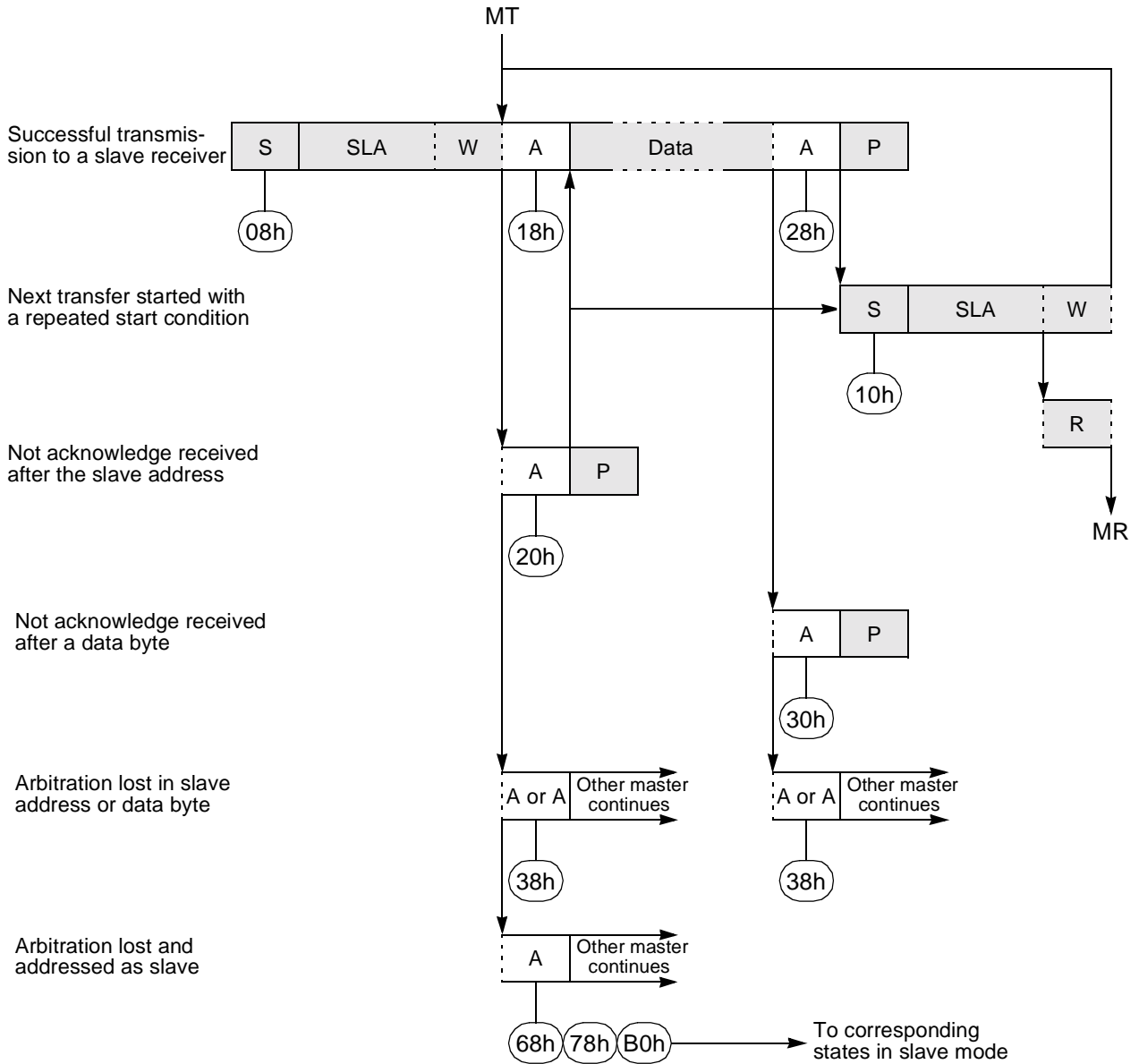
There are two SSSTA codes that do not correspond to a define two-wire hardware state (see Table 78). These are discussed hereafter.



Status F8h indicates that no relevant information is available because the serial interrupt flag is not yet set. This occurs between other states and when the controller is not involved in a serial transfer.

Status 00h indicates that a bus error has occurred during a serial transfer. A bus error is caused when a START or a STOP condition occurs at an illegal position in the format frame. Examples of such illegal positions are during the serial transfer of an address byte, a data byte, or an acknowledge bit. When a bus error occurs, SSI is set. To recover from a bus error, the SSSTO flag must be set and SSI must be cleared. This causes the controller to enter the not addressed slave mode and to clear the SSSTO flag (no other bits in S1CON are affected). The SDA and SCL lines are released and no STOP condition is transmitted.

Note: The two-wire controller interfaces to the external two-wire bus via two port 1 pins: P1.6/SCL (serial clock line) and P1.7/SDA (serial data line). To avoid low level asserting and conflict on these lines when the two-wire controller is enabled, the output latches of P1.6 and P1.7 must be set to logic 1.

Figure 75. Format and States in the Master Transmitter Mode



 From master to slave
 From slave to master



 Any number of data bytes and their associated acknowledge bits
 This number (contained in SSSTA) corresponds to a defined state of the two-wire bus

Figure 76. Format and States in the Master Receiver Mode

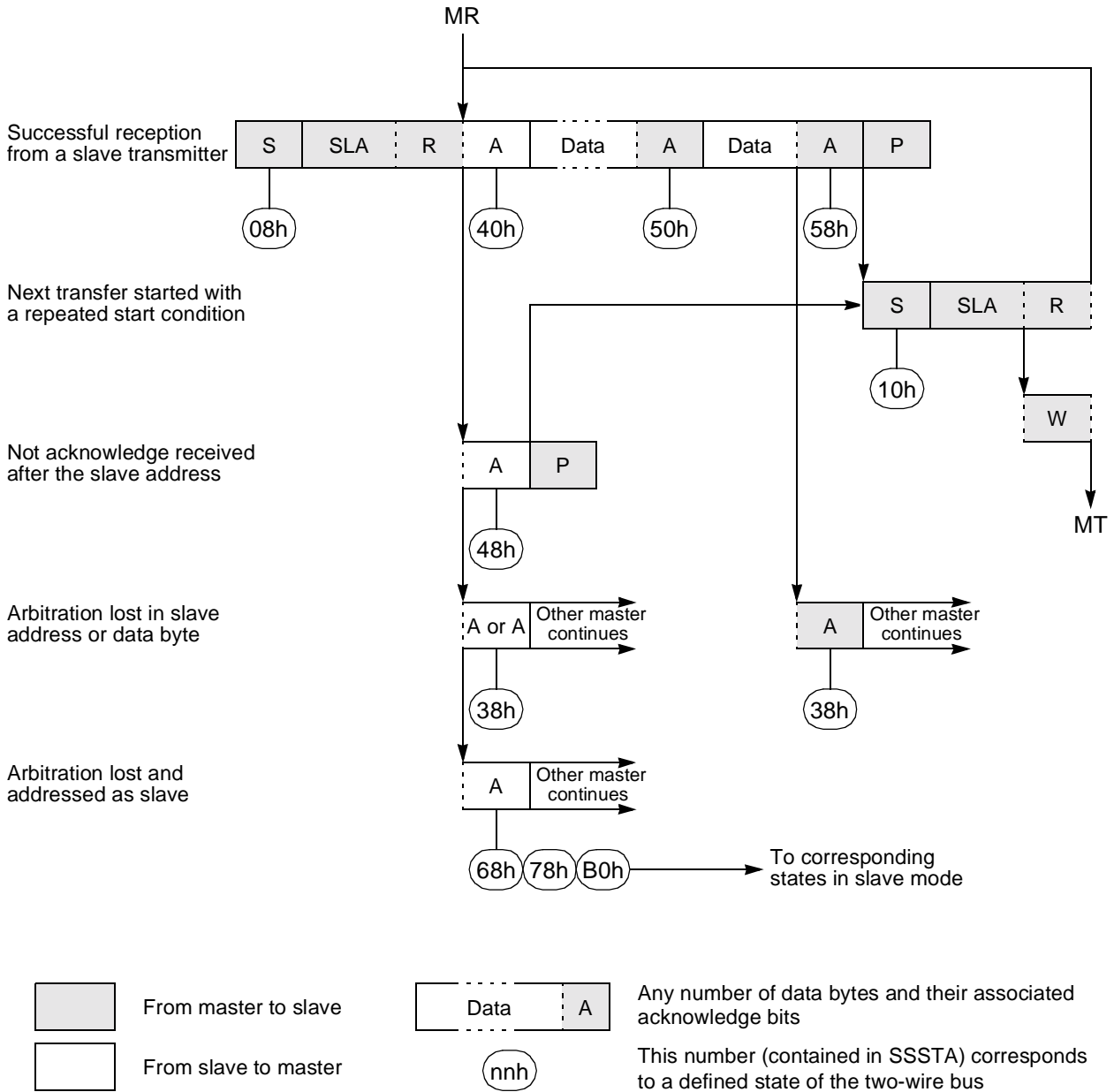


Figure 77. Format and States in the Slave Receiver Mode

Reception of the own slave address and one or more data bytes. All are acknowledged

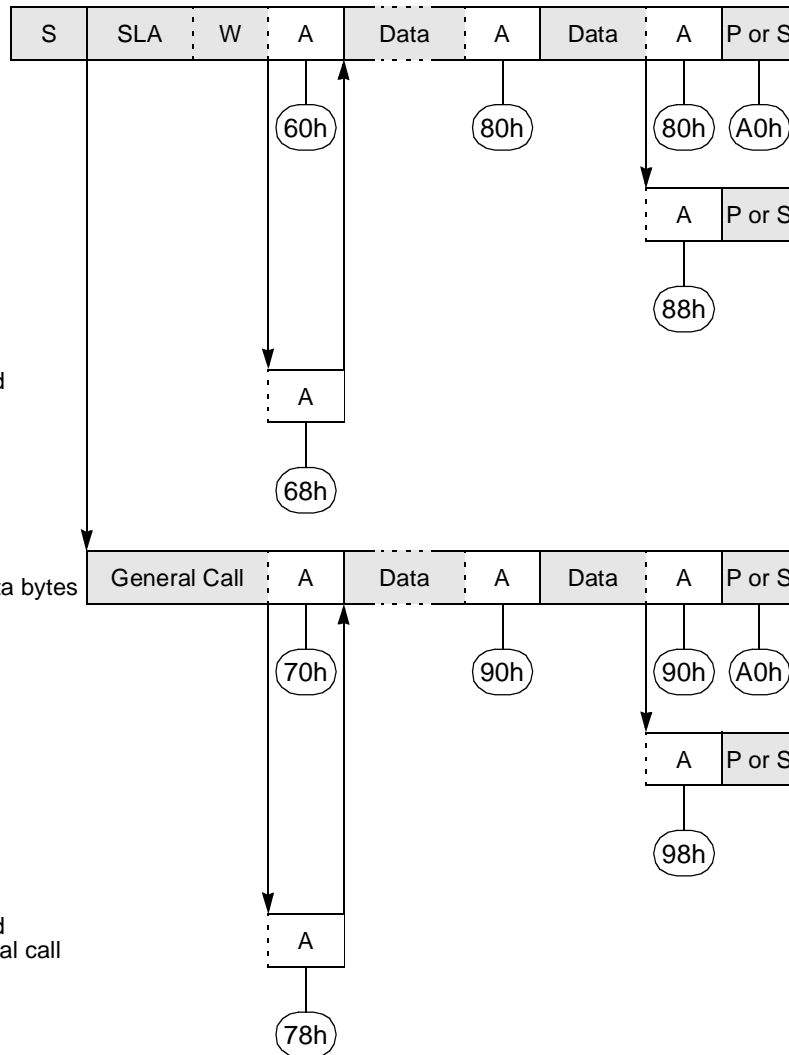
Last data byte received is not acknowledged



Arbitration lost as master and addressed as slave

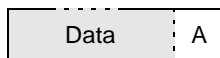

Reception of the general call address and one or more data bytes

Last data byte received is not acknowledged

Arbitration lost as master and addressed as slave by general call



 From master to slave
 From slave to master

 Data A
 (nnh)

Any number of data bytes and their associated acknowledge bits

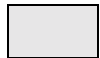
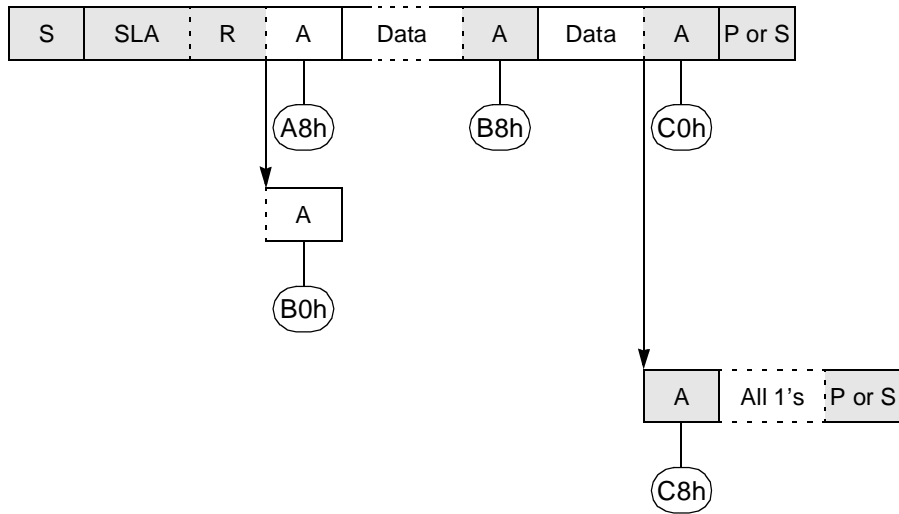
This number (contained in SSSTA) corresponds to a defined state of the two-wire bus

Figure 78. Format and States in the Slave Transmitter Mode

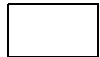
Reception of the own slave address and transmission of one or more data bytes.

Arbitration lost as master and addressed as slave

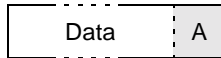
Last data byte transmitted. Switched to not addressed slave (SSAA = 0).



From master to slave



From slave to master



Any number of data bytes and their associated acknowledge bits

This number (contained in SSSTA) corresponds to a defined state of the two-wire bus

Table 119. Status for Master Transmitter Mode

Status Code SSSTA	Status of the Two-wire Bus and Two-wire Hardware	Application software response					Next Action Taken by Two-wire Hardware
		To/From SSDAT	To SSSCON				
			SSSTA	SSSTO	SSI	SSAA	
08h	A START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted.
10h	A repeated START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted.
		Write SLA+R	X	0	0	X	SLA+R will be transmitted. Logic will switch to master receiver mode
18h	SLA+W has been transmitted; ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
20h	SLA+W has been transmitted; NOT ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
28h	Data byte has been transmitted; ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
30h	Data byte has been transmitted; NOT ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
38h	Arbitration lost in SLA+W or data bytes	No SSDAT action	0	0	0	X	Two-wire bus will be released and not addressed slave mode will be entered.
		No SSDAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free.

Table 120. Status for Master Receiver Mode

Status Code SSSTA	Status of the Two-wire Bus and Two-wire Hardware	Application software response					Next Action Taken by Two-wire Hardware
		To/From SSDAT	To SSCON				
			SSSTA	SSSTO	SSI	SSAA	
08h	A START condition has been transmitted	Write SLA+R	X	0	0	X	SLA+R will be transmitted.
10h	A repeated START condition has been transmitted	Write SLA+R	X	0	0	X	SLA+R will be transmitted.
		Write SLA+W	X	0	0	X	SLA+W will be transmitted. Logic will switch to master transmitter mode.
38h	Arbitration lost in SLA+R or NOT ACK bit	No SSDAT action	0	0	0	X	Two-wire bus will be released and not addressed slave mode will be entered.
		No SSDAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free.
40h	SLA+R has been transmitted; ACK has been received	No SSDAT action	0	0	0	0	Data byte will be received and NOT ACK will be returned.
		No SSDAT action	0	0	0	1	Data byte will be received and ACK will be returned.
48h	SLA+R has been transmitted; NOT ACK has been received	No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
50h	Data byte has been received; ACK has been returned	Read data byte	0	0	0	0	Data byte will be received and NOT ACK will be returned.
		Read data byte	0	0	0	1	Data byte will be received and ACK will be returned.
58h	Data byte has been received; NOT ACK has been returned	Read data byte	1	0	0	X	Repeated START will be transmitted.
		Read data byte	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		Read data byte	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.

Table 121. Status for Slave Receiver Mode with Own Slave Address

Status Code SSSTA	Status of the Two-wire Bus and Two-wire Hardware	Application software response					Next Action Taken by Two-wire Hardware
		To/From SSDAT	To SSCON				
			SSSTA	SSSTO	SSI	SSAA	
60h	Own SLA+W has been received; ACK has been returned	No SSDAT action	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned.
68h	Arbitration lost in SLA+R/W as master; own SLA+W has been received; ACK has been returned	No SSDAT action	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned.
80h	Previously addressed with own SLA+W; data has been received; ACK has been returned	Read data byte	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.
88h	Previously addressed with own SLA+W; data has been received; NOT ACK has been returned	Read data byte	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA.
		Read data byte	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if SSGC = logic 1.
		Read data byte	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if SSGC = logic 1. A START condition will be transmitted when the bus becomes free.
A0h	A STOP condition or repeated START condition has been received while still addressed as slave	No SSDAT action	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA.
		No SSDAT action	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if SSGC = logic 1.
		No SSDAT action	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free.
		No SSDAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if SSGC = logic 1. A START condition will be transmitted when the bus becomes free.

Table 122. Status for Slave Receiver Mode with General Call Address

Status Code SSSTA	Status of the Two-wire Bus and Two-wire Hardware	Application software response					Next Action Taken by Two-wire Hardware
		To/From SSDAT	To SSCON				
			SSSTA	SSSTO	SSI	SSAA	
70h	General call address has been received; ACK has been returned	No SSDAT action	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned.
78h	Arbitration lost in SLA+R/W as master; general call address has been received; ACK has been returned	No SSDAT action	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No SSDAT action	X	0	0	1	Data byte will be received and ACK will be returned.
90h	Previously addressed with general call; data has been received; ACK has been returned	Read data byte	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.
98h	Previously addressed with general call; data has been received; NOT ACK has been returned	Read data byte	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA.
		Read data byte	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if SSGC = logic 1.
		Read data byte	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if SSGC = logic 1. A START condition will be transmitted when the bus becomes free.
A0h	A STOP condition or repeated START condition has been received while still addressed as slave	No SSDAT action	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA.
		No SSDAT action	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if SSGC = logic 1.
		No SSDAT action	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free.
		No SSDAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if SSGC = logic 1. A START condition will be transmitted when the bus becomes free.

Table 123. Status for Slave Transmitter Mode

Status Code SSSTA	Status of the Two-wire Bus and Two-wire Hardware	Application software response					Next Action Taken by Two-wire Hardware
		To/From SSDAT	To SSCON				
			SSSTA	SSSTO	SSI	SSAA	
A8h	Own SLA+R has been received; ACK has been returned	Write data byte	X	0	0	0	Last data byte will be transmitted.
		Write data byte	X	0	0	1	Data byte will be transmitted.
B0h	Arbitration lost in SLA+R/W as master; own SLA+R has been received; ACK has been returned	Write data byte	X	0	0	0	Last data byte will be transmitted.
		Write data byte	X	0	0	1	Data byte will be transmitted.
B8h	Data byte in SSDAT has been transmitted; ACK has been received	Write data byte	X	0	0	0	Last data byte will be transmitted.
		Write data byte	X	0	0	1	Data byte will be transmitted.
C0h	Data byte in SSDAT has been transmitted; NOT ACK has been received	No SSDAT action	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA.
		No SSDAT action	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if SSGC = logic 1.
		No SSDAT action	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free.
		No SSDAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if SSGC = logic 1. A START condition will be transmitted when the bus becomes free.
C8h	Last data byte in SSDAT has been transmitted (SSAA= 0); ACK has been received	No SSDAT action	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA.
		No SSDAT action	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if SSGC = logic 1.
		No SSDAT action	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free.
		No SSDAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognized; GCA will be recognized if SSGC = logic 1. A START condition will be transmitted when the bus becomes free.

Table 124. Status for Miscellaneous States

Status Code SSSTA	Status of the Two-wire Bus and Two-wire Hardware	Application software response					Next Action Taken by Two-wire Hardware
		To/From SSDAT	To SSCON				
			SSSTA	SSSTO	SSI	SSAA	
F8h	No relevant state information available; SSI = 0	No SSDAT action	No SSCON action				Wait or proceed current transfer.
00h	Bus error due to an illegal START or STOP condition	No SSDAT action	0	1	0	X	Only the internal hardware is affected, no STOP condition is sent on the bus. In all cases, the bus is released and SSSTO is reset.

Registers

Table 125. SSCR2 Register
SSCON (S:93h) – Synchronous Serial Control Register

7	6	5	4	3	2	1	0
SSCR2	SSPE	SSSTA	SSSTO	SSI	SSAA	SSCR1	SSCR0
Bit Number	Bit Mnemonic	Description					
7	SSCR2	Synchronous Serial Control Rate Bit 2 Refer to Table for rate description.					
6	SSPE	Synchronous Serial Peripheral Enable Bit Set to enable the controller. Clear to disable the controller.					
5	SSSTA	Synchronous Serial Start Flag Set to send a START condition on the bus. Clear not to send a START condition on the bus.					
4	SSSTO	Synchronous Serial Stop Flag Set to send a STOP condition on the bus. Clear not to send a STOP condition on the bus.					
3	SSI	Synchronous Serial Interrupt Flag Set by hardware when a serial interrupt is requested. Must be cleared by software to acknowledge interrupt.					
2	SSAA	Synchronous Serial Assert Acknowledge Flag Set to enable slave modes. Slave modes are entered when SLA or GCA (if SSGC set) is recognized. Clear to disable slave modes. <u>Master Receiver Mode in progress</u> Clear to force a not acknowledge (high level on SDA). Set to force an acknowledge (low level on SDA). <u>Master Transmitter Mode in progress</u> This bit has no specific effect when in master transmitter mode. <u>Slave Receiver Mode in progress</u> Clear to force a not acknowledge (high level on SDA). Set to force an acknowledge (low level on SDA). <u>Slave Transmitter Mode in progress</u> Clear to isolate slave from the bus after last data byte transmission. Set to enable slave mode.					
1	SSCR1	Synchronous Serial Control Rate Bit 1 Refer to Table for rate description.					
0	SSCR0	Synchronous Serial Control Rate Bit 0 Refer to Table for rate description.					

Reset Value = 0000 0000b

Table 126. SSSTA Register

SSSTA (S:94h) – Synchronous Serial Status Register

7	6	5	4	3	2	1	0
SSC4	SSC3	SSC2	SSC1	SSC0	0	0	0

Bit Number	Bit Mnemonic	Description
7:3	SSC4:0	Synchronous Serial Status Code Bits 0 to 4 Refer to Table 119 to Table 78 for status description.
2:0	0	Always 0.

Reset Value = F8h

Table 127. SSDAT Register

SSDAT (S:95h) – Synchronous Serial Data Register

7	6	5	4	3	2	1	0
SSD7	SSD6	SSD5	SSD4	SSD3	SSD2	SSD1	SSD0

Bit Number	Bit Mnemonic	Description
7:1	SSD7:1	Synchronous Serial Address bits 7 to 1 or Synchronous Serial Data Bits 7 to 1
0	SSD0	Synchronous Serial Address bit 0 (R/W) or Synchronous Serial Data Bit 0

Reset Value = 1111 1111b

Table 128. SSADR Register

SSADR (S:96h) – Synchronous Serial Address Register

7	6	5	4	3	2	1	0
SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSGC

Bit Number	Bit Mnemonic	Description
7:1	SSA7:1	Synchronous Serial Slave Address Bits 7 to 1.
0	SSGC	Synchronous Serial General Call Bit Set to enable the general call address recognition. Clear to disable the general call address recognition.

Reset Value = 1111 1110b



Analog to Digital Converter

The AT8xC51SND1A implements a 2-channel 10-bit (8 true bits) analog to digital converter (ADC). First channel of this ADC can be used for battery monitoring while the second one can be used for voice sampling at 8 kHz.

Description

The A/D converter interfaces with the C51 core through four special function registers: ADCON, the ADC control register (see Table 130); ADDH and ADDL, the ADC data registers (see Table 132 and Table 133); and ADCLK, the ADC clock register (see Table 131).

As shown in Figure 79, the ADC is composed of a 10-bit cascaded potentiometric digital to analog converter, connected to the negative input of a comparator. The output voltage of this DAC is compared to the analog voltage stored in the Sample and Hold and coming from AIN0 or AIN1 input depending on the channel selected (see Table 129).

Figure 79. ADC Structure

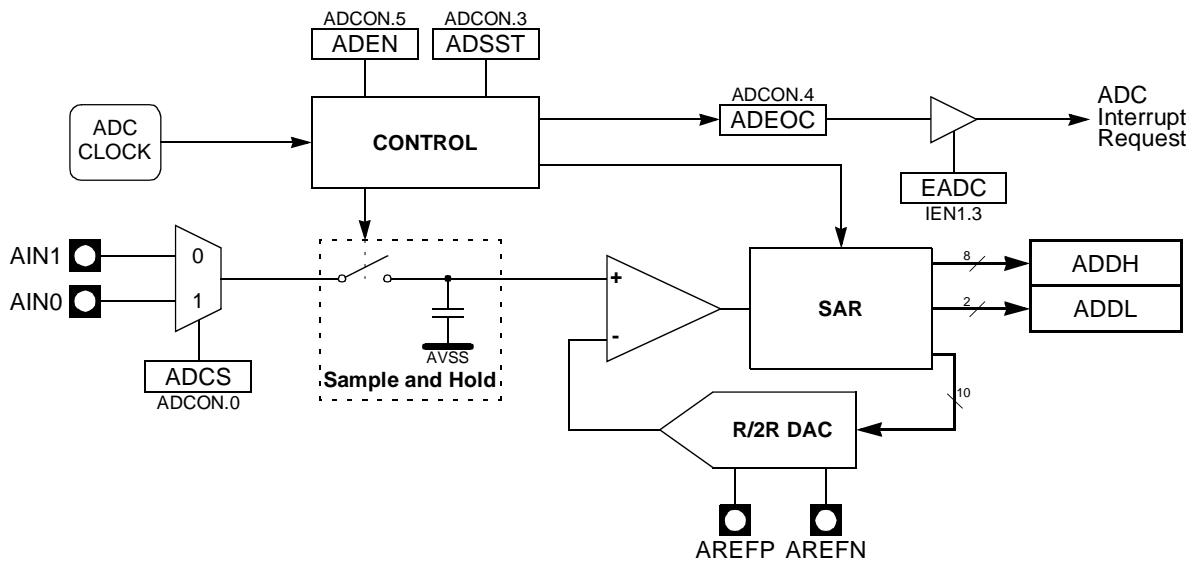
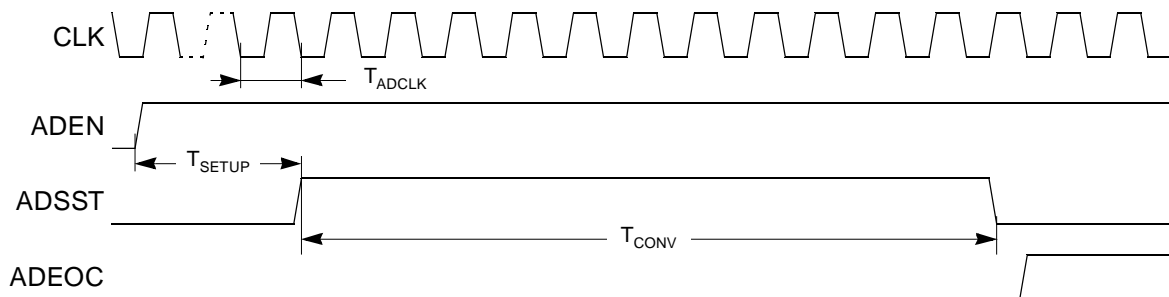


Figure 80 shows the timing diagram of a complete conversion. For simplicity, the figure depicts the waveforms in idealized form and do not provide precise timing information. For ADC characteristics and timing parameters refer to the Section “AC Characteristics” of the AT8xC51SND1A datasheet.

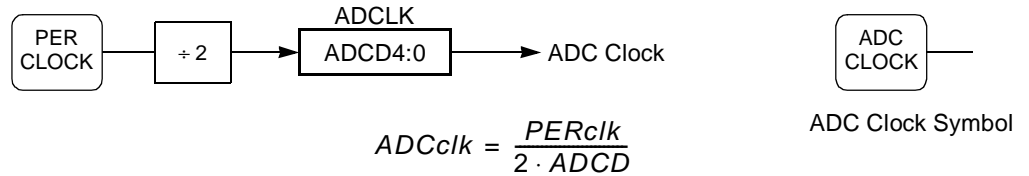
Figure 80. Timing Diagram



Clock Generation

The ADC clock is generated by division of the peripheral clock (see details in Section "X2 Feature", page 4). The division factor is then given by ADPC4:0 bits in ADCLK register. Figure 39 shows the ADC clock generator and its calculation formula⁽¹⁾.

Figure 39. ADC Clock Generator and Symbol Caution:



Note: In all cases, the ADC clock frequency may be higher than the maximum F_{ADCLK} parameter reported in the Section "AC Characteristics" of the AT8xC51SND1A datasheet.

Channel Selection

The channel on which conversion is performed is selected by the ADCS bit in ADCON register according to Table 129.

Table 129. ADC Channel Selection

ADCS	Channel
0	AIN1
1	AIN0

Conversion Precision

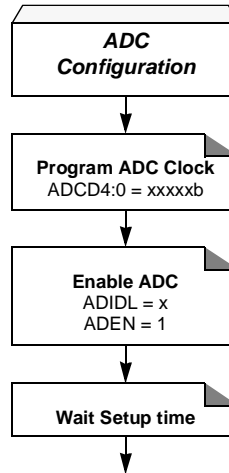
The 10-bit precision conversion is achieved by stopping the CPU core activity during conversion for limiting the digital noise induced by the core. This mode called the Pseudo-Idle mode^{(1), (2)} is enabled by setting the ADIDL bit in ADCON register. Thus, when conversion is launched (see Section "Conversion Launching", page 154), the CPU core is stopped until the end of the conversion (see Section "End Of Conversion", page 154). This bit is cleared by hardware at the end of the conversion.

- Notes:
1. Only the CPU activity is frozen, peripherals are not affected by the Pseudo-Idle mode.
 2. If some interrupts occur during the Pseudo-Idle mode, they will be delayed and processed, according to their priority after the end of the conversion.

Configuration

The ADC configuration consists in programming the ADC clock as detailed in the Section "Clock Generation", page 153. The ADC is enabled using the ADEN bit in ADCON register. As shown in Figure 93, user must wait the setup time (T_{SETUP}) before launching any conversion.

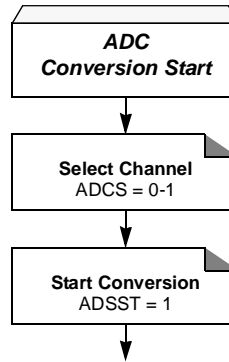
Figure 40. ADC Configuration Flow



Conversion Launching

The conversion is launched by setting the ADSST bit in ADCON register, this bit remains set during the conversion. As soon as the conversion is started, it takes 11 clock periods (T_{CONV}) before the data is available in ADDH and ADDL registers.

Figure 41. ADC Conversion Launching Flow



End Of Conversion

The end of conversion is signalled to you by the ADEOC flag in ADCON register becoming set or by the ADSST bit in ADCON register becoming cleared. ADEOC flag can generate an interrupt if enabled by setting EADC bit in IEN1 register. This flag is set by hardware and must be reset by software.

Registers

Table 130. ADCON Register

ADCON (S:F3h) – ADC Control Register

	7	6	5	4	3	2	1	0
	-	ADIDL	ADEN	ADEOC	ADSST	-	-	ADCS

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is always 0. Do not set this bit.
6	ADIDL	ADC Pseudo-Idle Mode Set to suspend the CPU core activity (pseudo-idle mode) during conversion. Clear by hardware at the end of conversion.
5	ADEN	ADC Enable Bit Set to enable the A to D converter. Clear to disable the A to D converter and put it in low power stand-by mode.
4	ADEOC	End Of Conversion Flag Set by hardware when ADC result is ready to be read. This flag can generate an interrupt. Must be cleared by software.
3	ADSST	Start and Status Bit Set to start an A to D conversion on the selected channel. Cleared by hardware at the end of conversion.
2-1	-	Reserved The value read from these bits is always 0. Do not set these bits.
0	ADCS	Channel Selection Bit Set to select channel 0 for conversion. Clear to select channel 1 for conversion.

Reset Value = 0000 0000b

Table 131. ADCLK Register

ADCLK (S:F2h) – ADC Clock Divider Register

	7	6	5	4	3	2	1	0
	-	-	-	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0

Bit Number	Bit Mnemonic	Description
7-5	-	Reserved The value read from these bits is always 0. Do not set these bits.
4-0	ADCD4:0	ADC Clock Divider 5-bit divider for ADC clock generation.

Table 132. ADDH Register

ADDH (S:F5h Read Only) – ADC Data High Byte Register

7	6	5	4	3	2	1	0
ADAT9	ADAT8	ADAT7	ADAT6	ADAT5	ADAT4	ADAT3	ADAT2
Bit Number	Bit Mnemonic	Description					
7 - 0	ADAT9:2	ADC Data Eight Most Significant Bits of the 10-bit ADC data.					

Reset Value = 0000 0000b

Table 133. ADDL Register

ADDL (S:F4h Read Only) – ADC Data Low Byte Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	ADAT1	ADAT0
Bit Number	Bit Mnemonic	Description					
7-2	-	Reserved The value read from these bits is always 0. Do not set these bits.					
1-0	ADAT1:0	ADC Data Two Least Significant Bits of the 10-bit ADC data.					

Reset Value = 0000 0000b

Keyboard Interface

The AT8xC51SND1A implements a keyboard interface allowing the connection of a 4 x n matrix keyboard. It is based on 4 inputs with programmable interrupt capability on both high or low level. These inputs are available as alternate function of P1.3:0 and allow exit from idle and power down modes.

Description

The keyboard interface interfaces with the C51 core through two special function registers: KBCON, the keyboard control register (see Table 134); and KBSTA, the keyboard control and status register (see Table 135).

The keyboard inputs are considered as 4 independent interrupt sources sharing the same interrupt vector. An interrupt enable bit (EKB in IEN1 register) allows global enable or disable of the keyboard interrupt (see Figure 42). As detailed in Figure 43 each keyboard input has the capability to detect a programmable level according to KINL3:0 bit value in KBCON register. Level detection is then reported in interrupt flags KINF3:0 in KBSTA register.

A keyboard interrupt is requested each time one of the four flags is set, i.e. the input level matches the programmed one. Each of these four flags can be masked by software using KINM3:0 bits in KBCON register and is cleared by reading KBSTA register. This structure allows keyboard arrangement from 1 by n to 4 by n matrix and allow usage of KIN inputs for any other purposes.

Figure 42. Keyboard Interface Block Diagram

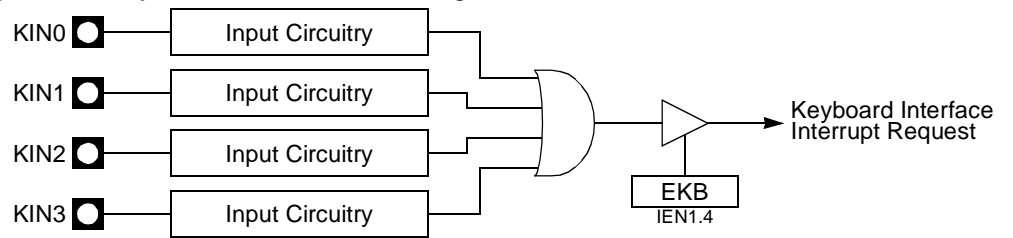
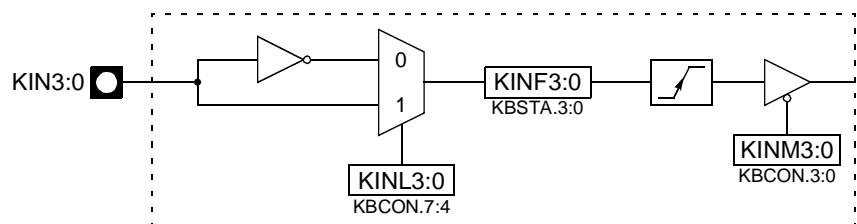


Figure 43. Keyboard Input Circuitry



Power Reduction Mode

KIN3:0 inputs allow exit from idle and power down modes as detailed in Section “Power Management”, page 41. To enable this feature, KPDE bit in KBSTA register must be set to logic 1.

Due to the asynchronous keypad detection in power down mode (all clocks are stopped), exit may happen on parasitic key press. In this case, no key is detected and software must enter power down again.

Registers

Table 134. KBCON Register

KBCON (S:A3h) – Keyboard Control Register

7	6	5	4	3	2	1	0
KINL3	KINL2	KINL1	KINL0	KINM3	KINM2	KINM1	KINM0
Bit Number	Bit Mnemonic	Description					
7-4	KINL3:0	Keyboard Input Level Bit Set to enable a high level detection on the respective KIN3:0 input. Clear to enable a low level detection on the respective KIN3:0 input.					
3-0	KINM3:0	Keyboard Input Mask Bit Set to prevent the respective KINF3:0 flag from generating a keyboard interrupt. Clear to allow the respective KINF3:0 flag to generate a keyboard interrupt.					

Reset Value = 0000 1111b

Table 135. KBSTA Register

KBSTA (S:A4h) – Keyboard Control and Status Register

7	6	5	4	3	2	1	0
KPDE	-	-	-	KINF3	KINF2	KINF1	KINF0
Bit Number	Bit Mnemonic	Description					
7	KPDE	Keyboard Power Down Enable Bit Set to enable exit of power down mode by the keyboard interrupt. Clear to disable exit of power down mode by the keyboard interrupt.					
6-4	-	Reserved The value read from these bits is always 0. Do not set these bits.					
3-0	KINF3:0	Keyboard Input Interrupt Flag Set by hardware when the respective KIN3:0 input detects a programmed level. Cleared when reading KBSTA.					

Reset Value = 0000 0000b

Table of Contents

Features	1
Description.....	1
Typical Applications	2
Block Diagram	3
Clock Controller	4
Oscillator	4
X2 Feature	4
PLL.....	5
Registers.....	7
Program/Code Memory.....	10
ROM Memory Architecture	10
Flash Memory Architecture	11
Hardware Security System	12
Boot Memory Execution.....	12
Registers.....	14
Hardware Bytes	15
Data Memory.....	17
Internal Space.....	17
External Space.....	19
Dual Data Pointer.....	21
Registers.....	22
Special Function Registers	24
Interrupt System.....	31
Interrupt System Priorities.....	31
External Interrupts.....	34
Registers.....	35
Power Management.....	41
Reset.....	41
Reset Recommendation to Prevent Flash Corruption	41
Idle Mode	42
Power-down Mode	42
Registers.....	44

Timers/Counters	45
Timer/Counter Operations	45
Timer Clock Controller	45
Timer 0	46
Timer 1	48
Interrupt	49
Registers	50
Watchdog Timer.....	53
Description.....	53
Watchdog Clock Controller.....	53
Watchdog Operation.....	54
Registers	55
MP3 Decoder	56
Decoder	56
Audio Controls.....	58
Decoding Errors.....	59
Frame Information	59
Ancillary Data	59
Interrupt	60
Registers	62
Audio Output Interface.....	67
Description.....	67
Clock Generator	68
Data Converter	68
Audio Buffer.....	69
MP3 Buffer.....	70
Interrupt Request.....	70
MP3 Song Playing.....	70
Voice or Sound Playing	71
Registers	72
Universal Serial Bus	74
Description.....	75
USB Interrupt System.....	77
Registers	79
MultiMediaCard Controller.....	88
Card Concept	88
Bus Concept.....	88
Description.....	93
Clock Generator	93
Command Line Controller.....	95
Data Line Controller.....	97

Interrupt.....	103
Registers.....	104
IDE/ATAPI Interface.....	110
Description.....	110
Registers.....	112
Serial I/O Port.....	113
Mode Selection.....	113
Baud Rate Generator.....	113
Synchronous Mode (Mode 0).....	114
Asynchronous Modes (Modes 1, 2 and 3).....	116
Multiprocessor Communication (Modes 2 and 3).....	119
Automatic Address Recognition.....	119
Interrupt.....	121
Registers.....	122
Synchronous Peripheral Interface.....	125
Description.....	126
Interrupt.....	129
Configuration.....	130
Registers.....	134
Two-wire Controller.....	136
Description.....	136
Registers.....	150
Analog to Digital Converter.....	152
Description.....	152
Registers.....	155
Keyboard Interface.....	157
Description.....	157
Registers.....	158



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