To all our customers

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Renesas Technology Corp.
April 1, 2003

RENESAS

Renesas Technology Corp.

HD66724/HD66725

(Graphics LCD Controller/Driver
with Key Scan Function)

HITACHI

ADE-207-309(Z)
Rev 1.2
'99.8

Description

The HD66724/HD66725, dot-matrix graphics LCD controller and driver LSI incorporating a key scan function up to a 4-by-8 key matrix, display characters such as alphanumerics, katakana, hiragana and symbols as well as graphics such as kanji and pictograms. They can be configured to drive a dot-matrix liquid crystal display and control key scan functions under the control of the microprocessor connected via the clock-synchronized serial or 4/8-bit bus. The HD66724 is capable of displaying up to three 12-character lines, 72-by-24 dot graphics and 144 segments. The HD66725 is capable of displaying up to three 16-character lines, 96-by-24 dot graphics and 192 segments. Of the 144 (192) segments displayed, 48 (64) segments can be grayscaled. The HD66724/HD66725 have a smooth horizontal/vertical scroll display and double-height display so that the user can easily see a variety of information within a small LCM.

The HD66724/HD66725 have various functions to reduce the power consumption of an LCD system such as low-voltage operation of 1.8 V or less, a booster to generate maximum triple LCD drive voltage from the supplied voltage, and voltage-followers to decrease the direct current flow in the LCD drive bleeder-resistors. Combining these hardware functions with software functions such as standby and sleep modes allows fine power control. The HD66724/HD66725 are suitable for any portable battery-driven product requiring long-term driving capabilities and small physical dimensions such as cellular phones, pagers, portable audio devices, or electronic wallets.

Features

- Control and drive of a character and graphics LCD with built-in key scan functions
- Three 12- (16-) character lines, 72 (96) -by-24 dot graphics, and 144 (192) segments
- 48 (64) grayscale segments
- Control up to a 4×8 (32 key) matrix key scan.
- 3 general ports built-in
- Low-power operation support:

  - — Vcc = 1.8 to 5.5 V (low voltage)
  - — V_{LCD} = 3.0 to 6.5 V (liquid crystal drive voltage)
  - — Single, double or triple booster for liquid crystal drive voltage
  - — Contrast adjuster and voltage followers to decrease direct current flow in the LCD drive bleeder-resistors
  - — Wake-up feature using key scan interrupt
  - — Programmable drive duty ratios and bias values displayed on LCD
- Clock-synchronized serial interface
- 4-/8-bit bus interface capability (except when key scan circuit is used)
- 80 × 8-bit display data RAM (80 characters max)
- 20,736-bit (6 × 8 dots : 432 characters) character generator ROM
- 384 × 8-bit (64 characters) character generator RAM
- 96 × 2-bit (192 segment-icons and marks max) segment RAM
- 72- (96-) segment × 26-common-signal liquid crystal display driver
- Programmable display sizes and duty ratios
- Vertical and horizontal smooth scrolls
- Vertical double-height display
- Selectable CGROM memory bank (max. 432 fonts)
- Wide range of instruction functions:
  - — Clear display, display on/off control, icon and mark control, character blink, black-white reversed blinking cursor, return home, cursor on/off, black-white reversed raster-row
- No wait time for instruction execution and RAM access (zero instruction)
- Internal oscillation (with external or built-in resistor) hardware reset
- Shift change of segment and common driver
- Slim chip with bumps for chip-on-glass (COG) mounting, and tape carrier package (TCP)

Table 1 Progammable Display Sizes and Duty Ratios

		Character Display		Graphics Display				
Duty Ratio	**Optimum Drive Bias**	**HD66724**	**HD66725**	**HD66724**	**HD66725**	**Segment Display**	**Scanned Keys**	**General Ports**
1/2	1/2	Unavailable	Unavailable	Unavailable	Unavailable		32 (4 x 8)	3
1/10	1/4	1 line x 12 characters	1 line x 16 characters	72 x 8 dots	96 x 8 dots	HD66724: 144		
1/18	1/5	2 lines x 12 characters	2 lines x 16 characters	72 x 16 dots	96 x 16 dots	HD66725: 192		
1/26	1/6	3 lines x 12 characters	3 lines x 16 characters	72 x 24 dots	96 x 24 dots			

Total Current Consumption Characteristics (Vcc = 3 V, fosc = 32 kHz, TYP Conditions, LCD Drive Power Current Included)

				Total Power Consumption				
				Normal Display Operation				
Character Display Size	Duty Ratio	Optimum Drive Bias	Frame Frequency	Internal Logic	LCD Power	Total*	Sleep Mode	Standby Mode
Segment only	1/2	1/2	80 Hz	(14 µA)	(12 µA)	(26 µA)	(11 µA)	0.1 µA
1-line display	1/10	1/4	80 Hz	(20 µA)	(17 µA)	(54 µA)	(11 µA)	
2-line display	1/18	1/5	74 Hz	(20 µA)	(17 µA)	(54 µA)	(11 µA)	
3-line display	1/26	1/6	77 Hz	(20 µA)	(17 µA)	(54 µA)	(11 µA)	

Note : When duty ratio = 1/2 and a double booster is not used:
the total power consumption = Internal logic current + LCD power current
When duty ratio = 1/10 and a double booster is used:
the total power consumption = Internal logic current + LCD power current x 2

Type Name

Types	External Dimensions	Operation Voltages	Internal Fonts
HD66724RA03TA0L	TCP	1.8 V to 5.5 V	Katakana, alphanumerics, symbols and European fonts
HCD66724RA03BP	Au-bumped chip		
HD66725A03TA0L	TCP		
HCD66725A03BP	Au-bumped chip		

LCD-II Family Comparison

Items	HD66712U	HD66720	HD66705U
Character display sizes	12 characters x 4 lines	8 characters x 2 lines	12 characters x 2 lines
Graphic display sizes	—	—	—
Multiplexing icons	60	42	40
Annunciator	—	—	Static: 10
Key scan control	—	5 x 6	—
LED control ports	—	2	—
General output port	—	—	—
Operating power voltages	2.7 V to 5.5 V	2.7 V to 5.5 V	2.4 V to 5.5 V
Liquid crystal drive voltages	3 V to 13 V	3 V to 11 V	3 V to 9 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	—	4 bits, 8 bits
Expansion driver control	Possible	Possible	Impossible
Liquid crystal drive duty ratios	1/17, 33	1/9, 17	1/10, 18
Liquid crystal drive biases	1/4 to 1/6, 7	1/4 to 1/5	1/4
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Double or triple	Double or triple	Double or triple
Bleeder-resistor for liquid crystal drive	External	External	Incorporated (external)
Liquid crystal drive operational amplifier	—	—	Incorporated
Liquid crystal contrast adjuster	—	—	Incorporated
Horizontal smooth scroll	Dot unit	Dot unit	—
Vertical smooth scroll	—	—	Line unit
Double-height display	—	—	Yes
DDRAM	80 x 8	40 x 8	60 x 8
CGROM	9,600	9,600	9,600
CGRAM	64 x 8	64 x 8	32 x 5
SEGRAM	16 x 8	16 x 8	8 x 5
No. of CGROM fonts	240	240	240
No. of CGRAM fonts	8	8	4
Font sizes	5 x 8	5 x 8	5 x 8
Bit map area	—	—	—
R-C oscillation resistor/oscillation frequency	External resistor (270 kHz)	External resistor (150 kHz)	External resistor (40, 80 kHz)
Reset function	Incorporated, external	Incorporated, external	External
Low power control	LP display mode	LP display mode Simple standby	Partial display off Display off Oscillation off Liquid crystal power off
SEG/COM direction switching	—	—	SEG only
QFP package	(S mask)	QFP-1420	—
TQFP package	—	TQFP-1414	—
TCP package	TCP-128	—	TCP-153
Bare chip	Yes	Yes	Yes
Bumped chip	Yes	—	Yes
No. of pins	128	100	153
Chip sizes	4.95 x 5.27	5.60 x 6.00	9.69 x 2.73
Pad intervals	128 μm	160 μm	120 μm

LCD-II Family Comparison (cont)

Items	HD66717	HD66727	HD66724
Character display sizes	12 characters x 4 lines	12 characters x 4 lines	12 characters x 3 lines
Graphic display sizes	—	—	72 x 26 dots
Multiplexing icons	40	40	144
Annunciator	Static: 10	Static: 12	1/2 duty: 144
Key scan control	—	4 x 8	8 x 4
LED control ports	—	3	—
General output ports	—	3	3
Operating power voltages	2.4 V to 5.5 V	2.4 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	3 V to 13 V	3 V to 13 V	3 V to 6 V
Serial bus	I2C, Clock-synchronized serial	I2C, Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	—	4 bits, 8 bits
Expansion driver control	Impossible	Impossible	Impossible
Liquid crystal drive duty ratios	1/10, 18, 26, 34	1/10, 18, 26, 34	1/2, 10, 18, 26
Liquid crystal drive biases	1/4, 1/6	1/4, 1/6	1/4 to 1/6.5
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Double or triple	Double or triple	Single, double or triple
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated	Incorporated	Incorporated
Horizontal smooth scroll	—	—	3-dot unit
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	60 x 8	60 x 8	80 x 8
CGROM	9,600	11,520	20,736
CGRAM	32 x 5	32 x 6	384 x 8
SEGRAM	8 x 5	8 x 6	72 x 8
No. of CGROM fonts	240	240	240 + 192
No. of CGRAM fonts	4	4	64
Font sizes	5 x 8	5 x 8, 6 x 8	6 x 8
Bit map area	—	—	72 x 26
R-C oscillation resistor/ oscillation frequency	External resistor (40-160 kHz)	External resistor (40-160 kHz)	External resistor, incorporated (32 kHz)
Reset function	External	External	External
Low power control	Partial display off Display off Oscillation off Liquid crystal power off	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt
SEG/COM direction switching	SEG only	SEG, COM	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	TCP-153	TCP-158	TCP-146
Bare chip	Yes	Yes	—
Bumped chip	Yes	Yes	Yes
No. of pins	153	158	146
Chip sizes	10.88 x 2.89	11.39 x 2.89	10.34 x 2.51
Pad intervals	120 μm	120 μm	80 μm

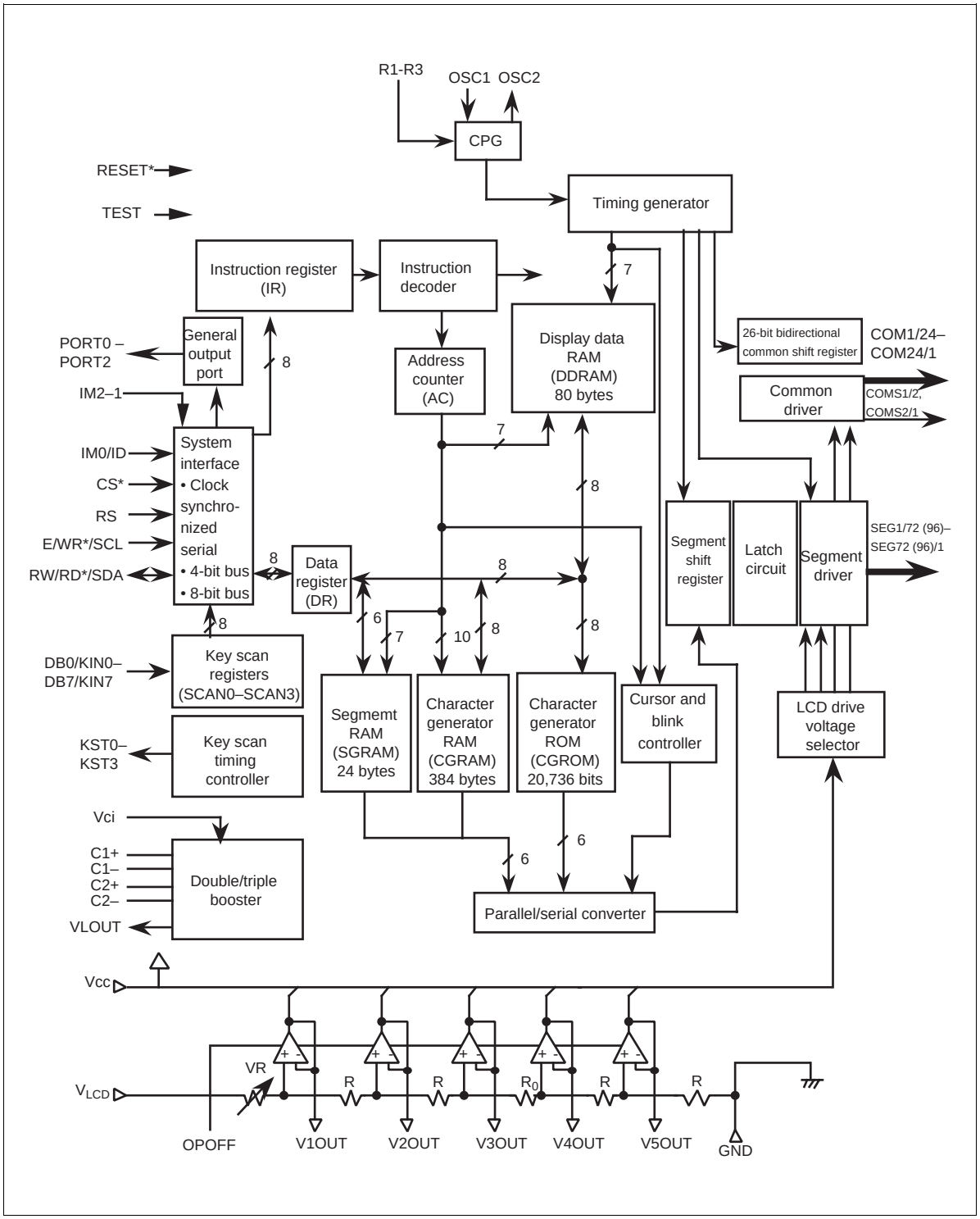
LCD-II Family Comparison (cont)

Items	HD66725	HD66726	HD66730
Character display sizes	16 characters x 3 lines	16 characters x 5 lines	6 (12) characters x 2 lines
Graphic display sizes	96 x 26 dots	96 x 42 dots	—
Multiplexing icons	192	192	71
Annunciator	1/2 duty: 192	1/2 duty: 192	—
Key scan control	8 x 4	8 x 4	—
LED control ports	—	—	—
General output ports	3	3	—
Operating power voltages	1.8 V to 5.5 V	1.8 V to 5.5 V	2.4 V to 5.5 V
Liquid crystal drive voltages	3 V to 6 V	4.0 V to 13 V	3 V to 15 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	8 bits
Expansion driver control	Impossible	Impossible	Possible
Liquid crystal drive duty ratios	1/2, 10, 18, 26	1/2, 10, 18, 26, 34, 42	1/14, 27, 40, 53
Liquid crystal drive biases	1/4 to 1/6.5	1/2 to 1/8	1/4 to 1/8.3
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Single, double, or triple	Single, double, triple, or quadruple	Double or triple
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	External
Liquid crystal drive operational amplifier	Incorporated	Incorporated	—
Liquid crystal contrast adjuster	Incorporated	Incorporated	—
Horizontal smooth scroll	3-dot unit	3-dot unit	Display unit
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	—
DDRAM	80 x 8	80 x 8	80 x 8
CGROM	20,736	20,736	506,880 + 9,216
CGRAM	384 x 8	480 x 8	32 x 6
SEGRAM	96 x 8	96 x 8	8 x 6
No. of CGROM fonts	240 + 192	240 + 192	3,840
No. of CGRAM fonts	64	64	8
Font sizes	6 x 8	6 x 8	11 x 12
Bit map areas	96 x 26	96 x 42	—
R-C oscillation resistor/ oscillation frequency	External resistor, incorporated (32 kHz)	External resistor (50 kHz)	External resistor (70–450 kHz)
Reset function	External	External	External
Low power control	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt	Booster off Internal division function
SEG/COM direction switching	SEG, COM	SEG, COM	—
QFP package	—	—	QFP-1420
TQFP package	—	—	—
TCP package	TCP-170	TCP-188	—
Bare chip	—	—	Yes
Bumped chip	Yes	Yes	—
No. of pins	170	188	128
Chip sizes	10.97 x 2.51	13.13 x 2.51	7.48 x 6.46
Pad intervals	80 μm	80 μm	180 μm

LCD-II Family Comparison (cont)

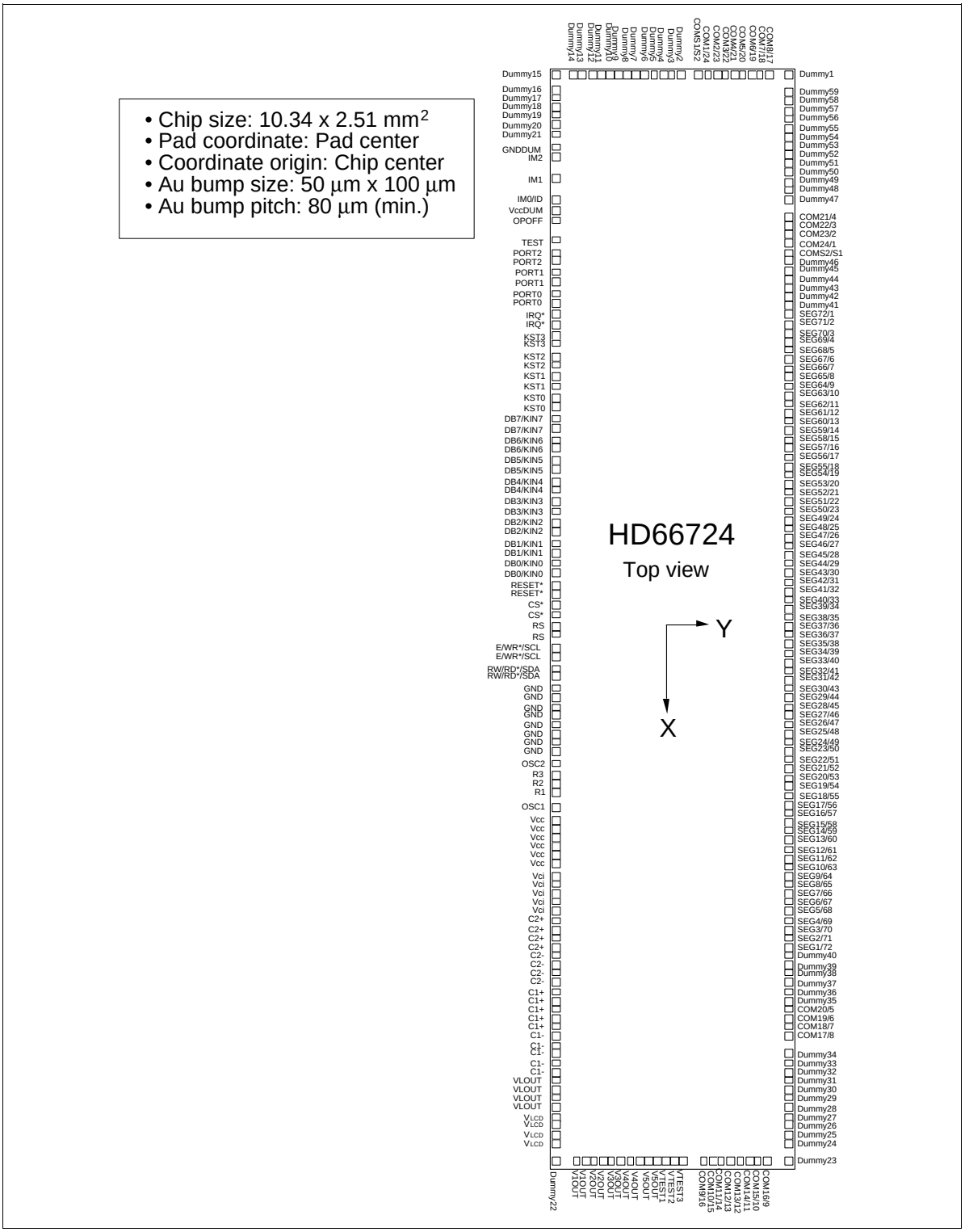
Items	HD66731
Character display sizes	10 (20) characters x 4 lines
Graphic display sizes	—
Multiplexing icons	120
Annunciator	—
Key scan control	—
LED control ports	—
General output ports	—
Operating power voltages	2.4 V to 5.5 V
Liquid crystal drive voltages	3 V to 15 V
Serial bus	Clock-synchronized serial
Parallel bus	8 bits
Expansion driver control	Possible
Liquid crystal drive duty ratios	1/14, 27, 40, 53
Liquid crystal drive biases	1/4 to 1/8.3
Liquid crystal drive waveforms	B
Liquid crystal voltage booster	Double or triple
Bleeder-resistor for liquid crystal drive	External
Liquid crystal drive operational amplifier	—
Liquid crystal contrast adjuster	—
Horizontal smooth scroll	Display unit
Vertical smooth scroll	Line unit
Double-height display	—
DDRAM	80 x 8
CGROM	506,880 + 9,216
CGRAM	32 x 6
SEGRAM	8 x 6
No. of CGROM fonts	3,840
No. of CGRAM fonts	8
Font sizes	11 x 12
Bit map areas	—
R-C oscillation resistor/ oscillation frequency	External resistor (70–450 kHz)
Reset function	External
Low power control	Booster off Internal division function
SEG/COM direction switching	—
QFP package	—
TQFP package	—
TCP package	TCP-170, 206
Bare chip	—
Bumped chip	Yes
No. of pins	206
Chip sizes	7.48 x 6.46
Pad intervals	80 µm

HD66724/HD66725 Block Diagram



HD66724 Pad Arrangement

- Chip size: 10.34 x 2.51 mm^2
- Pad coordinate: Pad center
- Coordinate origin: Chip center
- Au bump size: 50 μm x 100 μm
- Au bump pitch: 80 μm (min.)

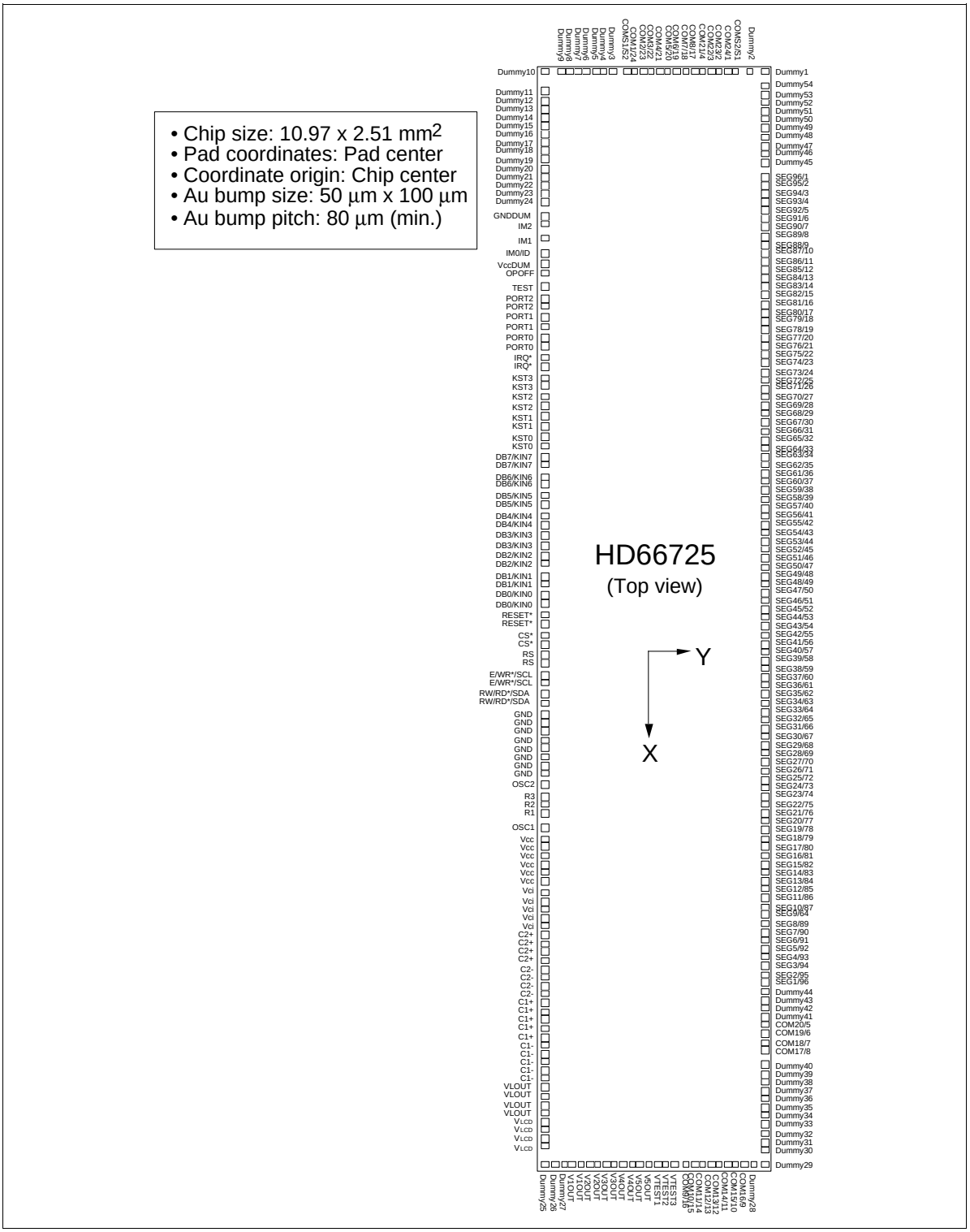


HD66724 Pad Coordinates

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
–	Dummy15	–4994	–1079	50	GND	564	–1079	104	V3OUT	4915	–469	142	SEG18/55	1572	999	–	Dummy41	–2863	999
–	Dummy16	–4771	–1079	51	GND	644	–1079	105	V3OUT	4915	–389	143	SEG19/54	1492	999	–	Dummy42	–2943	999
–	Dummy17	–4690	–1079	52	GND	725	–1079	106	V4OUT	4915	–308	144	SEG20/53	1411	999	–	Dummy43	–3024	999
–	Dummy18	–4610	–1079	53	GND	806	–1079	107	V4OUT	4915	–227	145	SEG21/52	1331	999	–	Dummy44	–3105	999
–	Dummy19	–4529	–1079	54	GND	886	–1079	108	V5OUT	4915	–147	146	SEG22/51	1250	999	–	Dummy45	–3185	999
–	Dummy20	–4449	–1079	55	GND	967	–1079	109	V5OUT	4915	–66	147	SEG23/50	1169	999	–	Dummy46	–3266	999
–	Dummy21	–4368	–1079	56	GND	1048	–1079	110	VTEST1	4915	15	148	SEG24/49	1089	999	197	COMS2/S1	–3347	999
1	GNDDUM	–4207	–1079	57	GND	1128	–1079	111	VTEST2	4915	95	149	SEG25/48	1008	999	198	COM24/1	–3427	999
2	IM2	–4126	–1079	58	OSC2	1209	–1079	112	VTEST3	4915	176	150	SEG26/47	927	999	199	COM23/2	–3508	999
3	IM1	–3942	–1079	59	R3	1364	–994	113	COM9/16	4915	282	151	SEG27/46	847	999	200	COM22/3	–3588	999
4	IM0/ID	–3758	–1079	60	R2	1445	–994	114	COM10/15	4915	363	152	SEG28/45	766	999	201	COM21/4	–3669	999
5	VccDUM	–3655	–1079	61	R1	1525	–994	115	COM11/14	4915	444	153	SEG29/44	685	999	–	Dummy47	–3830	1079
6	OPOFF	–3574	–1079	62	OSC1	1680	–1079	116	COM12/13	4915	524	154	SEG30/43	605	999	–	Dummy48	–3911	1079
7	TEST	–3390	–1079	63	Vcc	1783	–1079	117	COM13/12	4915	605	155	SEG31/42	524	999	–	Dummy49	–3992	1079
8	PORT2	–3287	–1079	64	Vcc	1864	–1079	118	COM14/11	4915	685	156	SEG32/41	444	999	–	Dummy50	–4072	1079
9	PORT2	–3206	–1079	65	Vcc	1945	–1079	119	COM15/10	4915	766	157	SEG33/40	363	999	–	Dummy51	–4153	1079
10	PORT1	–3103	–1079	66	Vcc	2025	–1079	120	COM16/9	4915	847	158	SEG34/39	282	999	–	Dummy52	–4234	1079
11	PORT1	–3022	–1079	67	Vcc	2106	–1079	–	Dummy23	4915	1079	159	SEG35/38	202	999	–	Dummy53	–4314	1079
12	PORT0	–2919	–1079	68	Vcc	2187	–1079	–	Dummy24	4717	1079	160	SEG36/37	121	999	–	Dummy54	–4395	1079
13	PORT0	–2838	–1079	69	Vci	2290	–999	–	Dummy25	4637	1079	161	SEG37/36	40	999	–	Dummy55	–4476	1079
14	IRQ*	–2735	–1079	70	Vci	2371	–999	–	Dummy26	4556	1079	162	SEG38/35	–40	999	–	Dummy56	–4556	1079
15	IRQ*	–2654	–1079	71	Vci	2451	–999	–	Dummy27	4476	1079	163	SEG39/34	–121	999	–	Dummy57	–4637	1079
16	KST3	–2551	–1079	72	Vci	2532	–999	–	Dummy28	4395	1079	164	SEG40/33	–202	999	–	Dummy58	–4717	1079
17	KST3	–2470	–1079	73	Vci	2613	–999	–	Dummy29	4314	1079	165	SEG41/32	–282	999	–	Dummy59	–4798	1079
18	KST2	–2367	–1079	74	C2+	2693	–999	–	Dummy30	4234	1079	166	SEG42/31	–363	999	–	Dummy1	–4994	1079
19	KST2	–2286	–1079	75	C2+	2774	–999	–	Dummy31	4153	1079	167	SEG43/30	–444	999	202	COM8/17	–4915	847
20	KST1	–2183	–1079	76	C2+	2854	–999	–	Dummy32	4072	1079	168	SEG44/29	–524	999	203	COM7/18	–4915	766
21	KST1	–2102	–1079	77	C2+	2935	–999	–	Dummy33	3992	1079	169	SEG45/28	–605	999	204	COM6/19	–4915	685
22	KST0	–1999	–1079	78	C2–	3016	–999	–	Dummy34	3911	1079	170	SEG46/27	–685	999	205	COM5/20	–4915	605
23	KST0	–1918	–1079	79	C2–	3096	–999	121	COM17/8	3750	999	171	SEG47/26	–766	999	206	COM4/21	–4915	524
24	DB7/KIN7	–1815	–1079	80	C2–	3177	–999	122	COM18/7	3669	999	172	SEG48/25	–847	999	207	COM3/22	–4915	444
25	DB7/KIN7	–1734	–1079	81	C2–	3258	–999	123	COM19/6	3588	999	173	SEG49/24	–927	999	208	COM2/23	–4915	363
26	DB6/KIN6	–1631	–1079	82	C1+	3338	–999	124	COM20/5	3508	999	174	SEG50/23	–1008	999	209	COM1/24	–4915	282
27	DB6/KIN6	–1551	–1079	83	C1+	3419	–999	–	Dummy35	3427	999	175	SEG51/22	–1089	999	210	COMS1/S2	–4915	202
28	DB5/KIN5	–1447	–1079	84	C1+	3500	–999	–	Dummy36	3347	999	176	SEG52/21	–1169	999	–	Dummy2	–4994	50
29	DB5/KIN5	–1367	–1079	85	C1+	3580	–999	–	Dummy37	3266	999	177	SEG53/20	–1250	999	–	Dummy3	–4994	–30
30	DB4/KIN4	–1263	–1079	86	C1+	3661	–999	–	Dummy38	3185	999	178	SEG54/19	–1331	999	–	Dummy4	–4994	–111
31	DB4/KIN4	–1183	–1079	87	C1–	3741	–999	–	Dummy39	3105	999	179	SEG55/18	–1411	999	–	Dummy5	–4994	–192
32	DB3/KIN3	–1079	–1079	88	C1–	3822	–999	–	Dummy40	3024	999	180	SEG56/17	–1492	999	–	Dummy6	–4994	–272
33	DB3/KIN3	–999	–1079	89	C1–	3903	–999	125	SEG1/72	2943	999	181	SEG57/16	–1572	999	–	Dummy7	–4994	–353
34	DB2/KIN2	–895	–1079	90	C1–	3983	–999	126	SEG2/71	2863	999	182	SEG58/15	–1653	999	–	Dummy8	–4994	–433
35	DB2/KIN2	–815	–1079	91	C1–	4064	–999	127	SEG3/70	2782	999	183	SEG59/14	–1734	999	–	Dummy9	–4994	–514
36	DB1/KIN1	–711	–1079	92	VLOUT	4145	–999	128	SEG4/69	2701	999	184	SEG60/13	–1814	999	–	Dummy10	–4994	–595
37	DB1/KIN1	–631	–1079	93	VLOUT	4225	–999	129	SEG5/68	2621	999	185	SEG61/12	–1895	999	–	Dummy11	–4994	–675
38	DB0/KIN0	–527	–1079	94	VLOUT	4306	–999	130	SEG6/67	2540	999	186	SEG62/11	–1976	999	–	Dummy12	–4994	–756
39	DB0/KIN0	–447	–1079	95	VLOUT	4387	–999	131	SEG7/66	2460	999	187	SEG63/10	–2056	999	–	Dummy13	–4994	–837
40	RESET*	–343	–1079	96	VLCD	4467	–999	132	SEG8/65	2379	999	188	SEG64/9	–2137	999	–	Dummy14	–4994	–917
41	RESET*	–263	–1079	97	VLCD	4548	–999	133	SEG9/64	2298	999	189	SEG65/8	–2218	999				
42	CS*	–159	–1079	98	VLCD	4629	–999	134	SEG10/63	2218	999	190	SEG66/7	–2298	999				
43	CS*	–79	–1079	99	VLCD	4709	–999	135	SEG11/62	2137	999	191	SEG67/6	–2379	999				
44	RS	24	–1079	–	Dummy22	4915	–1079	136	SEG12/61	2056	999	192	SEG68/5	–2460	999				
45	RS	105	–1079	100	V1OUT	4915	–792	137	SEG13/60	1976	999	193	SEG69/4	–2540	999				
46	E/WR*/SCL	198	–1079	101	V1OUT	4915	–711	138	SEG14/59	1895	999	194	SEG70/3	–2621	999				
47	E/WR*/SCL	279	–1079	102	V2OUT	4915	–631	139	SEG15/58	1814	999	195	SEG71/2	–2701	999				
48	RW/RD*/SDA	368	–1079	103	V2OUT	4915	–550	140	SEG16/57	1734	999	196	SEG72/1	–2782	999				
49	RW/RD*/SDA	449	–1079					141	SEG17/56	1653	999								

HD66725 Pad Arrangement

- Chip size: 10.97 x 2.51 mm^2
- Pad coordinates: Pad center
- Coordinate origin: Chip center
- Au bump size: 50 µm x 100 µm
- Au bump pitch: 80 µm (min.)

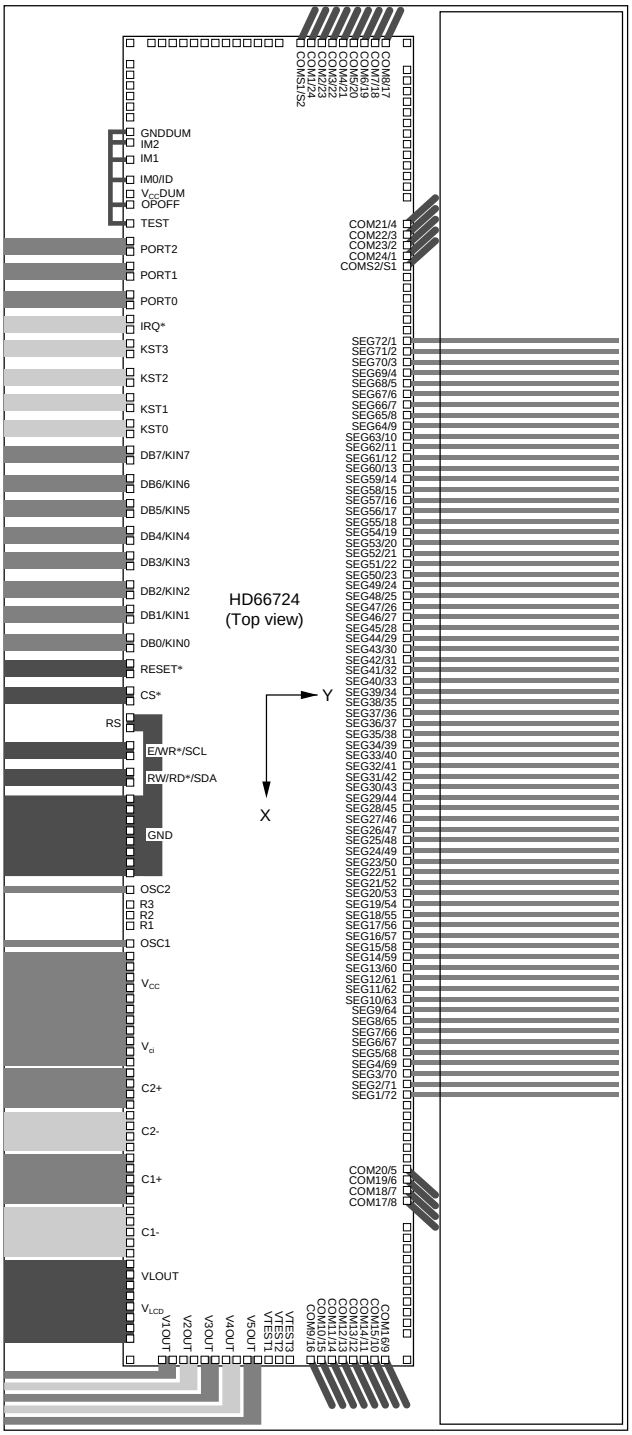


HD66725 Pad Coordinates

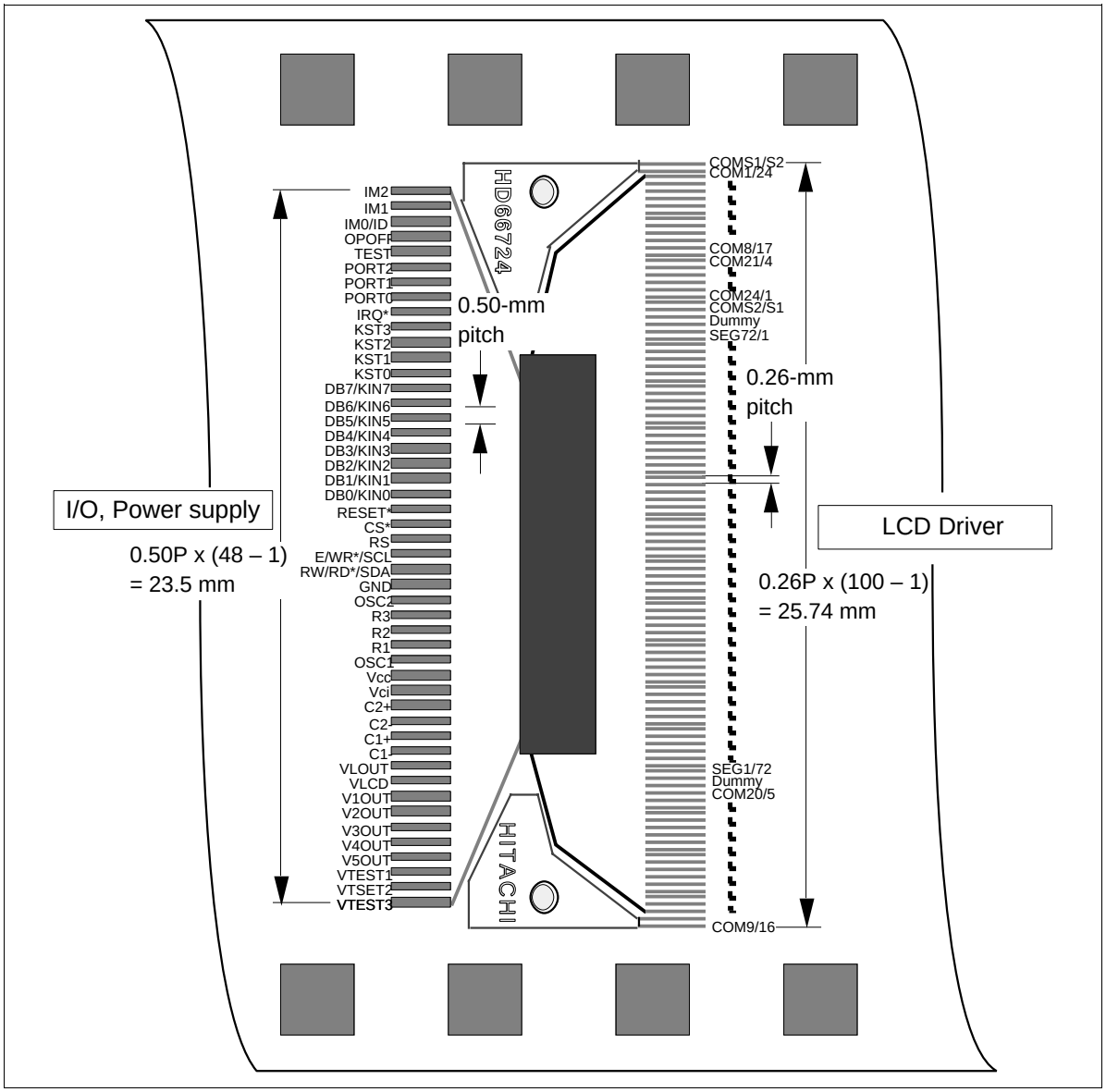
No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
—	Dummy10	–5309	–1079	46	E/WR*/SCL	513	–1079	103	V2OUT	5230	–550	146	SEG22/75	1726	999	206	SEG82/15	–3112	999
—	Dummy11	–5101	–1079	47	E/WR*/SCL	594	–1079	104	V3OUT	5230	–469	147	SEG23/74	1646	999	207	SEG83/14	–3193	999
—	Dummy12	–5021	–1079	48	RW/RD*/SDA	683	–1079	105	V3OUT	5230	–389	148	SEG24/73	1565	999	208	SEG84/13	–3273	999
—	Dummy13	–4940	–1079	49	RW/RD*/SDA	764	–1079	106	V4OUT	5230	–308	149	SEG25/72	1484	999	209	SEG85/12	–3354	999
—	Dummy14	–4859	–1079	50	GND	879	–1079	107	V4OUT	5230	–227	150	SEG26/71	1404	999	210	SEG86/11	–3435	999
—	Dummy15	–4779	–1079	51	GND	959	–1079	108	V5OUT	5230	–147	151	SEG27/70	1323	999	211	SEG87/10	–3515	999
—	Dummy16	–4698	–1079	52	GND	1040	–1079	109	V5OUT	5230	–66	152	SEG28/69	1242	999	212	SEG88/9	–3596	999
—	Dummy17	–4617	–1079	53	GND	1121	–1079	110	VTEST1	5230	15	153	SEG29/68	1162	999	213	SEG89/8	–3677	999
—	Dummy18	–4537	–1079	54	GND	1201	–1079	111	VTEST2	5230	95	154	SEG30/67	1081	999	214	SEG90/7	–3757	999
—	Dummy19	–4456	–1079	55	GND	1282	–1079	112	VTEST3	5230	176	155	SEG31/66	1000	999	215	SEG91/6	–3838	999
—	Dummy20	–4375	–1079	56	GND	1363	–1079	113	COM9/16	5230	282	156	SEG32/65	920	999	216	SEG92/5	–3919	999
—	Dummy21	–4295	–1079	57	GND	1443	–1079	114	COM10/15	5230	363	157	SEG33/64	839	999	217	SEG93/4	–3999	999
—	Dummy22	–4214	–1079	58	OSC2	1524	–1079	115	COM11/14	5230	444	158	SEG34/63	759	999	218	SEG94/3	–4080	999
—	Dummy23	–4134	–1079	59	R3	1679	–994	116	COM12/13	5230	524	159	SEG35/62	678	999	219	SEG95/2	–4161	999
—	Dummy24	–4053	–1079	60	R2	1760	–994	117	COM13/12	5230	605	160	SEG36/61	597	999	220	SEG96/1	–4241	999
1	GNDDUM	–3892	–1079	61	R1	1840	–994	118	COM14/11	5230	685	161	SEG37/60	517	999	—	Dummy45	–4404	1079
2	IM2	–3811	–1079	62	OSC1	1995	–1079	119	COM15/10	5230	766	162	SEG48/59	436	999	—	Dummy46	–4484	1079
3	IM1	–3627	–1079	63	Vcc	2098	–1079	120	COM16/9	5230	847	163	SEG39/58	355	999	—	Dummy47	–4565	1079
4	IM0/ID	–3443	–1079	64	Vcc	2179	–1079	—	Dummy28	5230	927	164	SEG40/57	275	999	—	Dummy48	–4646	1079
5	VccDUM	–3340	–1079	65	Vcc	2260	–1079	—	Dummy29	5230	1079	165	SEG41/56	194	999	—	Dummy49	–4726	1079
6	OPOFF	–3259	–1079	66	Vcc	2340	–1079	—	Dummy30	6032	1079	166	SEG42/55	113	999	—	Dummy50	–4807	1079
7	TEST	–3075	–1079	67	Vcc	2421	–1079	—	Dummy31	4952	1079	167	SEG43/54	33	999	—	Dummy51	–4888	1079
8	PORT2	–2972	–1079	68	Vcc	2502	–1079	—	Dummy32	4871	1079	168	SEG44/53	–48	999	—	Dummy52	–4968	1079
9	PORT2	–2891	–1079	69	Vci	2605	–999	—	Dummy33	4791	1079	169	SEG45/52	–129	999	—	Dummy53	–5049	1079
10	PORT1	–2788	–1079	70	Vci	2686	–999	—	Dummy34	4710	1079	170	SEG46/51	–209	999	—	Dummy54	–5129	1079
11	PORT1	–2707	–1079	71	Vci	2766	–999	—	Dummy35	4629	1079	171	SEG47/50	–290	999	—	Dummy1	–5309	1079
12	PORT0	–2604	–1079	72	Vci	2847	–999	—	Dummy36	4549	1079	172	SEG48/49	–370	999	—	Dummy2	–5309	955
13	PORT0	–2523	–1079	73	Vci	2928	–999	—	Dummy37	4468	1079	173	SEG49/48	–451	999	221	COMS2/S1	–5229	794
14	IRQ*	–2420	–1079	74	C2+	3008	–999	—	Dummy38	4387	1079	174	SEG50/47	–532	999	222	COM24/1	–5229	713
15	IRQ*	–2339	–1079	75	C2+	3089	–999	—	Dummy39	4307	1079	175	SEG51/46	–612	999	223	COM23/2	–5229	633
16	KST3	–2236	–1079	76	C2+	3169	–999	—	Dummy40	4226	1079	176	SEG52/45	–693	999	224	COM22/3	–5229	552
17	KST3	–2155	–1079	77	C2+	3250	–999	121	COM17/8	4065	999	177	SEG53/44	–774	999	225	COM21/4	–5229	471
18	KST2	–2052	–1079	78	C2–	3331	–999	122	COM18/7	3984	999	178	SEG54/43	–854	999	226	COM8/17	–5229	391
19	KST2	–1971	–1079	79	C2–	3411	–999	123	COM19/6	3903	999	179	SEG55/42	–935	999	227	COM7/18	–5229	310
20	KST1	–1868	–1079	80	C2–	3492	–999	124	COM20/5	3823	999	180	SEG56/41	–1016	999	228	COM6/19	–5229	229
21	KST1	–1787	–1079	81	C2–	3573	–999	—	Dummy41	3742	999	181	SEG57/40	–1096	999	229	COM5/20	–5229	149
22	KST0	–1684	–1079	82	C1+	3653	–999	—	Dummy42	3662	999	182	SEG58/39	–1177	999	230	COM4/21	–5229	68
23	KST0	–1603	–1079	83	C1+	3734	–999	—	Dummy43	3581	999	183	SEG59/38	–1257	999	231	COM3/22	–5229	–13
24	DB7/KIN7	–1500	–1079	84	C1+	3815	–999	—	Dummy44	3500	999	184	SEG60/37	–1338	999	232	COM2/23	–5229	–93
25	DB7/KIN7	–1419	–1079	85	C1+	3895	–999	125	SEG1/96	3420	999	185	SEG61/36	–1419	999	233	COM1/24	–5229	–174
26	DB6/KIN6	–1316	–1079	86	C1+	3976	–999	126	SET2/95	3339	999	186	SEG62/35	–1499	999	234	COMS1/S2	–5229	–255
27	DB6/KIN6	–1236	–1079	87	C1–	4056	–999	127	SEG3/94	3258	999	187	SEG63/34	–1580	999	—	Dummy3	–5309	–433
28	DB5/KIN5	–1132	–1079	88	C1–	4137	–999	128	SEG4/93	3178	999	188	SEG64/33	–1661	999	—	Dummy4	–5309	–514
29	DB5/KIN5	–1052	–1079	89	C1–	4218	–999	129	SEG5/92	3097	999	189	SEG65/32	–1741	999	—	Dummy5	–5309	–595
30	DB4/KIN4	–948	–1079	90	C1–	4298	–999	130	SEG6/91	3016	999	190	SEG66/31	–1822	999	—	Dummy6	–5309	–675
31	DB4/KIN4	–868	–1079	91	C1–	4379	–999	131	SEG7/90	2936	999	191	SEG67/30	–1903	999	—	Dummy7	–5309	–756
32	DB3/KIN3	–764	–1079	92	VLOUT	4460	–999	132	SEG8/89	2855	999	192	SEG68/29	–1983	999	—	Dummy8	–5309	–837
33	DB3/KIN3	–684	–1079	93	VLOUT	4540	–999	133	SEG9/88	2775	999	193	SEG69/28	–2064	999	—	Dummy9	–5309	–917
34	DB2/KIN2	–580	–1079	94	VLOUT	4621	–999	134	SEG10/87	2694	999	194	SEG70/27	–2145	999				
35	DB2/KIN2	–500	–1079	95	VLOUT	4702	–999	135	SEG11/86	2613	999	195	SEG71/26	–2225	999				
36	DB1/KIN1	–396	–1079	96	VLCD	4782	–999	136	SEG12/85	2533	999	196	SEG72/25	–2306	999				
37	DB1/KIN1	–316	–1079	97	VLCD	4863	–999	137	SEG13/84	2452	999	197	SEG73/24	–2386	999				
38	DB0/KIN0	–212	–1079	98	VLCD	4944	–999	138	SEG14/83	2371	999	198	SEG74/23	–2467	999				
39	DB0/KIN0	–132	–1079	99	VLCD	5024	–999	139	SEG15/82	2291	999	199	SEG75/22	–2548	999				
40	RESET*	–28	–1079	—	Dummy25	5230	–1079	140	SEG16/81	2210	999	200	SEG76/21	–2628	999				
41	RESET*	52	–1079	—	Dummy26	5230	–953	141	SEG17/80	2129	999	201	SEG77/20	–2709	999				
42	CS*	156	–1079	—	Dummy27	5230	–872	142	SEG18/79	2049	999	202	SEG78/19	–2790	999				
43	CS*	236	–1079	100	V1OUT	5230	–792	143	SEG19/78	1968	999	203	SEG79/18	–2870	999				
44	RS	339	–1079	101	V1OUT	5230	–711	144	SEG20/77	1887	999	204	SEG80/17	–2951	999				
45	RS	420	–1079	102	V2OUT	5230	–631	145	SEG21/76	1807	999	205	SEG81/16	–3032	999				

Chip-on-Glass (COG) Routing Example

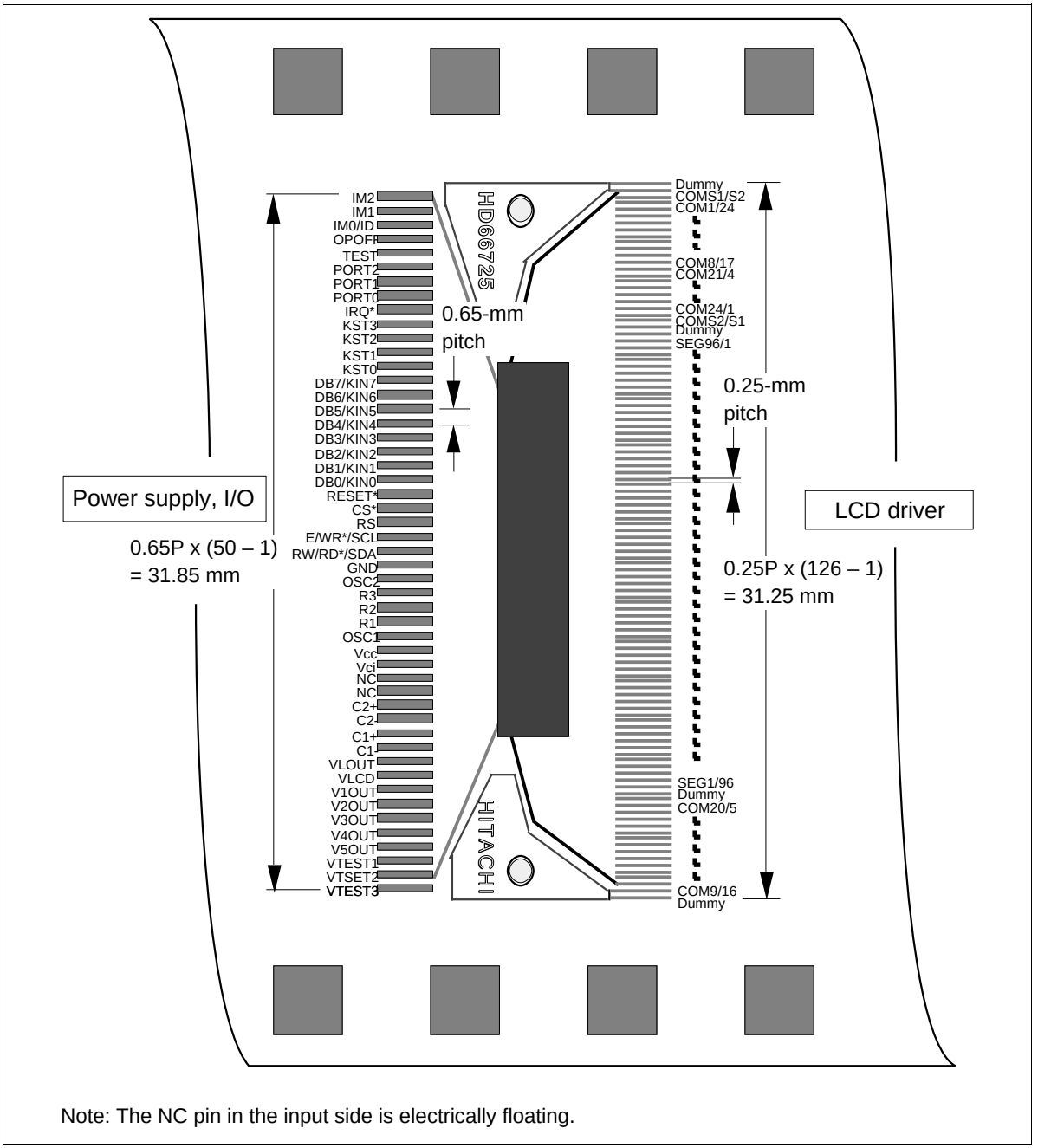
- Clock-synchronized serial bus
- Unused key scan
- Unused port output
- Quadruple booster
- Internal operational amplifier



TCP Dimensions (HD66724TA0)



TCP Dimensions (HD66725TA0)



Note: The NC pin in the input side is electrically floating.

Pin Functions

Table 2 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions
IM2, IM1	2	I	V_{CC} or GND	Selects the MPU interface mode: IM2 "GND" "GND" Clock-synchronized serial interface IM2 "GND" "Vcc" 68-system parallel bus interface IM2 "Vcc" "GND" Setting inhibited IM2 "Vcc" "Vcc" 80-system parallel bus interface
IM0/ID	1	I	V_{CC} or GND	Inputs the ID of the device ID code for a serial bus interface. Selects the transfer bus width for a parallel bus interface. GND: 8-bit bus, Vcc: 4-bit bus
CS*	2	I	MPU	Selects the HD66724/HD66725: Low: HD66724/HD66725 are selected and can be accessed High: HD66724/HD66725 are not selected and cannot be accessed Must be fixed at GND level when not in use.
RS	2	I	MPU	Selects the register for a parallel bus interface. Low: Instruction High: RAM access Selects the key scan interrupt method in the standby period for a serial interface. Monitors a total of eight keys connected to KST0 at the GND level and monitors all keys at the Vcc level to generate an interrupt. Must be fixed at the Vcc or GND level.
E/WR*/SCL	2	I	MPU	Inputs the serial transfer clock for a serial interface. Fetches data at the rising edge of a clock. For a 68-system parallel bus interface, serves as an enable signal to activate data read/write operation. For an 80-system parallel bus interface, serves as a write strobe signal and writes data at the low level.
RW/RD*/ SDA	2	I/O or I	MPU	Serves as the bidirectional serial transfer data for a serial interface. Sends/Receives data. For a 68-system parallel bus interface, serves as a signal to select data read/write operation. For an 80-system parallel bus interface, serves as a write strobe signal and reads data at the low level.
IRQ*	2	O	MPU	Generates the key scan interrupt signal.
KST0–KST3	8	O	Key matrix	Generates strobe signals for latching scanned data from the key matrix at specific time intervals. Available for a serial interface only.
DB0/KIN0–DB7/KIN7	16	I or I/O	Key matrix or MPU	Samples key state from key matrix synchronously with strobe signals for a serial interface. Serves as a bidirectional data bus for a parallel bus interface. For a four-bit bus, data transfer uses KIN7/DB7–KIN4/DB4; leave KIN3/DB3–KIN0/DB0 disconnected.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
PORT0–PORT2	6	O	General output	General output ports. These ports cannot drive current such as for LEDs or backlighting control. Boost the current using an external transistor.
COMS1/2, COMS2/1	2	O	LCD	Two common output signals for segment-icon display.
COM1/24–COM24/1	24	O	LCD	Common output signals for character/graphics display: COM1 to COM8 for the first line; COM9 to COM16 for the second line, and COM17 to COM24 for the third line. All the unused pins output deselection waveforms. In the sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, COM1/24 is COM1. If CMS = 1, COM1/24 is COM24.
SEG1/72–SEG72/1 (HD66724)	72	O	LCD	Segment output signals for segment-icon display and character/graphics display. In the sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level.
SEG1/96–SEG96/1 (HD66725)	96			The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, SEG1/72 (96) is SEG1. If SGS = 1, SEG1/72 (96) is SEG72 (96).
V1OUT–V5OUT	10	O or I	Open or external bleeder-resistor	Used for output from the internal operational amplifiers when they are used (OPOFF = GND); attach a capacitor to stabilize the output. When the amplifiers are not used (OPOFF = V_{CC}), V1 to V5 voltages can be supplied to these pins externally.
V_{LCD}	4	—	Power supply	Power supply for LCD drive. V_{LCD} – GND = 6.5 V max.
V_{CC}, GND	14	—	Power supply	V_{CC}: +1.8 V to +5.5 V; GND (logic): 0 V
OSC1, OSC2	2	I or O	Oscillation resistor or clock	For R-C oscillation using an external resistor, connect an external resistor. For R-C oscillation using an internal resistor, connect R1–R3 to OSC2 and leave OSC1 disconnected. For external clock supply, input clock pulses to OSC1.
R1–R3	3	O	OSC2	For R-C oscillation using an internal resistor, adjust the internal resistor value. Fluctuation of the resistor value is ±30% of the reference value. Care must be taken to avoid fluctuation of the frame frequency in crystal display drive operation.
Vci	5	I	Power supply	Inputs a reference voltage and supplies power to the booster; generates the liquid crystal display drive voltage from the operating voltage. Vci = 0 V to 3.0 V ≤ V_{CC} Must be left disconnected when the booster is not used.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
VLOUT	4	O	V_{LCD} pin/booster capacitance	Potential difference between Vci and GND is boosted twice or three times and then output. Magnitude of boost is selected by instruction.
C1+, C1–	10	—	Booster capacitance	External capacitance should be connected here when using the double or triple booster.
C2+, C2–	8	—	Booster capacitance	External capacitance should be connected here when using the triple booster. Must be left disconnected only when using the double booster.
RESET*	2	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low. Must reset after power-on.
OPOFF	1	I	V_{CC} or GND	Turns the internal operational amplifier off when OPOFF = V_{CC}, and turns it on when OPOFF = GND. If the amplifier is turned off (OPOFF = V_{CC}), V1 to V5 must be supplied to the V1OUT to V5OUT pins.
VccDUM	1	O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.
GNDDUM	1	O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
VTEST1–VTEST3	3	—	—	Test pins. Must be left disconnected.

Block Function Description

System Interface

The HD66724/HD66725 have five types of system interfaces, and a clock-synchronized serial, a 68-system 4-bit/8-bit bus, and a 80-system 4-bit/8-bit bus. The interface mode is selected by the IM2-0 pins. The key scan of the HD66724/HD66725 are not available for the 4-bit/8-bit bus interface. Instead, use the clock-synchronized serial interface.

The HD66724/HD66725 have two 8-bit registers: an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as clear display, display control, and address information for the display data RAM (DDRAM), character generator RAM (CGRAM), and segment RAM (SEGRAM).

The DR temporarily stores the data to be written to and read from the DDRAM, CGRAM, or SEGRAM. The data written to the DR from the MPU is automatically written to the DDRAM, CGRAM, or SEGRAM by internal operation. Since the data is read from the RAM through the DR, the first read data is invalid and the second read data is valid. After reading, the data in DDRAM, CGRAM, or SEGRAM at the next address is sent to the DR for the next reading from the MPU.

Execution time for instruction excluding clear display is 0 clock cycle and instructions can be written in succession.

Table 3 Register Selection by RS and R/W Bits

R/W Bits	RS Bits	Operations
0	0	Writes an instruction to the IR
1	0	Reads key scan data (SCAN0-3)
0	1	Writes the data to the DR to DDRAM, CGRAM, or SEGRAM
1	1	Reads the data from the DDRAM, CGRAM, or SEGRAM to DR

Key Scan Registers (SCAN0 to SCAN3)

The key matrix scanner senses and holds the key states at each rising edge of key strobe signals KST0 to KST3 that are output by the HD66724/HD66725. After passing through the key matrix, these strobe signals are used to sample the key states on eight inputs from KIN0 to KIN7, enabling up to 32 keys to be scanned.

Key states KIN0 to KIN7 are sampled by key strobe signal KST0 and latched into register SCAN0. Similarly, the data sampled by strobe signals KST1 to KST3 is latched into registers SCAN1 to SCAN3, respectively. For details, see the Key Scan Control section.

General Output Ports (PORT0 to PORT 2)

The HD66724/HD66725 have three general output ports. These ports control drive current such as that for LEDs or backlighting by using the current boosted by an external transistor.

Address Counter (AC)

The address counter (AC) assigns addresses to DDRAM, CGRAM, or SEGRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC. Selection of DDRAM, CGRAM, and SEGRAM is also determined concurrently by the RAM select bit (RM1/0).

After writing into (reading from) DDRAM, CGRAM, or SEGRAM, the AC is automatically incremented by 1 (or decremented by 1). The cursor display position is determined by the address counter value.

Display Data RAM (DDRAM)

The display data RAM (DDRAM) stores display data represented in 8-bit character codes in the character display mode. Its capacity is 80 × 8 bits, or 80 characters, which is equivalent to an area of 16 characters × 5 lines. Any number of display lines (LCD drive duty ratio) from 1 to 3 can be selected by software. Here, assignment of DDRAM addresses is the same for all display modes (table 5). The line to be displayed at the top of the display (display-start line) can also be selected by register settings. The graphics display mode does not use the data in the DDRAM.

Character Generator ROM (CGROM)

The character generator ROM (CGROM) generates 6 × 8-dot character patterns from 8-bit character codes. It is equipped with a memory bank to generate 240 character patterns or 192 character patterns, which can be switched according to applications. For details, see the CGROM Bank Switching Function section. Table 6 illustrates the relation between character codes and character patterns for the Hitachi standard CGROM. User-defined character patterns are also available using a mask-programmed ROM (see the Modifying Character Patterns section).

Character Generator RAM (CGRAM)

The character generator RAM (CGRAM) allows the user to redefine the character patterns in the character display mode. Up to 64 character patterns of 6 x 8-dot characters can be simultaneously displayed. The DDRAM-specified character code can be selected to display one of these user font patterns.

The CGRAM serves as a RAM to store 72 x 24-dot (96 x 24-dot) bit pattern data in the graphics display mode. Here, display patterns are directly written to the CGRAM. Character codes set in the DDRAM are not used. For details, see the Graphics Display Function section.

Segment RAM (SEGRAM)

The segment RAM (SEGRAM) is used to enable control of segments such as icons and marks through the user program. Segments and characters are driven by a multiplexing drive method.

The SEGRAM has a capacity of 96 × 2 bits, to control the display of a maximum of 144 (192) icons and marks. While COMS1 and COMS2 outputs are being selected, the SEGRAM is read and segments (icons and marks) are displayed by a multiplexing drive method (72 (96) segments each during COMS1 and COMS2 selection).

Bits in SEGRAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DDRAM and CGRAM.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as DDRAM, CGROM, CGRAM, and SEGRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another. This prevents flickering in areas other than the display area when writing the data to the DDRAM, for example.

Cursor/Blink Control Circuit

The cursor/blink (or black-white reversed) control is used to create a cursor or a flashing area on the display in a position corresponding to the location stored in the address counter (AC).

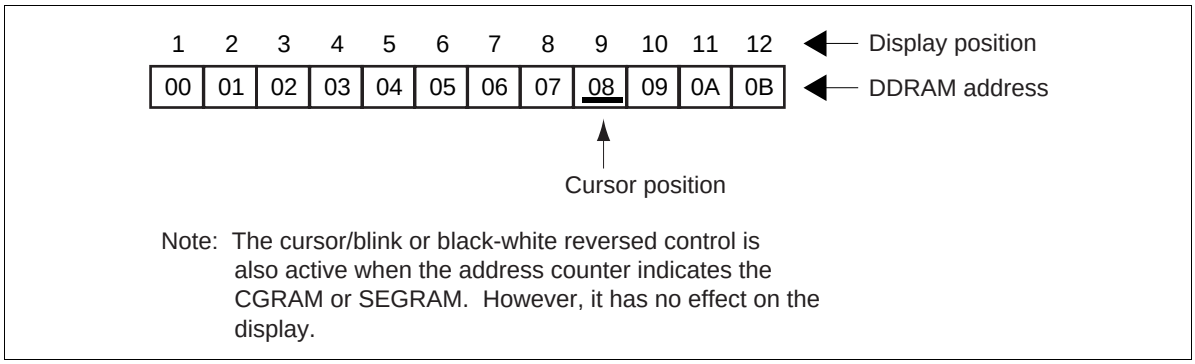


Figure 1 Cursor Position and DDRAM Address (When AC = 08H)

Oscillation Circuit (OSC)

The HD66724/HD66725 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Internal resistors can be used for R-C oscillation. If this is done, care must be taken due to variations in the oscillation frequency caused by fluctuations in internal-resistor values. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 26 common signal drivers (COM1 to COM24, COMS1, COMS2) and 72 (96) segment signal drivers (SEG1 to SEG72 (96)). When the number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output deselection waveforms.

The character pattern data is sent serially through a 72-bit (96-bit) shift register and latched when all needed data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs.

The shift direction of 72-bit (96-bit) data can be changed by the SGS bit. The shift direction for the common driver can also be changed by the CMS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

Booster (DC-DC Converter)

The booster doubles or triples a voltage input to the Vci pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. Boost output level from single to triple boost can be software-selected. For details, see the Power Supply for Liquid Crystal Display Drive section.

V-Pin Voltage Follower

A voltage follower for each voltage level (V1 to V5) reduces current consumption by the LCD drive power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD drive voltage. This internal bleeder-resistor can be software-specified from 1/2 bias to 1/6.5 bias, according to the liquid crystal display drive duty value. The voltage followers can be turned off while multiplexing drive is not being used. For details, see the Power Supply for Liquid Crystal Display Drive section.

Contrast Adjuster

The contrast adjuster can be used to adjust LCD contrast in 32 steps by varying the LCD drive voltage by software. This can be used to select an appropriate LCD brightness or to compensate for temperature.

Table 4 DDRAM Addresses and Display Positions

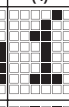
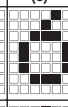
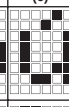
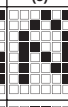
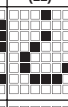
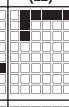
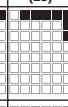
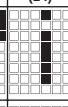
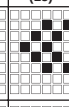
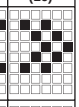
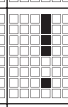
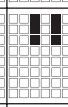
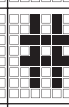
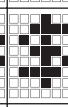
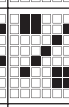
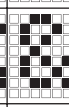
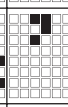
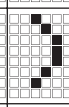
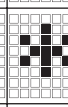
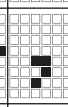
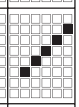
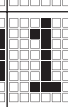
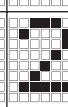
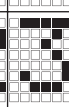
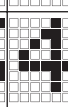
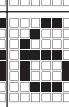
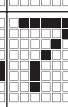
Dis-play Line	1st Char.	2nd Char.	3rd Char.	4th Char.	5th Char.	6th Char.	7th Char.	8th Char.	9th Char.	10th Char.	11th Char.	12th Char.	13th Char.	14th Char.	15th Char.	16th Char.
1st	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2nd	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
3rd	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
4th	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
5th	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

Note: When SGS = 0, SEG 1/72 (96) to SEG 6/67 (91) appear at the first character at the extreme left of the screen.
When SGS = 1, SEG 72 (96)/1 to SEG 67 (91)/6 appear at the first character at the extreme left of the screen.

Table 5 Display-Line Modes, Display-Start Line, and DDRAM Addresses

			Display-Start Lines				
Display-Line Mode	**Duty Ratio**	**Common Pins**	**1st Line (SN = 000)**	**2nd Line (SN = 001)**	**3rd Line (SN = 010)**	**4th Line (SN = 011)**	**5th Line (SN = 100)**
1-line (NL = 001)	1/10	COM1–COM8	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH
2-line (NL = 010)	1/18	COM1–COM8	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH
2-line (NL = 010)	1/18	COM9–COM16	10H–1FH	20H–2FH	30H–3FH	40H–4FH	00H–0FH
3-line (NL = 011)	1/26	COM1–COM8	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH
3-line (NL = 011)	1/26	COM9–COM16	10H–1FH	20H–2FH	30H–3FH	40H–4FH	00H–0FH
3-line (NL = 011)	1/26	COM17–COM24	20H–2FH	30H–3FH	40H–4FH	00H–0FH	10H–1FH

Table 6 CGROM Memory Bank 0 (ROM Bit = 0)

Upper bits / Lower bits	x 0	x 1	x 2	x 3	x 4	x 5	x 6	x 7	x 8	x 9	x A	x B	x C	x D	x E	x F
0 y	CGRAM (1)	CGRAM (2)	CGRAM (3)	CGRAM (4)	CGRAM (5)	CGRAM (6)	CGRAM (7)	CGRAM (8)	CGRAM (9)	CGRAM (10)	CGRAM (11)	CGRAM (12)	CGRAM (13)	CGRAM (14)	CGRAM (15)	CGRAM (16)
1 y																
2 y																
3 y																
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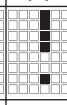
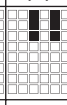
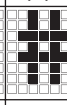
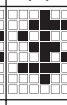
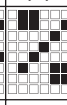
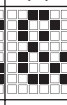
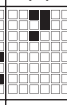
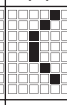
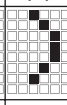
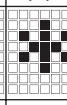
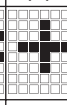
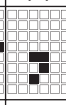
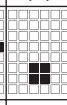
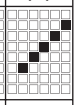
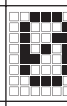
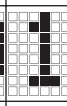
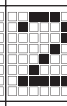
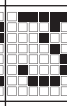
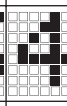
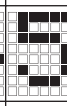
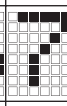
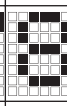
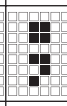
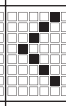
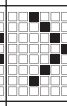
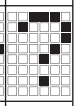
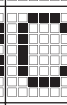
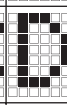
8 y																
9 y																
A y																
B y																
C y																
D y																
E y																
F y																

Table 7 CGROM Memory Bank 1 (ROM Bit = 1)

Upper bits / Lower bits	x 0	x 1	x 2	x 3	x 4	x 5	x 6	x 7	x 8	x 9	x A	x B	x C	x D	x E	x F
0 y	CGRAM (1)	CGRAM (2)	CGRAM (3)	CGRAM (4)	CGRAM (5)	CGRAM (6)	CGRAM (7)	CGRAM (8)	CGRAM (9)	CGRAM (10)	CGRAM (11)	CGRAM (12)	CGRAM (13)	CGRAM (14)	CGRAM (15)	CGRAM (16)
1 y	CGRAM (17)	CGRAM (18)	CGRAM (19)	CGRAM (20)	CGRAM (21)	CGRAM (22)	CGRAM (23)	CGRAM (24)	CGRAM (25)	CGRAM (26)	CGRAM (27)	CGRAM (28)	CGRAM (29)	CGRAM (30)	CGRAM (31)	CGRAM (32)
2 y																
3 y																
4 y																
5 y																
6 y																
7 y																
8 y	CGRAM (33)	CGRAM (34)	CGRAM (35)	CGRAM (36)	CGRAM (37)	CGRAM (38)	CGRAM (39)	CGRAM (40)	CGRAM (41)	CGRAM (42)	CGRAM (43)	CGRAM (44)	CGRAM (45)	CGRAM (46)	CGRAM (47)	CGRAM (48)
9 y	CGRAM (49)	CGRAM (50)	CGRAM (51)	CGRAM (52)	CGRAM (53)	CGRAM (54)	CGRAM (55)	CGRAM (56)	CGRAM (57)	CGRAM (58)	CGRAM (59)	CGRAM (60)	CGRAM (61)	CGRAM (62)	CGRAM (63)	CGRAM (64)
A y																
B y																
C y																
D y																
E y																
F y																

CGRAM Address Map

Table 8 Relationship between Character Display Mode (GR = 0) and CGRAM Address

Font Bank	Memory Bank: ROM = 0, 1															
Character Code	"00"H	"01"H	"02"H	"03"H	"04"H	"05"H	"06"H	"07"H	"08"H	"09"H	"0A"H	"0B"H	"0C"H	"0D"H	"0E"H	"0F"H
CGRAM Address (HEX)	000 to 005	006 to 00B	00C to 011	012 to 017	018 to 01D	01E to 023	024 to 029	02A to 02F	030 to 035	036 to 03B	03C to 041	042 to 047	048 to 04D	04E to 053	054 to 059	05A to 05F
Font Bank	Memory Bank: ROM = 1															
Character Code	"10"H	"11"H	"12"H	"13"H	"14"H	"15"H	"16"H	"17"H	"18"H	"19"H	"1A"H	"1B"H	"1C"H	"1D"H	"1E"H	"1F"H
CGRAM Address (HEX)	100 to 105	106 to 10B	10C to 111	112 to 117	118 to 11D	11E to 123	124 to 129	12A to 12F	130 to 135	136 to 13B	13C to 141	142 to 147	148 to 14D	14E to 153	154 to 159	15A to 15F
Font Bank	Memory Bank: ROM = 1															
Character Code	"80"H	"81"H	"82"H	"83"H	"84"H	"85"H	"86"H	"87"H	"88"H	"89"H	"8A"H	"8B"H	"8C"H	"8D"H	"8E"H	"8F"H
CGRAM Address (HEX)	200 to 205	206 to 20B	20C to 211	212 to 217	218 to 21D	21E to 223	224 to 229	22A to 22F	230 to 235	236 to 23B	23C to 241	242 to 247	248 to 24D	24E to 253	254 to 259	25A to 25F
Font Bank	Memory Bank: ROM = 1															
Character Code	"90"H	"91"H	"92"H	"93"H	"94"H	"95"H	"96"H	"97"H	"98"H	"99"H	"9A"H	"9B"H	"9C"H	"9D"H	"9E"H	"9F"H
CGRAM Address (HEX)	300 to 305	306 to 30B	30C to 311	312 to 317	318 to 31D	31E to 323	324 to 329	32A to 32F	330 to 335	336 to 33B	33C to 341	342 to 347	348 to 34D	34E to 353	354 to 359	35A to 35F

Notes: 1. In the character display mode (GR = 0), CGRAM font pattern is displayed using character codes set to DDRAM as per the above table. In the graphics display mode (GR = 1), CGRAM data is displayed irrespective of the DDRAM set data (character code).

2. When the memory bank switching bit generates ROM = 0, CGRAM fonts for 16 character codes "00"H to "0F"H can be displayed. When ROM = 1, CGRAM fonts for 64 character codes "00"H to "1F"H and "80"H to "9F"H can be displayed.

Table 9 Relationship between CGRAM Address and Character Pattern (CGRAM Data)

Character Code	"00"H						"01"H							"8F"H					
CGRAM Address	000	001	002	003	004	005	006	007	008	009	00A	00B	00C ▪▪▪▪▪▪▪	35A	35B	35C	35D	35E	35F
DB0	0	0	1	1	1	0	0	1	1	1	1	0	0 ▪▪▪▪▪▪▪	0	1	1	1	1	1
DB1	0	1	0	0	0	1	0	1	0	0	0	1	0 ▪▪▪▪▪▪▪	0	1	0	0	0	0
DB2	0	1	0	0	0	1	0	1	0	0	0	1	0 ▪▪▪▪▪▪▪	0	1	0	0	0	0
DB3	0	1	0	0	0	1	0	1	1	1	1	0	0 ▪▪▪▪▪▪▪	0	1	1	1	1	0
DB4	0	1	1	1	1	1	0	1	0	0	0	1	0 ▪▪▪▪▪▪▪	0	1	0	0	0	0
DB5	0	1	0	0	0	1	0	1	0	0	0	1	0 ▪▪▪▪▪▪▪	0	1	0	0	0	0
DB6	0	1	0	0	0	1	0	1	1	1	1	0	0 ▪▪▪▪▪▪▪	0	1	0	0	0	0
DB7	0	0	0	0	0	0	0	0	0	0	0	0	0 ▪▪▪▪▪▪▪	0	0	0	0	0	0

Notes: 1. The least significant bit (LSB) of write data is displayed on the first line. The most significant bit (MSB) is displayed on the 8th raster-row.
2. The 8th raster-row is the cursor position and its display is formed by a logical OR with the cursor.
3. A set bit in the CGRAM data corresponds to display selection (lit) and 0 to non-selection (unlit).

Table 10 Relationship between Display Position and CGRAM Address in Graphics Display Mode (GR = 1)

Display Line	1st Char.	2nd Char.	3rd Char.	4th Char.	5th Char.	6th Char.	7th Char.	8th Char.	9th Char.	10th Char.	11th Char.	12th Char.	13th Char.	14th Char.	15th Char.	16th Char.
1st	000 to 005	006 to 00B	00C to 011	012 to 017	018 to 01D	01E to 023	024 to 029	02A to 02F	030 to 035	036 to 03B	03C to 041	042 to 047	048 to 04D	04E to 053	054 to 059	05A to 05F
2nd	100 to 105	106 to 10B	10C to 111	112 to 117	118 to 11D	11E to 123	124 to 129	12A to 12F	130 to 135	136 to 13B	13C to 141	142 to 147	148 to 14D	14E to 153	154 to 159	15A to 15F
3rd	202 to 205	206 to 20B	20C to 211	212 to 217	218 to 21D	21E to 223	224 to 229	22A to 22F	230 to 235	236 to 23B	23C to 241	242 to 247	248 to 24D	24E to 253	254 to 259	25A to 25F
4th	303 to 305	306 to 30B	33C to 311	312 to 317	318 to 31D	31E to 323	324 to 329	32A to 32F	330 to 335	336 to 33B	33C to 341	342 to 347	348 to 34D	34E to 353	354 to 359	35A to 35F

Notes: 1. In the graphic display mode (GR = 1), graphics pattern is displayed using bitmap data set to CGRAM as per the above table.
2. Each display character and display line are converted to 6-dot width/character and 8 dots/line, respectively.
3. The 4th line is displayed by vertical smooth scroll operation.

Table 11 Relationship between CGRAM Address and Screen Display Position in Graphics Display Mode (GR = 1) (HD66724)

Segment Driver		SEG1/72	SEG2/71	SEG3/70	SEG4/69	SEG5/68	SEG6/67	SEG7/66	SEG8/65	SEG9/64	SEG10/63	SEG11/62	SEG12/61	SEG13/60	SEG14/59	SEG15/58	SEG16/57	SEG17/56	▪▪▪	SEG68/5	SEG69/4	SEG70/3	SEG71/2	SEG72/1	Segment / Common
Address	SGS="0"	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	▪▪▪	043	044	045	046	047	(HEX)
	SGS="1"	047	046	045	044	043	042	041	040	03F	02E	03D	03C	03B	03A	039	038	037	▪▪▪	004	003	002	001	000	
	DB0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	▪▪▪	0	0	1	0	0	COM1
	DB1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	▪▪▪	0	1	1	0	0	COM2
	DB2	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	▪▪▪	0	0	1	0	0	COM3
	DB3	0	0	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	▪▪▪	0	0	1	0	0	COM4
	DB4	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	▪▪▪	0	0	1	0	0	COM5
	DB5	0	0	1	1	1	1	1	1	1	1	1	0	0	0	1	0	0	▪▪▪	0	0	1	0	0	COM6
	DB6	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	▪▪▪	0	1	1	1	0	COM7
	DB7	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	▪▪▪	0	0	0	0	0	COM8
Address	SGS="0"	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	▪▪▪	143	144	145	146	147	(HEX)
	SGS="1"	147	146	145	144	143	142	141	140	13F	13E	13D	13C	13B	13A	139	138	137	▪▪▪	104	103	102	101	100	
	DB0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	0	▪▪▪	0	1	1	1	0	COM9
	DB1	0	0	0	1	0	0	1	0	0	1	0	0	0	1	0	0	0	▪▪▪	1	0	0	0	1	COM10
	DB2	0	1	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	▪▪▪	0	0	0	0	1	COM11
	DB3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	▪▪▪	0	0	0	1	0	COM12
	DB4	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	▪▪▪	0	0	1	0	0	COM13
	DB5	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	▪▪▪	0	1	0	0	0	COM14
	DB6	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	1	1	▪▪▪	1	1	1	1	1	COM15
	DB7	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	▪▪▪	0	0	0	0	0	COM16
Address	SGS="0"	200	201	202	203	204	205	206	207	208	209	20A	20B	20C	20D	20E	20F	210	▪▪▪	243	244	245	246	247	(HEX)
	SGS="1"	247	246	245	244	243	242	241	240	23F	23E	23D	23C	23B	23A	239	238	237	▪▪▪	205	204	203	201	200	
	DB0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	▪▪▪	1	1	1	1	1	COM17
	DB1	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	▪▪▪	0	0	0	1	0	COM18
	DB2	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	▪▪▪	0	0	1	0	0	COM19
	DB3	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	▪▪▪	0	0	0	1	0	COM20
	DB4	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	▪▪▪	0	0	0	0	1	COM21
	DB5	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	▪▪▪	1	0	0	0	1	COM22
	DB6	0	0	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	▪▪▪	0	1	1	1	0	COM23
	DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	▪▪▪	0	0	0	0	0	COM24

Notes: 1. In the graphics display mode (GR=1), the CGRAM data is displayed irrespective of the DDRAM set data.
2. The HD66725 can display addresses from 000H to 35FH.
3. A set bit in the CGRAM data corresponds to display selection (lit) and 0 to non-selection (unlit).

SEGRAM Address Map

Table 12 Relationship between SEGRAM Address and Screen Display Position (HD66724)

Segment Driver		SEG1/72	SEG2/71	SEG3/70	SEG4/69	SEG5/68	SEG6/67	SEG7/66	SEG8/65	SEG9/64	SEG10/63	SEG11/62	SEG12/61	SEG13/60	SEG14/59	SEG15/58	SEG16/57	SEG17/56	▪▪▪▪▪	SEG68/5	SEG69/4	SEG70/3	SEG71/2	SEG72/1	Segment / Common
Address	SGS=0	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	▪▪▪▪▪	43	44	45	46	47	(HEX)
	SGS=1	47	46	45	44	43	42	41	40	3F	3E	3D	3C	3B	3A	39	38	37	▪▪▪▪▪	04	03	02	01	00	
DB0		0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	▪▪▪▪▪	0/1	0/1	0/1	0/1	0/1	COMS1
DB1		0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	▪▪▪▪▪	0/1	0/1	0/1	0/1	0/1	
DB2		0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	▪▪▪▪▪	0/1	0/1	0/1	0/1	0/1	
DB3		0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	▪▪▪▪▪	0/1	0/1	0/1	0/1	0/1	
DB4		0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	▪▪▪▪▪	0/1	0/1	0/1	0/1	0/1	COMS2
DB5		0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	▪▪▪▪▪	0/1	0/1	0/1	0/1	0/1	
DB6		0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	▪▪▪▪▪	0/1	0/1	0/1	0/1	0/1	
DB7		0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	▪▪▪▪▪	0/1	0/1	0/1	0/1	0/1	

Note: The HD66725 can display addresses from 00H to 5FH.

Table 13 Relationship between Segment Driver Output Pin and Segment Display Function (HD66724)

When SGS = 0	When SGS = 1	Segment Output Control
SEG1/72, SEG4/69, SEG7/66, SEG10/63, SEG13/60, SEG16/57, SEG19/54, SEG22/51, SEG25/48, SEG28/45, SEG31/42, SEG34/39, SEG37/36, SEG40/33, SEG43/30, SEG46/27, SEG49/24, SEG52/21, SEG55/18, SEG58/15, SEG61/12, SEG64/9, SEG67/6, SEG70/3	SEG72/1, SEG69/4, SEG66/7, SEG63/10, SEG60/13, SEG57/16, SEG54/19, SEG51/22, SEG48/25, SEG45/28, SEG42/31, SEG39/34, SEG36/37, SEG33/40, SEG30/43, SEG27/46, SEG24/49, SEG21/52, SEG18/55, SEG15/58, SEG12/61, SEG9/64, SEG6/67, SEG3/70	Grayscale segment display allowed (Reflective color segment supported)
Output pins other than above	Output pins other than above	Segment blinking allowed

Table 14 Relationship between Segment Driver Output Pin and Segment Display Function (HD66725)

When SGS = 0	When SGS = 1	Segment Output Control
SEG1/96, SEG4/93, SEG7/90, SEG10/87, SEG13/84, SEG16/81, SEG19/78, SEG22/75, SEG25/72, SEG28/69, SEG31/66, SEG34/63, SEG37/60, SEG40/57, SEG43/54, SEG46/51, SEG49/48, SEG52/45, SEG55/42, SEG58/39, SEG61/36, SEG64/33, SEG67/30, SEG70/27, SEG73/24, SEG74/21, SEG79/18, SEG82/15, SEG85/12, SEG88/9, SEG91/6, SEG94/3	SEG96/1, SEG93/4, SEG90/7, SEG87/10, SEG84/13, SEG81/16, SEG78/19, SEG75/22, SEG72/25, SEG69/28, SEG66/31, SEG63/34, SEG60/37, SEG57/40, SEG54/43, SEG51/46, SEG48/49, SEG45/52, SEG42/55, SEG39/58, SEG36/61, SEG33/64, SEG30/67, SEG27/70, SEG24/73, SEG21/76, SEG18/79, SEG15/82, SEG12/85, SEG9/88, SEG6/91, SEG3/94	Grayscale segment display allowed (Reflective color segment supported)
Output pins other than above	Output pins other than above	Segment blinking allowed

Note: For details, see the Reflective Color Mark/Blink Mark Display section.

Table 15 Relationship between SEGRAM Data and Grayscale Control Segment Display

SEGRAM Data Setting				Effective Applied Voltage	SEGRAM Data Setting				Effective Applied Voltage
DB3	DB2	DB1	DB0	for COMS1 Segment	DB7	DB6	DB5	DB4	for COMS2 Segment
0	0	0	0	0 (Always unlit)	0	0	0	0	0 (Always unlit)
0	0	0	1	1 (Always lit)	0	0	0	1	1 (Always lit)
0	0	1	0	0.34 (Grayscale display)	0	0	1	0	0.34 (Grayscale display)
0	0	1	1	0.38 (Grayscale display)	0	0	1	1	0.38 (Grayscale display)
0	1	0	0	0.41 (Grayscale display)	0	1	0	0	0.41 (Grayscale display)
0	1	0	1	0.44 (Grayscale display)	0	1	0	1	0.44 (Grayscale display)
0	1	1	0	0.47 (Grayscale display)	0	1	1	0	0.47 (Grayscale display)
0	1	1	1	0.50 (Grayscale display)	0	1	1	1	0.50 (Grayscale display)
1	0	0	0	(Blink display) *1	1	0	0	0	(Blink display) *1
1	0	0	1	0.53 (Grayscale display)	1	0	0	1	0.53 (Grayscale display)
1	0	1	0	0.56 (Grayscale display)	1	0	1	0	0.56 (Grayscale display)
1	0	1	1	0.59 (Grayscale display)	1	0	1	1	0.59 (Grayscale display)
1	1	0	0	0.63 (Grayscale display)	1	1	0	0	0.63 (Grayscale display)
1	1	0	1	0.66 (Grayscale display)	1	1	0	1	0.66 (Grayscale display)
1	1	1	0	0.69 (Grayscale display)	1	1	1	0	0.69 (Grayscale display)
1	1	1	1	0.72 (Grayscale display)	1	1	1	1	0.72 (Grayscale display)

Note: Blinking is provided by repeatedly turning on the segment for 32 frames and turning it off for the next 32 frames.

Table 16 Relationship between SEGRAM Data and Blinking Control Segment Display (Blinking Control Segment Driver)

SEGRAM Data Setting				LCD Display Control for	SEGRAM Data Setting				LCD Display Control for
DB3	DB2	DB1	DB0	COMS1 Segment	DB7	DB6	DB5	DB4	COMS2 Segment
0	*[1]	*[1]	0	0 (Always unlit)	0	*[1]	*[1]	0	0 (Always unlit)
0	*[1]	*[1]	1	1 (Always lit)	0	*[1]	*[1]	1	1 (Always lit)
1	*[1]	*[1]	0	Blinking display	1	*[1]	*[1]	0	Blinking display
1	*[1]	*[1]	1	Double-speed blinking display	1	*[1]	*[1]	1	Double-speed blinking display

Notes: 1. 0 or 1.

2. Blinking is provided by repeatedly turning on the segment for 32 frames and turning it off for the next 32 frames.
3. Double-speed blinking is provided by repeatedly turning on the segment for 16 frames and turning it off for the next 16 frames.

Modifying Character Patterns

Character Pattern Development Procedure

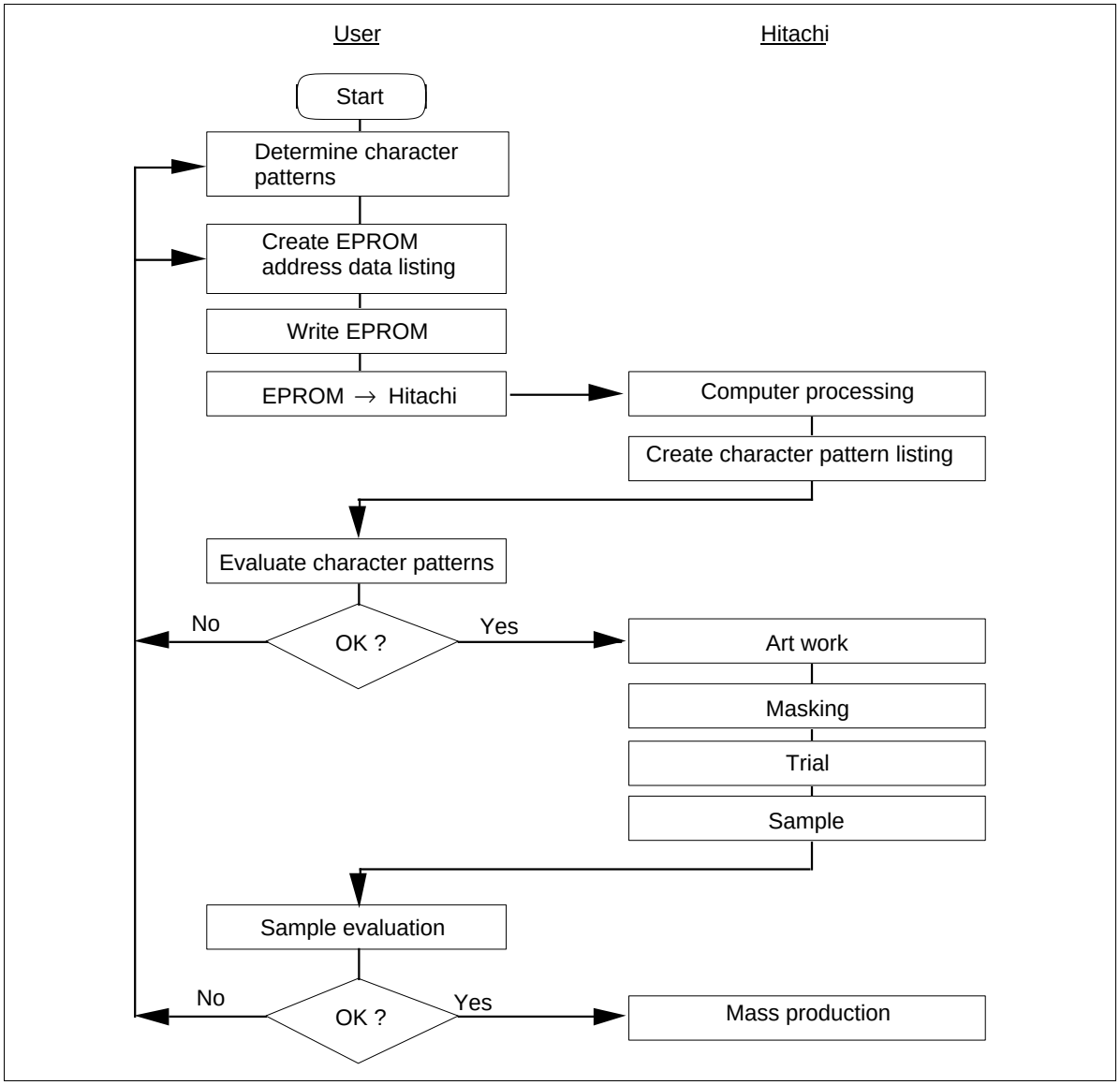


Figure 2 Character Pattern Development Procedure

The following operations correspond to the numbers listed in figure 2:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into an EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing of the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When the user confirms that the character patterns are correctly written, Hitachi will commence LSI mass production.

Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM.

Programming to EPROM: The HD66724/HD66725 character generator ROM can generate 432 6 × 8-dot character patterns. Table 17 shows the correspondence between the EPROM address, data, and the character pattern.

Table 17 Examples of Correspondence between EPROM Address, Data, and Character Pattern (6 × 8 Dots)

EPROM Address													Data						
													MSB						LSB
A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	1	0	1	1	0	0	1	0	0	0	0	0	1	0	0	0	1	
									0	0	0	1	0	1	0	0	0	1	
									0	0	1	0	0	1	0	0	0	1	
									0	0	1	1	0	0	1	0	1	0	
									0	1	0	0	0	0	0	1	0	0	
									0	1	0	1	0	0	0	1	0	0	
									0	1	1	0	0	0	0	1	0	0	
									0	1	1	1	0	0	0	0	0	0	

ROM bit — Character code — 0 — Line position

Notes:
1. EPROM address: Bit A12 corresponds to the CGROM memory bank switch bit ("ROM").
2. EPROM address: Bits A11 to A4 correspond to a character code.
3. EPROM address: Bits A2 to A0 specify the line position of the character pattern. EPROM address bit A3 must be set to 0.
4. EPROM data: Bits O5 to O0 correspond to character pattern data.
5. Areas which are lit (indicated by shading) are stored as 1, and unlit areas as 0.
6. The eighth raster-row is also stored in the CGROM, and must also be programmed. If the eighth raster-row is used for a cursor, this data must all be set to zero.
7. EPROM data: Bits O7 to O6 are invalid. 0 must be written in all bits.

Handling Unused Character Patterns:

1. EPROM data outside the character pattern area: This is ignored by character generator ROM for display operation so any data is acceptable.
2. EPROM data in CGRAM area: Always fill with zeros.
3. Treatment of unused user patterns in the HD66724/HD66725 EPROM: Depending on to the user application, these are handled in either of two ways:

a. When unused character patterns are not programmed: If an unused character code is written into DDRAM, all its dots are lit, because the EPROM is filled with 1s after it is erased.
b. When unused character patterns are programmed as 0s: Nothing is displayed even if unused character codes are written into DDRAM. (This is equivalent to a space.)

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66724/HD66725 can be controlled by the MPU. Before starting internal operation of the HD66724/HD66725, control information is temporarily stored in these registers to allow interfacing with various peripheral control devices or MPUs which operate at different speeds. The internal operation of the HD66724/HD66725 is determined by signals sent from the MPU. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signal (DB0 to DB7), make up the HD66724/HD66725 instructions. There are five categories of instructions that:

- Control the display
- Control power management
- Set internal RAM addresses
- Transfer data with the internal RAM
- Control key scan (when serial interface mode)

Normally, instructions that perform data transfer with the internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66724/HD66725 RAM addresses after each data write can lighten the MPU program load.

Because instructions other than clear display instruction are executed in 0 cycle, instructions can be written in succeccion.

While the clear display instruction is being executed for internal operation, or during reset, no instruction other than the key scan read instruction can be executed.

Instruction Descriptions

Key Scan Data Read

In the serial interface mode, the key scan data read instruction reads scan data in scan registers SCAN0 to SCAN3. Following transfer of the start byte, scan data read operation starts from scan register SCAN0 and proceeds in the order of SCAN1, SCAN2, and SCAN3. When data read from SCAN 0 to SCAN3 is completed, the operation starts from SCAN0 again. For details, see the Key Scan Control section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**1**	**0**	**1**	**1**	**SSE**	**SE2**	**SE1**	(SSE = 0)
								SE4	**SE3**	(SSE = 1)
0	0	**0**	**1**	**1**	**0**	**0**	**SQ2**	**SQ1**	**SQ0**	

Figure 3 Key Scan Data Read Instruction

Clear Display

The clear display instruction writes space code 20H (the character pattern for character code 20H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter. It also sets I/D to 1 (increment mode) in the entry mode set instruction. Since the execution of this instruction needs 85 clock cycles, do not send the next instruction during the execution time.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Figure 4 Clear Display Instruction

Return Home

The return home instruction sets DDRAM address 0 into the address counter. The DDRAM contents do not change. The cursor or blinking goes to the top left of the display.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

Figure 5 Return Home Instruction

Start Oscillation

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (Refer to the Standby Mode section.)

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**

Figure 6 Start Oscillation Instruction

Driver Output Control

CMS: Selects the output shift direction of a common driver. When CMS = "0", COM1/24 shifts to COM1, and COM24/1 to COM24. When CMS = "1", COM1/24 shifts to COM24, and COM24/1 to COM1. Output position of a common driver shifts depending on the CEN bit setting. For details, see the Display On/Off Control section.

SGS: Selects the output shift direction of a segment driver. When SGS = "0", SEG1/72 (96) shifts to SEG1, and SEG72 (96)/1 to SEG72 (96). When SGS = "1", SEG1/72 (96) shifts SEG72 (96), and SEG72 (96)/1 to SEG1.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**1**	**CMS**	**SGS**

Figure 7 Driver Output Control Instruction

Power Control

AMP: When AMP = 1, each voltage follower for the V1 to V5 pins and the booster are turned on. When AMP = 0, current consumption can be reduced when the display is not being used. In this case, set BT1/0 = 00 for single boosting output.

SLP: When SLP = 1, the HD66724/HD66725 enter the sleep mode, where the internal operations are halted except for the key scan function and the R-C oscillator, thus reducing current consumption. For details, refer to the Sleep Mode section. Only the following instructions can be executed during the sleep mode.

a. Key scan data read
b. Key scan control (IRE, KF1/0 bit)
c. Power control (AMP, SLP, and STB bits)
d. Port control (PT2-0 bits)

During the sleep mode, the other RAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66724/HD66725 enter the standby mode, where display operation and key scan completely stop, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. This setting can be used as the system wake-up, because an interrupt is generated when a specific key is pressed. For details, refer to the Standby Mode section. Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)
b. Voltage follower circuit on/off (AMP = 1/0)
c. Start oscillator
d. Key scan interrupt generation enabled/disabled (IRE = 1/0)
e. Port control (PT2-0 bits)

During the standby mode, the other RAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**1**	**AMP**	**SLP**	**STB**

Figure 8 Power Control Instruction

Contrast Control 1/2

SW: Switches the bit configuration for the contrast control instruction. SW = 0 corresponds to CT4 to CT0. SW = 1 corresponds to BT1/0 and BS2 to BS0.

CT4–CT0: When SW = 0 controls the LCD drive voltage (potential difference between V1 and GND) to adjust contrast. A 32-step adjustment is possible. For details, refer to the Contrast Adjuster section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**0**	**0**	**1**	**0**	**SW**	**CT4**	**CT3**	(SW = 0)
								BT1	**BT0**	(SW = 1)
0	0	**0**	**0**	**0**	**1**	**1**	**CT2**	**CT1**	**CT0**	(SW = 0)
							BS2	**BS1**	**BS0**	(SW = 1)

Figure 9 Contrast Control 1/2 Instruction

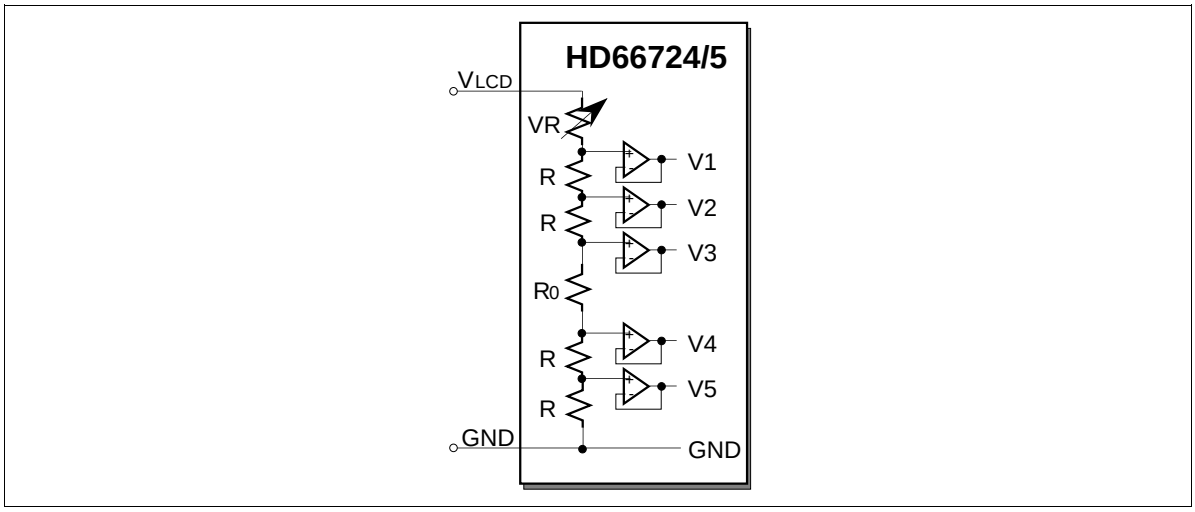


Figure 10 Contrast Adjuster

Table 18 CT Bits and Variable Resistor Value of Contrast Adjuster

CT Set Value					Variable	CT Set Value					Variable
CT4	CT3	CT2	CT1	CT0	Resistor (VR)	CT4	CT3	CT2	CT1	CT0	Resistor (VR)
0	0	0	0	0	3.2 x R	1	0	0	0	0	1.6 x R
0	0	0	0	1	3.1 x R	1	0	0	0	1	1.5 x R
0	0	0	1	0	3.0 x R	1	0	0	1	0	1.4 x R
0	0	0	1	1	2.9 x R	1	0	0	1	1	1.3 x R
0	0	1	0	0	2.8 x R	1	0	1	0	0	1.2 x R
0	0	1	0	1	2.7 x R	1	0	1	0	1	1.1 x R
0	0	1	1	0	2.6 x R	1	0	1	1	0	1.0 x R
0	0	1	1	1	2.5 x R	1	0	1	1	1	0.9 x R
0	1	0	0	0	2.4 x R	1	1	0	0	0	0.8 x R
0	1	0	0	1	2.3 x R	1	1	0	0	1	0.7 x R
0	1	0	1	0	2.2 x R	1	1	0	1	0	0.6 x R
0	1	0	1	1	2.1 x R	1	1	0	1	1	0.5 x R
0	1	1	0	0	2.0 x R	1	1	1	0	0	0.4 x R
0	1	1	0	1	1.9 x R	1	1	1	0	1	0.3 x R
0	1	1	1	0	1.8 x R	1	1	1	1	0	0.2 x R
0	1	1	1	1	1.7 x R	1	1	1	1	1	0.1 x R

BT1-0: When SW = 1, it switches the output of V5OUT between single, double, and triple boost. The liquid crystal display drive voltage level can be selected according to its drive duty ratio and bias. A lower amplification of the booster consumes less current.

BS2-0: When SW = 1, it sets the crystal display drive bias value within the range of 1/4 to 1/6.5 bias. The liquid crystal display drive bias value can be selected according to its drive duty ratio and voltage. For details, see the Liquid Crystal Display Drive Bias Selector Circuit section.

Table 19 BT Bits and Output Level

BT1	BT0	V5OUT Output Level
0	0	Single boost (no boost)
0	1	Double boost
1	0	Triple boost
1	1	Setting inhibited

Table 20 BS Bits and LCD Drive Bias Value

BS2	BS1	BS0	Liquid Crystal Display Drive Bias Value
0	0	0	1/6.5 bias drive
0	0	1	1/6 bias drive
0	1	0	1/5.5 bias drive
0	1	1	1/5 bias drive
1	0	0	1/4.5 bias drive
1	0	1	1/4 bias drive
1	1	0	Inhibit
1	1	1	Inhibit

Entry Mode Set

ROM: Switches the CGROM memory bank in the character mode (GR = 0). Uses bank 0 for display when ROM = 0 and bank 1 for display when ROM = 1. For details, see the CGROM Bank Switching Function section.

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into or read from DDRAM. The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to the writing and reading of CGRAM and SEGRAM.

GR: Activates the character mode when GR = 0. Displays the font pattern on CGROM or CGRAM according to the character code written in DDRAM. Activates the graphics mode when GR = 1. Displays a given pattern according to the bitmap data written in CGRAM. In this case, data in DDRAM is not used for display. Segment pattern display set to SEGRAM is enabled both in the character mode and graphics mode. For details, see the Graphics Display Function section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**1**	**0**	**0**	**ROM**	**I/D**	**GR**

Figure 11 Entry Mode Set Instruction

Cursor Control

B/W: When B/W is 1, the character at the cursor position is cyclically (every 32 frames) blink-displayed with black-white inversion.

When B/W = 1 and LC = 1, all characters including the cursor on the display line appear with black-white inversion. The characters do not blink. For details, refer to the Line-Cursor Display section.

C: The cursor is displayed on the 8th raster-row when C is 1. The 6-dot cursor is ORed with the character pattern and displayed on the 8th raster-row.

B: The character indicated by the cursor blinks when B is 1. The blinking is displayed as switching between all black dots and displayed characters every 32 frames. The cursor and blinking can be set to display simultaneously. When LC and B = 1, the blinking is displayed as switching between all white dots and displayed characters.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**1**	**0**	**1**	**B/W**	**C**	**B**

Figure 12 Cursor Control Instruction

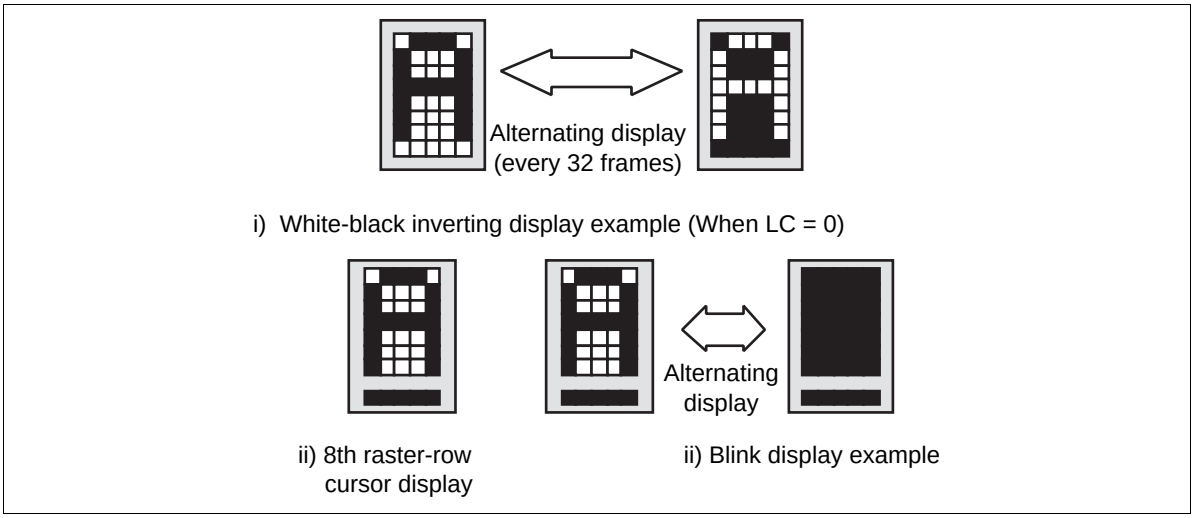


Figure 13 Cursor Control Examples

Display On/Off Control

D: Display is on when D is 1 and off when D is 0. When off, the display data remains in DDRAM, and can be displayed instantly by setting D to 1. When D is 0, the display is off with the SEG1 to SEG72 (96) outputs, COM1 to COM24 outputs, and COMS1/2 output set to the GND level and off. Because of this, the HD66724/HD66725 can control charging current for the LCD with AC driving.

CEN: Switches the common driver position from COM1 to COM8. When CEN = 1, it outputs the first line of COM1 to COM8 in the center of the screen. For details, see the Partial-Display-On Function section.

LC: When LC = 1, a cursor attribute is assigned to the line that contains the address counter (AC) value. Cursor mode can be selected with the B/W, C, and B bits. Refer to the Line-Cursor Display section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**1**	**1**	**0**	**D**	**CEN**	**LC**

Figure 14 Display On/Off Control Instruction

Table 21 Common Driver Pin Function

	Common Driver Pin Function			
	CEN = 0 (Normal Output)		CEN = 1 (Center Output)	
Common Driver Pin	CMS = 0 (Normal Display)	CMS = 1 (Inverted Display)	CMS = 0 (Normal Display)	CMS = 1 (Inverted Display)
COM1/24	COM1	COM24	COM17	COM16
COM2/23	COM2	COM23	COM18	COM15
COM3/22	COM3	COM22	COM19	COM14
COM4/21	COM4	COM21	COM20	COM13
COM5/20	COM5	COM20	COM21	COM12
COM6/19	COM6	COM19	COM22	COM11
COM7/18	COM7	COM18	COM23	COM10
COM8/17	COM8	COM17	COM24	COM9
COM9/16	COM9	COM16	COM1	COM8
COM10/15	COM10	COM15	COM2	COM7
COM11/14	COM11	COM14	COM3	COM6
COM12/13	COM12	COM13	COM4	COM5
COM13/12	COM13	COM12	COM5	COM4
COM14/11	COM14	COM11	COM6	COM3
COM15/10	COM15	COM10	COM7	COM2
COM16/9	COM16	COM9	COM8	COM1
COM17/8	COM17	COM8	COM9	COM24
COM18/7	COM18	COM7	COM10	COM23
COM19/6	COM19	COM6	COM11	COM22
COM20/5	COM20	COM5	COM12	COM21
COM21/4	COM21	COM4	COM13	COM20
COM22/3	COM22	COM3	COM14	COM19
COM23/2	COM23	COM2	COM15	COM18
COM24/1	COM24	COM1	COM16	COM17
COM1/2	COMS1	COMS2	COMS1	COMS2
COM2/1	COMS2	COMS1	COMS2	COMS1

Display Line Control

NL2-0: Specifies the display lines. Display lines change the liquid crystal display drive duty ratio. DDRAM address mapping does not depend on the number of display lines.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**1**	**1**	**1**	**NL2**	**NL1**	**NL0**

Figure 15 Display Line Control Instruction

Table 22 NL Bits and Display Lines

NL2	NL1	NL0	Display Lines	Liquid Crystal Display Drive Duty Ratio	Common Driver Used
0	0	0	Segment display	1/2 Duty	COMS1, COMS2
0	0	1	One character line + segment display	1/10 Duty	COM1-8, COMS1, COMS2
0	1	0	Two character lines + segment display	1/18 Duty	COM1-16, COMS1, COMS2
0	1	1	Three character lines + segment display	1/26 Duty	COM1-24, COMS1, COMS2
1	*	*	Setting inhibited		

Double-Height Display Control

DL3-1: Specifies the double-height display for a given line. When DL1 = 1, the first line is displayed at double height. When DL2 = 1, the second line is displayed at double height. When DL3 = 1, the third line is displayed at double height. Double-height display of multiple lines is possible. For details, see the Double-Height Display section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**1**	**0**	**0**	**0**	**DL3**	**DL2**	**DL1**

Figure 16 Double-Height Display Control Instruction

Vertical Scroll Control 1/2

SN2-0: Specifies the display start line output from COM1. Because DDRAM is assigned a 5-line display area, data is displayed sequentially from the first line to the fifth line then repeated from the first line again.

SL2–0: Selects the top raster-row to be displayed (display-start raster-row) in the display-start line specified by SN2 to SN0. Any raster-row from the first to eighth can be selected (Table 24). This function

is used to achieve vertical smooth scrolling together with SN2 to SN0. For details, refer to the Vertical Smooth Scroll section. During horizontal scrolling, the SN0 bit must be 0 (SN0 = 0).

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**1**	**0**	**0**	**1**	**SN2**	**SN1**	**SN0**
0	0	**0**	**1**	**0**	**1**	**0**	**SL2**	**SL1**	**SL0**

Figure 17 Vertical Scroll Control 1/2 Instruction

Table 23 SN Bits and Display-Start Lines

SN2	SN1	SN0	Display-Start Line
0	0	0	1st line
0	0	1	2nd line
1	1	0	3rd line
1	1	1	4th line
1	0	0	5th line
1	0	1	Setting inhibited
1	1	0	Setting inhibited
1	1	1	Setting inhibited

Table 24 SL Bits and Display-Start Raster-Row

SL2	SL1	SL0	Display-Start Raster-Row
0	0	0	1st raster-row
0	0	1	2nd raster-row
0	1	0	3rd raster-row
0	1	1	4th raster-row
1	0	0	5th raster-row
1	0	1	6th raster-row
1	1	0	7th raster-row
1	1	1	8th raster-row

Horizontal Scroll Control

SSE: When SSE = 0, it selects SE2 and SE1 bits and when SSE = 1, it selects SE3 and SE4 bits.

SE3-1: Specifies the horizontal smooth scroll display for a given line. When SE = 1, the first line is displayed in a horizontal scroll. When SE = 1, the second line is displayed in a horizontal scroll. When SE = 1, the third line is displayed in a horizontal scroll. When SE = 4, the fourth line is displayed in a horizontal scroll. Horizontal scroll display of multiple lines is possible.

SQ2-0: Shifts the line to which horizontal smooth scroll is specified by units of 3 dots, up to 21 dots, to the left. For details, see the Horizontal Smooth Scroll section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**1**	**0**	**1**	**1**	**SSE**	**SE2**	**SE1**	(SSE = 0)
								SE4	**SE3**	(SSE = 1)
0	0	**0**	**1**	**1**	**0**	**0**	**SQ2**	**SQ1**	**SQ0**	

Figure 18 Horizontal Scroll Control Instruction

Table 25 SQ Bits and Display Start Line

SQ2	SQ1	SQ0	Display Start Line
0	0	0	Displayed with no shift
0	0	1	Displayed with 3 dots shifted to the left
0	1	0	Displayed with 6 dots shifted to the left
0	1	1	Displayed with 9 dots shifted to the left
1	0	0	Displayed with 12 dots shifted to the left
1	0	1	Displayed with 15 dots shifted to the left
1	1	0	Displayed with 18 dots shifted to the left
1	1	1	Displayed with 21 dots shifted to the left

Key Scan Control

IRE: When IRE = 1, it permits interrupts when a key is pressed. This causes interrupts to occur in the standby period when the oscillator clock is halted, as well as key scan interrupts during normal operation, allowing system wake-up.

KF1-0: Sets the key scan cycle. The following table shows the key scan pulse width and key scan cycle used when the oscillation frequency (fosc) is 32 kHz, which depend on the oscillation frequency. For details, see the Key Scan Control section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**1**	**1**	**0**	**1**	**IRE**	**KF1**	**KF0**

Figure 19 Key Scan Control Instruction

Table 26 KF Bits and Key Scan Cycle

KF1	KF0	Key Scan Pulse Width	Key Scan Cycle
0	0	0.25 ms	1.0 ms (32 clock cycles)
0	1	0.5 ms	2.0 ms (64 clock cycles)
1	0	1.0 ms	4.0 ms (128 clock cycles)
1	1	2.0 ms	8.0 ms (256 clock cycles)

Note: The data is a value obtained when the oscillation frequency (fosc) is 32 kHz. The value depends on the oscillation frequency.

Port Control

PT2-0: Controls the output level of a port output pin (PORT2-PORT0). When PT0 = 0, it specifies the POT0 output to GND and when PT0 = 1, to VCC. Similarly, PT1 and PT2 bits control PORT1 and PORT2 output levels respectively.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**1**	**1**	**1**	**0**	**PT2**	**PT1**	**PT0**

Figure 20 Port Control Instruction

RAM Address Set

RM1-0: Selects DDRAM, CGRAM, and SEGRAM. The selected RAM is accessed with this setting.

AD9-0: Initially sets RAM addresses to the address counter (AC). Once RAM data is accessed, the AC is automatically updated according to the I/D bit. This allows consecutive accesses without resetting addresses. RAM address setting is not allowed in the sleep mode or standby mode.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**1**	**0**	**RM1**	**RM0**	**AD9**	**AD8**	**AD7**	**AD6**
0	0	**1**	**1**	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**

Figure 21 RAM Address Set Instruction

Table 27 RM Bits and RAM Selection

RM1	RM0	RAM Selection
0	0	DDRAM
0	1	Setting inhibited
1	0	CGRAM
1	1	SEGRAM

Table 28 AD Bits and DDRAM Setting

RM1/0	AD9-AD0	DDRAM Setting
00	"000"H-"00F"H	Character code on the 1st line
00	"010"H-"01F"H	Character code on the 2nd line
00	"020"H-"02F"H	Character code on the 3rd line
00	"030"H-"03F"H	Character code on the 4th line
00	"040"H-"04F"H	Character code on the 5th line

Table 29 AD Bits and CGRAM Setting (GR = 0)

RM1/0	AD9-AD0	CGRAM (1) Setting in the Character Display Mode (GR = 0)
10	"000"H-"05F"H	Font pattern of CGRAM characters (1) to (16)
10	"100"H-"15F"H	Font pattern of CGRAM characters (17) to (32)
10	"200"H-"25F"H	Font pattern of CGRAM characters (33) to (48)
10	"300"H-"35F"H	Font pattern of CGRAM characters (49) to (64)

Table 30 AD Bits and CGRAM Setting (GR = 1)

RM1/0	AD9-AD0	CGRAM (1) (2) Setting in the Graphics Display Mode (GR = 1)
10	"000"H-"05F"H	Bitmap data for COM1 to COM8
10	"100"H-"15F"H	Bitmap data for COM9 to COM16
10	"200"H-"25F"H	Bitmap data for COM17 to COM24
10	"300"H–"35F"H	Bitmap data for COM25 to COM32

Table 31 AD Bits and SEGRAM Setting

RM1/0	AD9-AD0	SEGRAM Setting
11	"000"H-"05F"H	SEGRAM display data

Write Data to RAM

WD7-0 : Writes 8-bit data to DDRAM and CGRAM lower 2-bit data to SEGRAM. DDRAM/ CGRAM/ SEGRAM is selected by the previous specification of the RM 1/0bit. After a write, the address is automatically incremented or decremented by 1 according to the I/D bit setting in the entry mode set instruction. During the sleep and standby modes, DDRAM, CGRAM, or SEGRAM cannot be accessed.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	**WD7**	**WD6**	**WD5**	**WD4**	**WD3**	**WD2**	**WD1**	**WD0**

Figure 22 Write Data to RAM Instruction

Read Data from RAM

RD7-0 : Reads the 8-bit data from DDRAM, CGRAM or SEGRAM. DDRAM/CGRAM/SEGRAM is selected by the previous specification of the RM 1/0 bit. In the parallel bus interface mode, the first-byte data read will be invalid immediately after the RAM address is set, and the subsequent second-byte data will be read normally. In the serial interface mode, two bytes will be invalid immediately after the start byte, and the subsequent third-byte data will be read normally. For details, see the Serial Data Transfer section. After a DDRAM read, the address is automatically incremented or decremented by 1 according to the I/D bit setting in the entry mode set instruction.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	**RD7**	**RD6**	**RD5**	**RD4**	**RD3**	**RD2**	**RD1**	**RD0**

Figure 23 Read Data from RAM Instruction

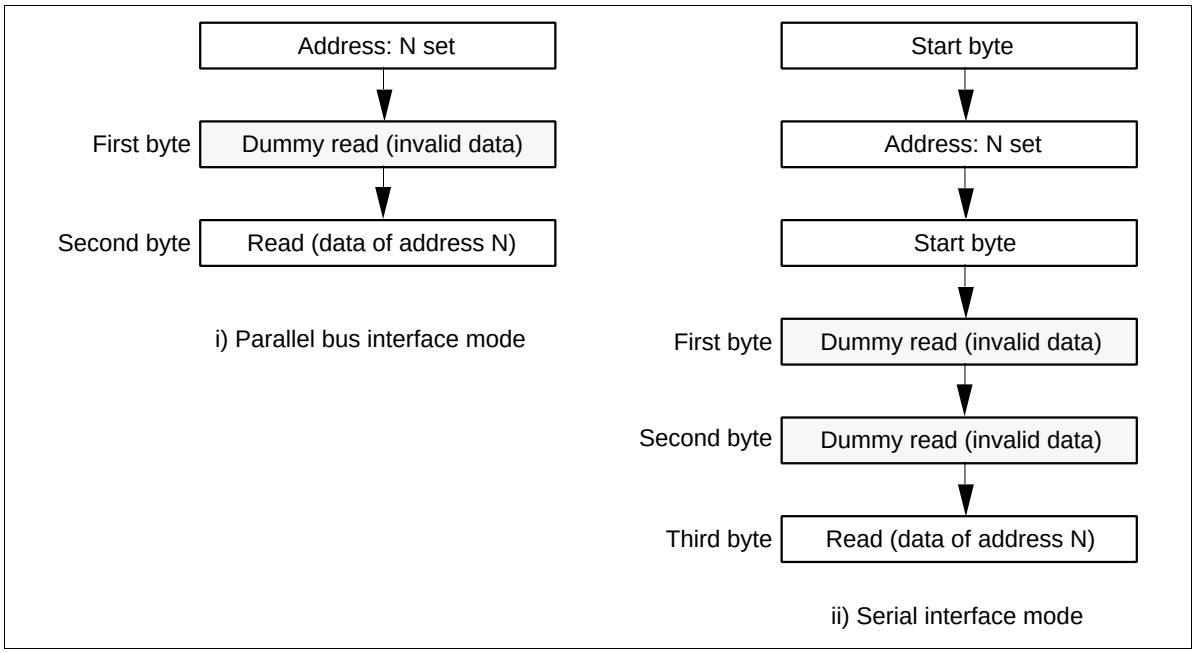


Figure 24 RAM Read Sequence

Table 32 Instruction List

Register Name	Code										Description	Execution Cycle *1
	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Key scan data read	1	0				KSD					Reads key scan data (KSD).	0
No operation	0	0	0	0	0	0	0	0	0	0	No operation (NOP).	0
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets address 0 into the address counter.	85
Return home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM address 0 into the address counter.	0
Start oscillator	0	0	0	0	0	0	0	0	1	1	Starts the oscillation standby mode.	—
Driver output control	0	0	0	0	0	0	0	1	CMS	SGS	Selects the common driver shift direction (CMS) and segment driver shift direction (SGS).	0
Power control	0	0	0	0	0	0	1	AMP	SLP	STB	Turns on LCD power supply (AMP), and sets the sleep mode (SLP) and standby mode (STB).	0
Contrast control 1	0	0	0	0	0	1	0	SW	CT4	CT3	Sets the register selection (SW), upper contrast adjustment bits (CT4-3) or boost level (BT1/0).	0
									BT1	BT0		
Contrast control 2	0	0	0	0	0	1	1	CT2	CT1	CT0	Sets the lower contrast adjustment bits (CT2-0) or LCD bias value (BS2-0).	0
								BS2	BS1	BS0		
Entry mode set	0	0	0	0	1	0	0	ROM	I/D	GR	Sets the CGROM memory bank switching (ROM), address update direction after RAM access (I/D), and graphics mode (GR).	0
Cursor control	0	0	0	0	1	0	1	B/W	C	B	Sets black-white inverting cursor (B/W), 8th raster-row cursor (C), and blink cursor (B).	0
Display on/off control	0	0	0	0	1	1	0	D	CEN	LC	Sets display on (D), centers the screen (CEN), and displays the line cursor (LC).	0
Display line control	0	0	0	0	1	1	1	NL2	NL1	NL0	Sets the number of display lines (NL2-0).	0
Double-height display control	0	0	0	1	0	0	0	DL3	DL2	DL1	Specifies double-height display lines (DL3-1).	0
Vertical scroll control 1	0	0	0	1	0	0	1	SN2	SN1	SN0	Sets the display-start line (SN2-0).	0
Vertical scroll control 2	0	0	0	1	0	1	0	SL2	SL1	SL0	Sets the display-start raster-row (SL2-0).	0

Table 31 Instruction List (cont)

Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle *1
Horizontal scroll control 1	0	0	0	1	0	1	1	SSE	SE2	SE1	Specifies SE1-4 bit selection (SSE) and the display line where horizontal scroll is applied (SE1-4).	0
									SE4	SE3		
Horizontal scroll control 2	0	0	0	1	1	0	0	SQ2	SQ1	SQ0	Specifies the amount of scroll dot shift (SQ2-0) in horizontal smooth scroll.	0
Key scan control	0	0	0	1	1	0	1	IRE	KF1	KF0	Sets the key scan interrupt (IRE) and key scan cycle (KF1/0).	0
Port control	0	0	0	1	1	1	0	PT2	PT1	PT0	Sets the general port output (PT2-0).	0
RAM address set (upper bits)	0	0	1	0	RM1	RM0	AD9-6 (upper bits)				Sets the RAM selection (RM1/0) and initial higher RAM address to the address counter (AC).	0
RAM address set (lower bits)	0	0	1	1	AD5-0 (lower bits)						Sets the initial higher RAM address to the address counter (AC).	0
Write data to RAM	0	1	Write data								Writes data to DDRAM, CGRAM, or SEGRAM.	0
Read data from RAM	1	1	Read data								Reads data from DDRAM, CGRAM, or SEGRAM.	0

Note: 1. Represented by the number of operating clock pulses; the execution time depends on the supplied clock frequency or the internal oscillation frequency.

Bit definition:

CMC = 0: COM1/24 => COM1
SGS = 0: SEG1/72 => SEG1
AMP = 1: Operational amplifier and booster circuit on
SLP = 1: Sleep mode
STB = 1: Standby mode
SW = 0: CT4-0 access/SW = 1: BT1/0 and BS2-0 access
CT4-0: Contrast adjustment
BT1/0: Boost level selection (00: Single, 01: Double, 10: Triple)
BS2-0: LCD drive bias selection
ROM = 0: CGROM bank 0 selection/ROM = 1: CGROM bank 1 selection
ID = 1: Address increment
ID = 0: Address decrement
GR = 1: Graphics display mode
GR = 0: Character display mode
B/W = 1: Black-white inverting cursor on

C = 1: 8th raster-row cursor on

B = 1: Blink cursor on

D = 1: Display on

CEN = 1: Centering COM1-8

LC = 1: Cursor display for the all display lines including AC

NL2-0: Display line setting (000: 1/2 duty ratio, 001: 1/10 duty ratio, 010: 1/18 duty ratio, 011: 1/26 duty ratio)

DL3-1: Double-height line specifications (DL1: 1st line, Dl2: 2nd line, Dl3: 3rd line)

SN2-0: Display-start line (000: 1st line, 001: 2nd line, 010: 3rd line, 011: 4th line, 100: 5th line)

SL2-0: Display-start raster-row specifications (000: 1st raster-row...111: 8th raster-row)

SSE: SE1-4 bit selection (SSE = 0: SE1/2 bit selection, SSE = 1: SE3/4 bit selection)

SE1-4: Horizontal smooth scroll display line specifications (SE1 = 1: 1st line, SE2 = 1: 2nd line, SE3 = 1: 3rd line, SE4 = 1: 4th line)

SQ2-0: Horizontal scroll dots specifications (000: 0-dot shift...111: 21-dot shift)

IRE = 1: Key scan interrupt generation enabled

KF1/0: Key scan cycle set

PT2-0: Port output control (PT2 = 1: PORT2 = Vcc, PT1 = 1: PORT1 = Vcc, PT0 = 1: PORT0 = Vcc)

RM1/0: RAM selection (00/01: DDRAM, 10: CGRAM, 11: SEGRAM)

ADD9-0: DDRAM/CGRAM/SEGRAM address set (DDRAM: 000H-04FH, CGRAM: 000H-35FH, SEGRAM: 000H-047H)

Reset Function

The HD66724/HD66725 are internally initialized by RESET input. During initialization, the system executes a clear display instruction after reset is canceled. The system executes the other instructions during the reset period. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period and execution of the clear display instruction following reset cancellation, no instruction or RAM data access from the MPU is accepted. Here, reset input must be held back for at least 1 ms, and an issuing instruction must wait for 1,000 clock cycles after reset is canceled because the display clearing continues after reset cancellation.

Instruction Set Initialization:

1. Clear display executed (Writes 20H to DDRAM)
2. Return home executed (Sets the address counter (AC) to 00H to select DDRAM)
3. Start oscillator executed
4. Driver output control (SGS = 0, CMS = 0)
5. Power control (AMP = 0: LCD power off, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
6. Single boost (BT1/0 = 00), 1/6.5 bias drive (BS2/1/0 = 000), Weak contrast (CT4-0 = 00000)
7. Entry mode set (ROM = 0: CGROM bank 0, I/D = 1: Increment by 1, GR = 0: Character display mode)
8. Cursor display off (B/W = 0, C = 0, B = 0)
9. Display on/off control (D = 0: Display off, CEN = 0: Normal position, LC = 0: Line-cursor off)
10. Display control (NL2/1/0 = 100: 1/34 duty ratio)
11. Double-height display off (DL3/2/1 = 000)
l2. Vertical scroll control (SN2/1/0 = 000: First line displayed at the top, SL2/1/0: First raster-row displayed at the top of the first line)
13. Horizontal scroll off (SEE = 0, SE2/1 = 00, SE4/3 = 00, SQ2/1/0 = 000)
14. Key scan control (IRE = 0: Key scan interrupt (IRQ) generation disabled, KF1/0 = 00: Key scan set to 32 cycles)
15. Port control (PT2/1/0 = 000: PORT2/1/0 output = GND level)

RAM Data Initialization:

1. DDRAM
   All addresses are initialized to 20H by the clear display instruction after the reset is canceled.
2. CGRAM/SEGRAM
   This is not automatically initialized by reset input but must be initialized by software while display is off (D = 0)

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Outputs GND level
2. Booster output pins (VLOUT): Outputs GND level
3. Oscillator output pin (OSC2): Outputs oscillation signal
4. Key strobe pins (KST0 to KST3): KST0 outputs GND level. KST1 to KST3 output V_{CC} level.
5. Key scan interrupt pin (IRQ*): Outputs V_{CC} level
6. General output port (PORT0–PORT2): Outputs GND level

Serial Data Transfer

Setting the IM1 and IM2 pins (interface mode pins) to the GND level allows standard clock-synchronized serial data transfer, using the chip select line (CS*), serial data line (SDA), and serial transfer clock line (SCL). For a serial interface, the IM0/ID pin function uses an ID pin.

The HD66724/HD66725 initiate serial data transfer by transferring the start byte at the falling edge of CS* input. They end serial data transfer at the rising edge of CS* input.

The HD66724/HD66725 are selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66724/HD66725. The HD66724/HD66725, when selected, receive the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66724/HD66725 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, an instruction can be issued or key scan data can be read, and when RS = 1, the data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit) as shown in table 33.

After receiving the start byte, the HD66724/HD66725 receive or transmit the subsequent data byte-by-byte. The data is transferred with the MSB first. To transfer the data consecutively, note that only the display-clear instruction requires a longer execution time than the others (table 32).

Two bytes of the RAM read data after the start byte are invalid. The HD66724/HD66725 start to read the correct RAM data from the third byte. Write a dummy instruction ("00H") before reading the key scan data.

Table 33 Start Byte Format

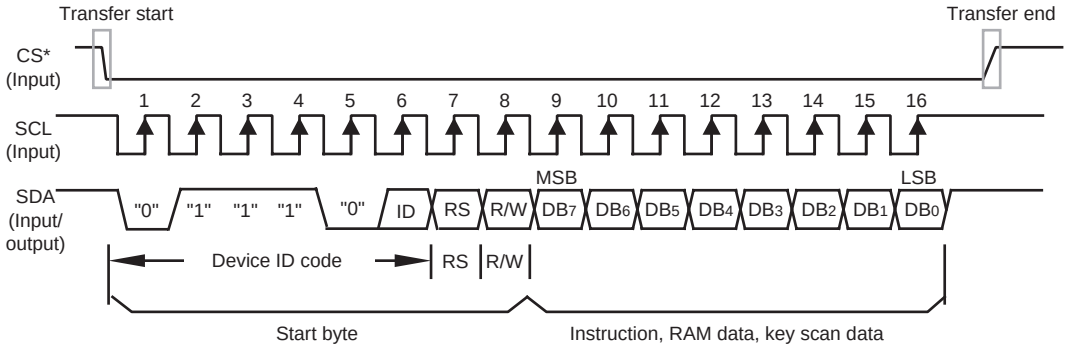
Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

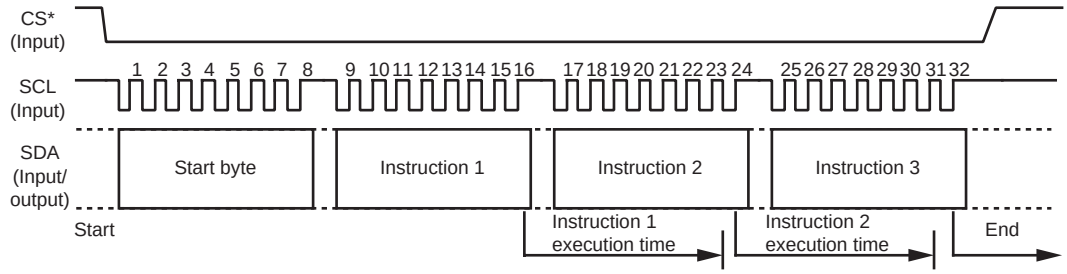
Table 34 RS and R/W Bit Function of Clock-Synchronized Serial Interface Data

RS	R/W	Function
0	0	Writes instruction
0	1	Reads key scan data
1	0	Writes RAM data
1	1	Reads RAM data

a) Basic Data-Transfer Timing through Clock-Synchronized Serial Bus Interface

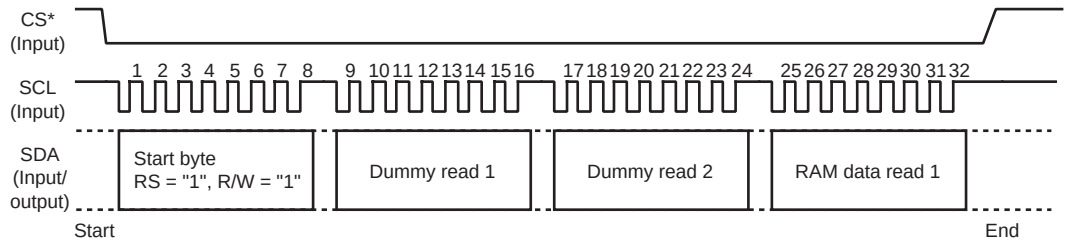


b) Consecutive Data-Transfer Timing through Clock-Synchronized Serial Bus Interface



Note: When instruction 1 is a clear display instruction, adjust the transfer rate so that the 8th bit of instruction 2 is transferred after execution of the clear display instruction.

c) RAM Data Read-Transfer Timing



Note: Two bytes of RAM read data after the start byte are invalid. The HD66724/HD66725 start to read correct RAM data from the third byte.

Figure 25 Clock-Synchronized Serial Interface Timing Sequence

Key Scan Control

The key matrix scanner senses and holds the key states at each rising edge of key strobe signals (KST) that are output by the HD66724/HD66725. The key strobe signals are output as time-multiplexed signals from KST0 to KST3. After passing through the key matrix, these strobe signals are used to sample the key state of eight inputs KIN0 to KIN7, enabling up to 32 keys to be scanned.

The states of inputs KIN0 to KIN7 are sampled by key strobe signal KST0 and latched into the SCAN0 register. Similarly, the data sampled by strobe signals KST1 to KST3 is latched into the SCAN1 to SCAN3 registers, respectively. Key pressing is stored as 1 in these registers.

The generation cycle and pulse width of the key strobe signals depend on the operating frequency (oscillation frequency) of the HD66724/HD66725 and the key scan cycle determined by the KF0 and KF1 bits. For example, when the operating frequency is 32 kHz and KF0 and KF1 are both 10, the generation cycle is 4.0 ms and the pulse width is 1.0 ms. When the operating frequency (oscillation frequency) is changed, the above generation cycle and the pulse width are changed in inverse proportion.

In order to compensate for the mechanical features of the keys, such as chattering and noise and for the key-strobe generation cycle and the pulse width of the HD66724/HD66725, software should read the scanned data two to three times in succession to obtain valid data. Multiple keypress combinations should also be processed in the software.

Up to three keys can be pressed simultaneously. Note, however, that if the third key is pressed on the intersection between the rows and columns of the first two keys pressed, incorrect data will be sampled. For three-key input, the third key must be on a separate column or row.

The input pins KIN0 to KIN7 are pulled up to V_{CC} with internal MOS transistors (see the Electrical Characteristics section). External resistors may also be required to further pull the voltages up when the internal pull-ups are insufficient for the desired noise margins or for a large key matrix.

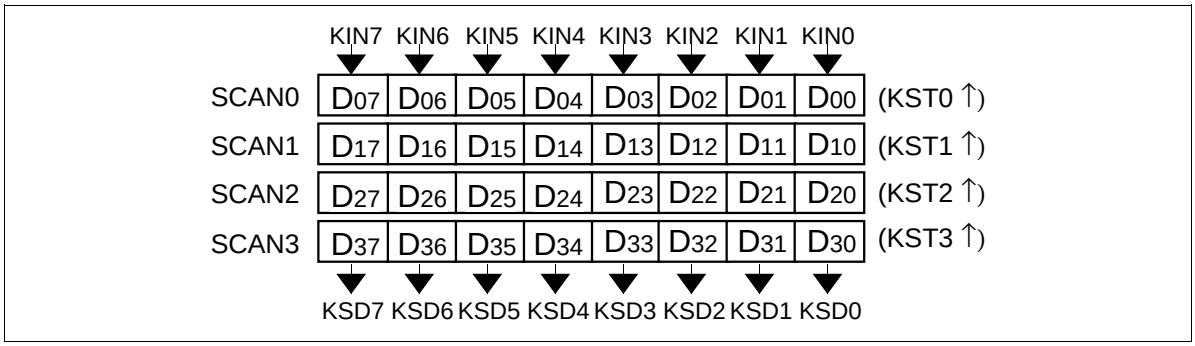


Figure 26 Key Scan Register Configuration

Table 35 Key Scan Cycles for Each Operating Frequency

KF1	KF0	Key Scan Pulse Width	Key Scan Cycle
0	0	0.25 ms	1.0 ms (32 clock cycles)
0	1	0.5 ms	2.0 ms (64 clock cycles)
1	0	1.0 ms	4.0 ms (128 clock cycles)
1	1	2.0 ms	8.0 ms (256 clock cycles)

Note: The data is a value obtained when the oscillation frequency (fosc) is 32 kHz. The value depends on the oscillation frequency.

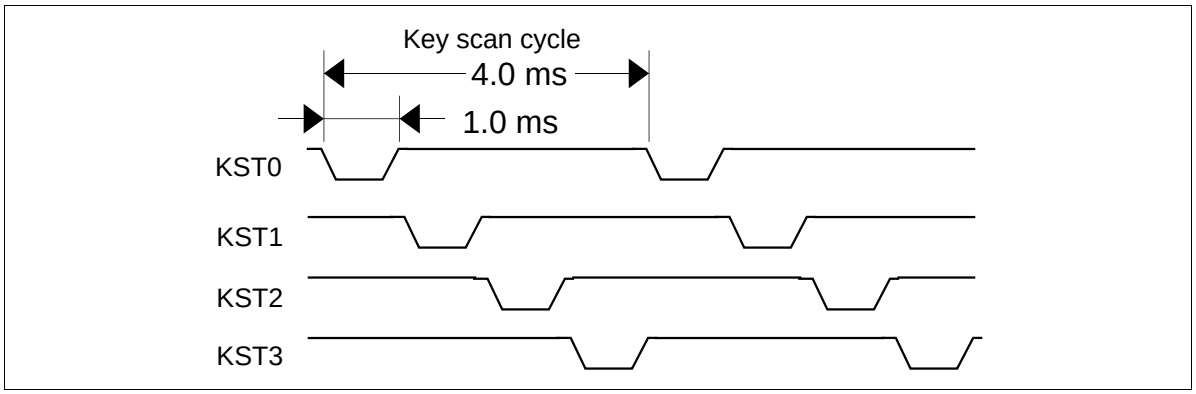


Figure 27 Key Strobe Output Timing (KF1/0 = 10, fcp/fosc = 32 kHz)

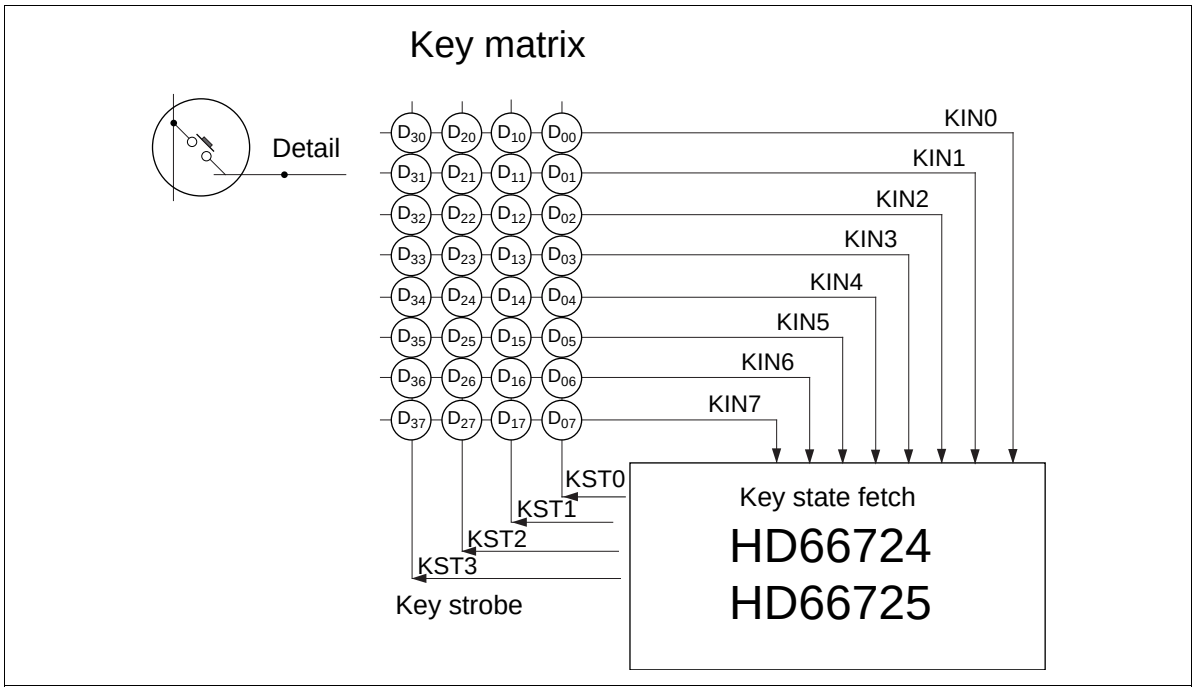


Figure 28 Key Scan Configuration

The key scan data can be read by an MPU via a serial interface. First, a start byte should be transferred. After the HD66724/HD66725 have received the start byte, the MPU reads scan data KSD7 to KSD0 from the SCAN0 register starting from the MSB. Similarly, the MPU reads the data from SCAN1, SCAN2 and SCAN3 in that order. After reading SCAN3, the MPU starts reading at SCAN0 again.

The HD66724/HD66725 may be read out while they are latching scan data and are thus unstable. Consequently, they should also be reconfirmed with software if required.

Write a dummy instruction ("00H") before reading the key scan data.

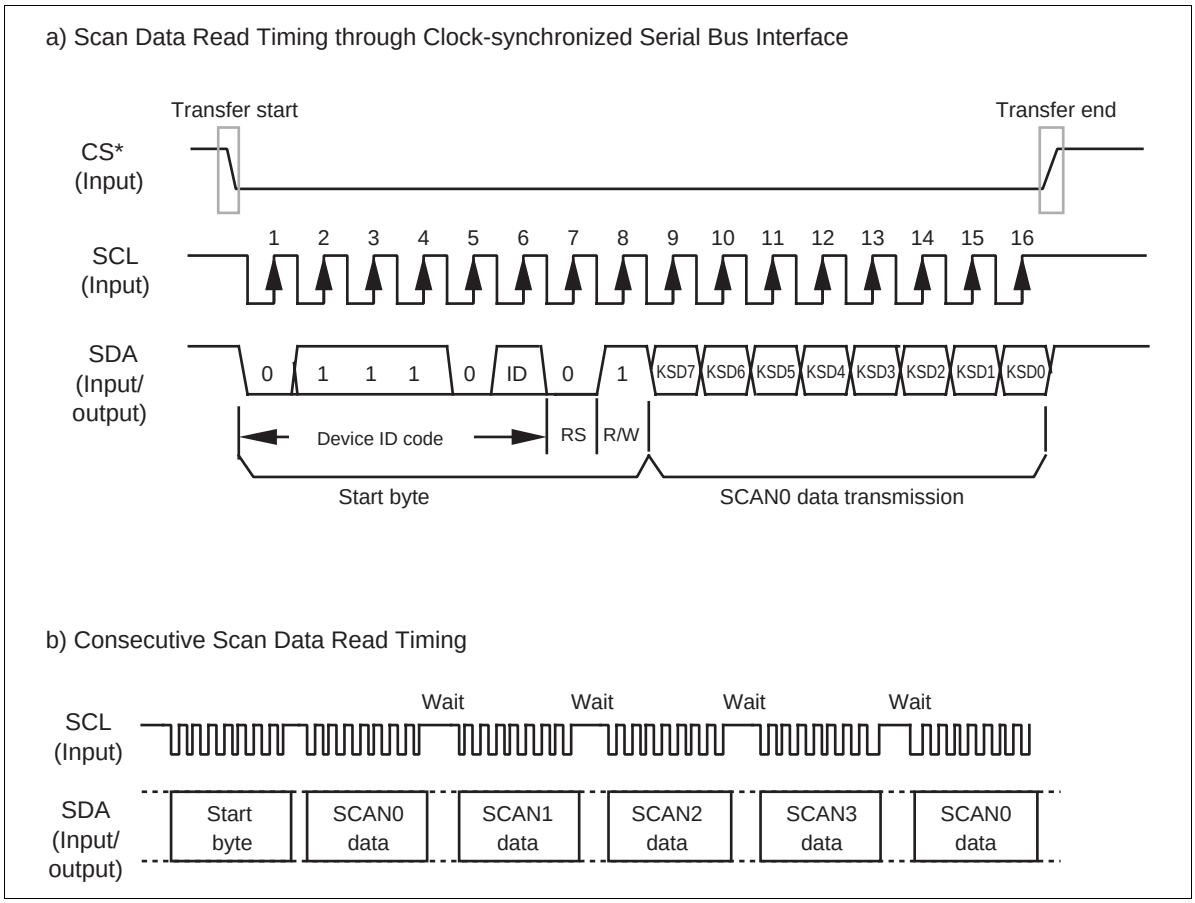


Figure 29 Scan Data Serial Transfer Timing

Key Scan Interrupt (Wake-Up Function)

If the interrupt enable bit (IRE) is set to 1, the HD66724/HD66725 send an interrupt signal to the MPU on detecting that a key has been pressed in the key scan circuit by setting the IRQ* output pin to a low level. An interrupt signal can be generated by pressing any key in a 32-key matrix. The interrupt level continues to be output during the key scan cycle during which the key is being pressed.

Normal key scanning is performed and interrupts can occur in the HD66724/HD66725 sleep mode (SLP = 1). Accordingly, power consumption can be minimized in the sleep mode, by triggering the MPU to read key states via the interrupt which is generated only when the HD66724/HD66725 detect a key input. For details, refer to the Sleep Mode section.

On the other hand, normal key scanning and the internal operating clock stop in the standby mode (STB = 1). During this period, the KST0 output is kept low, so the HD66724/HD66725 can always monitor eight key inputs (KIN0-KIN7) connected to KST0 when RS = GND. Therefore, if any of the eight keys is pressed, an interrupt occurs. When RS = Vcc, all outputs KST0 to KST3 are kept low, so the HD66724/HD66725 can always monitor 32 key inputs. If any of 32 keys is pressed, an interrupt occurs. Accordingly, power consumption can further be minimized in the standby mode, where the whole system is inactive, by triggering the MPU via the interrupt which is generated only when the HD66724/HD66725 detect a key input from the above keys. For details, refer to the Standby Mode section.

The IRQ* output pin is pulled up to the V_{CC} with an internal MOS resistor of approximately 50 kΩ. Additional external resistors may be required to obtain stronger pull-ups. Interrupts may occur if noise occurs in KIN0-KIN7 input during key scanning. Interrupts must be inhibited if not needed by setting the interrupt enable bit (IRE) to 0.

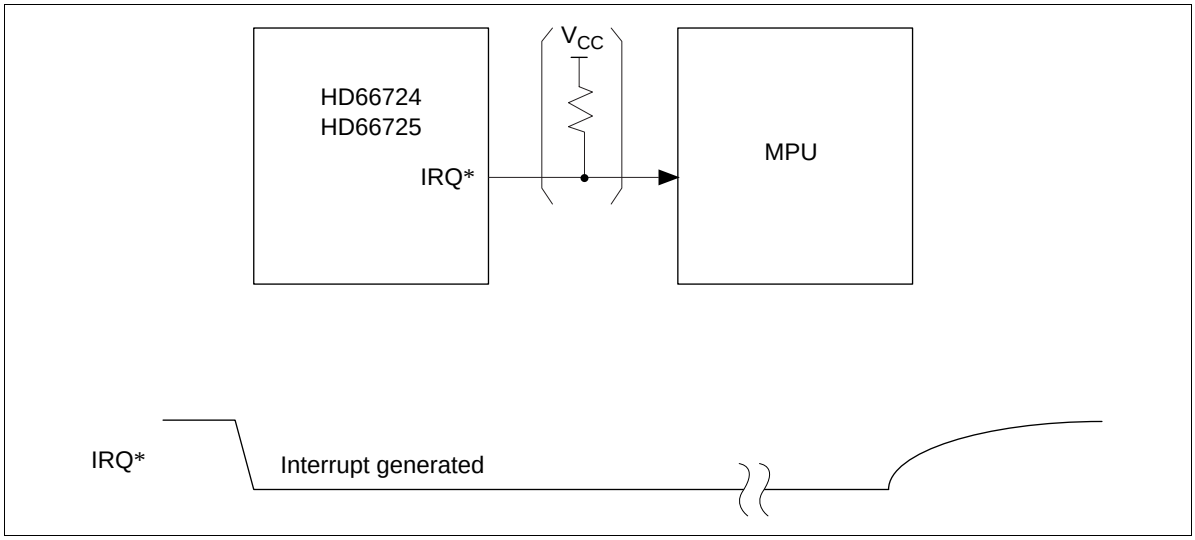


Figure 30 Interrupt Generation

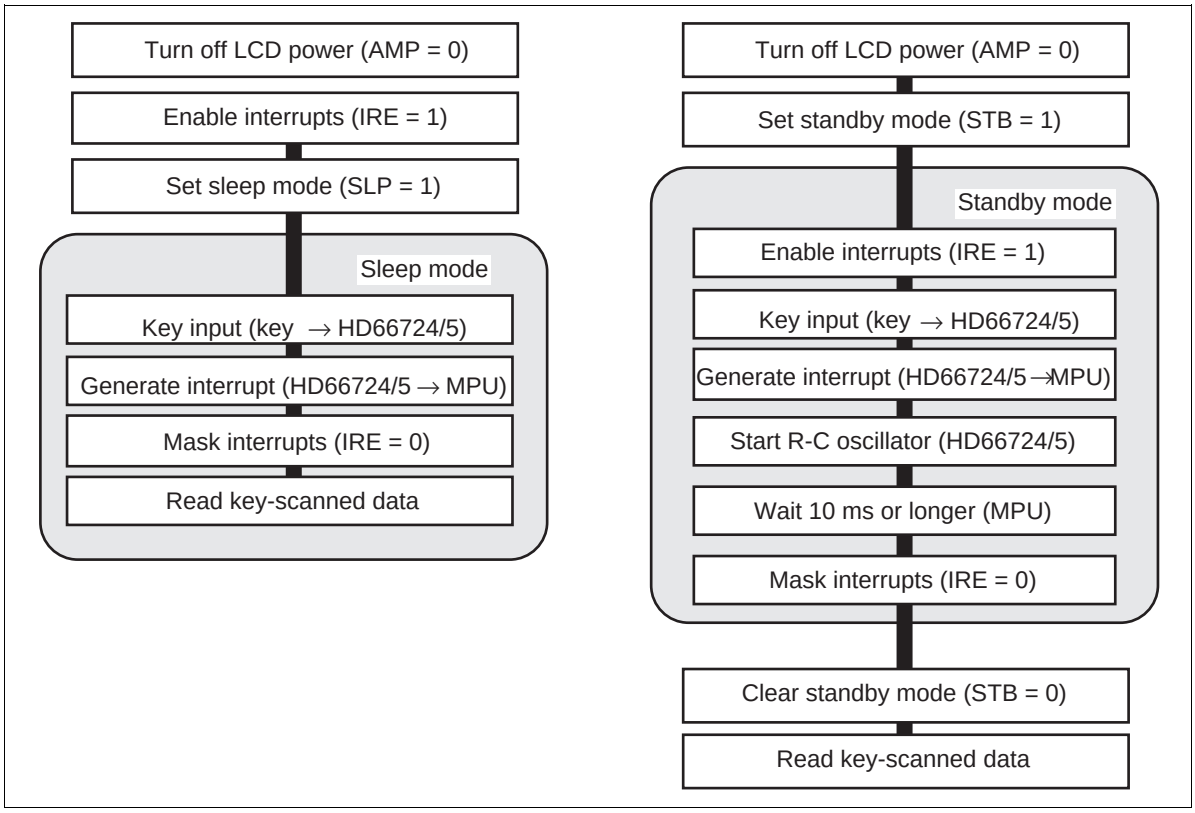


Figure 31 Key Scan Interrupt Processing Flow in Sleep and Standby Modes

Parallel Data Transfer

8-Bit Interface

Setting the IM2/1/0 (interface mode) to the GND/V_{CC}/GND level allows 68-system 8-bit parallel data transfer. A direct interface using the 8-bit E-clock-synchronized bus or an interface via the I/O bus can be established. Setting the IM2/1/0 to the V_{CC}/V_{CC}/GND level allows 80-system 8-bit parallel data transfer. When the number of buses or mounting area is limited, use a 4-bit bus interface or serial data transfer.

Using a parallel bus interface disables the key scan function. To prevent this, use a clock-synchronized serial interface.

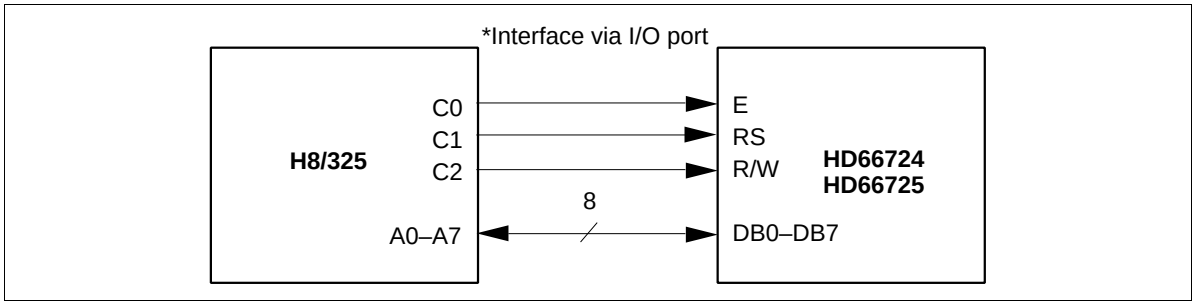


Figure 32 Interface to 8-Bit Microcomputer

4-Bit Interface

Setting the IM2/1/0 (interface mode) to the GND/V_{CC}/V_{CC} level allows 68-system 4-bit parallel data transfer using pins DB7/KIN7-DB4/KIN4. Setting the IM2/1/0 to the V_{CC}/V_{CC}/V_{CC} level allows 80-system 4-bit parallel data transfer. 8-bit instructions and RAM data are divided into four upper/lower bits and transfer starts from the upper four bits.

Using a parallel bus interface disables the key scan function. To prevent this, use a clock-synchronized serial interface.

Note: Transfer synchronization function for a 4-bit bus interface
The HD66724/HD66725 support transfer synchronization function which resets the upper/lower counter to count upper/lower four-bit data transfer in the 4-bit bus interface. Noise causing transfer mismatch between the four upper and lower bits can be corrected by a reset triggered by consecutively writing a 0000 instruction four times. The next transfer starts from the upper four bits. Executing synchronization function periodically can recover any runaway in the display system.

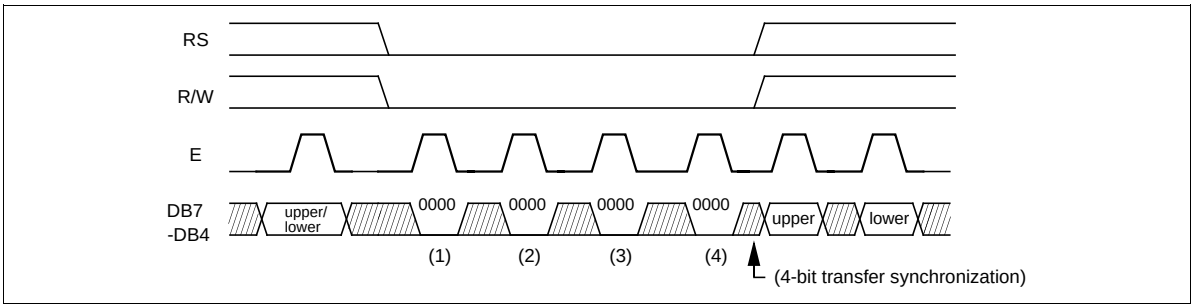


Figure 33 4-Bit Transfer Synchronization

Oscillator Circuit

The HD66724/HD66725 can either be supplied with operating pulses externally (external clock mode), oscillate using an internal CR oscillator with an external oscillator-resistor (external resistor oscillation mode), or oscillate using an internal oscillator-resistor (internal resistor oscillation mode). Internal oscillator-resistors fluctuate by ±30% depending on products. Avoid frame frequency fluctuations as these affect video quality. To prevent these, use an external resistor.

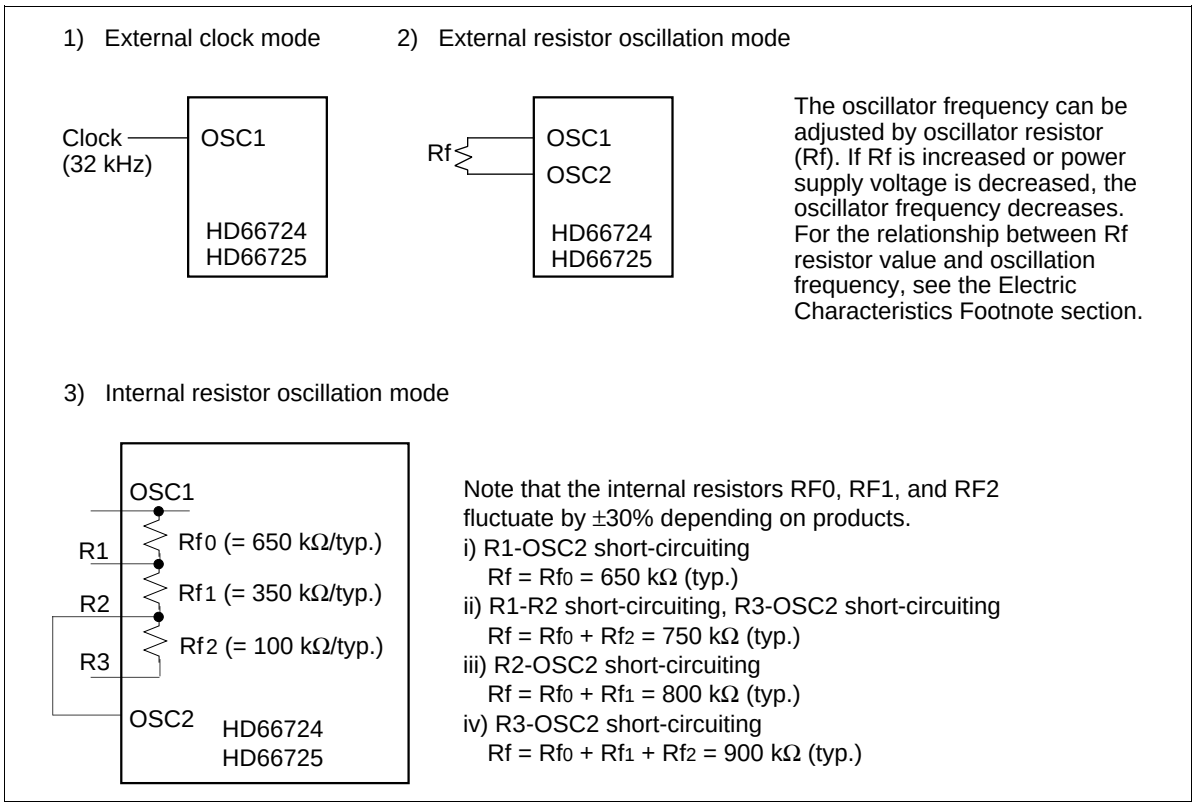


Figure 34 Oscillator Circuits

Table 36 Multiplexing Duty Ratio and LCD Frame Frequency (fosc = 32 kHz)

Item	Segment mode (NL2/1/0 = 000)	1-Line Display (NL2/1/0 = 001)	2-Line Display (NL2/1/0 = 010)	3-Line Display (NL2/1/0 = 011)
Multiplexing duty ratio	1/2	1/10	1/18	1/26
Optimum drive bias (recommended value)	1/2	1/4	1/5	1/6
Frame frequency	80 Hz	80 Hz	74 Hz	77 Hz

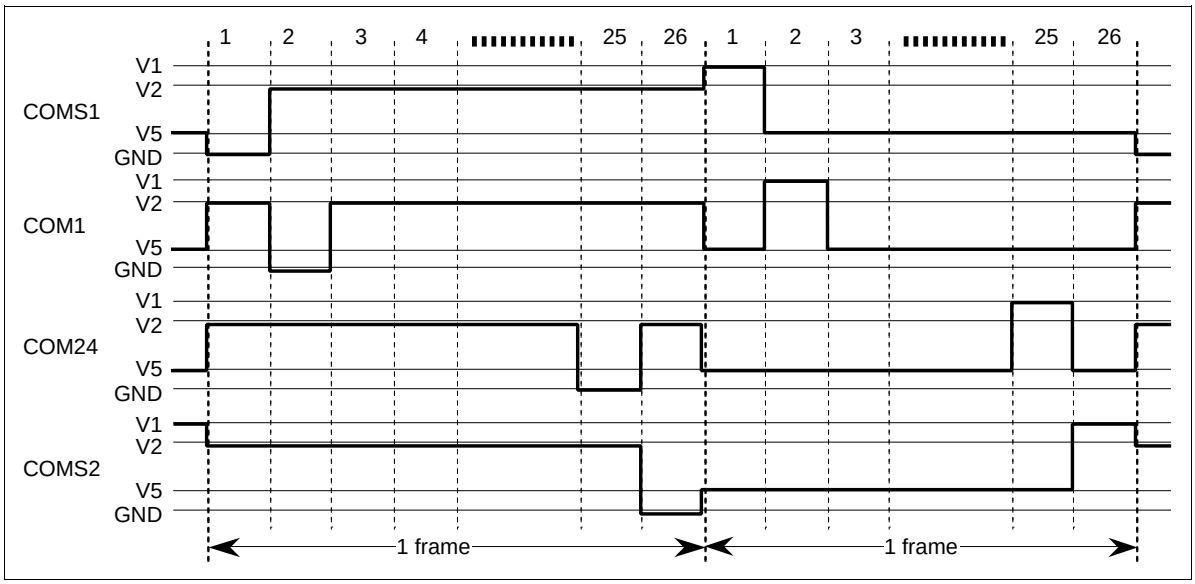


Figure 35 LCD Drive Output Waveform (3-Line Display with 1/26 Multiplexing Duty Ratio)

Power Supply for Liquid Crystal Display Drive

When External Power Supply and Internal Operational Amplifiers are Used

To supply LCD drive voltage directly from the external power supply without using the internal booster, circuits should be connected as shown in figure 36. Here, contrast can be adjusted through the CT bits of the contrast control instruction.

The HD66724/HD66725 incorporate a voltage-follower operational amplifier for each V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, potential differences between V_{LCD} and V1 and between V5 and GND must be 0.1 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.1 µF to 0.5 µF between each internal operational amplifier V1out to V5out output and GND and stabilize the output level of the operational amplifier.

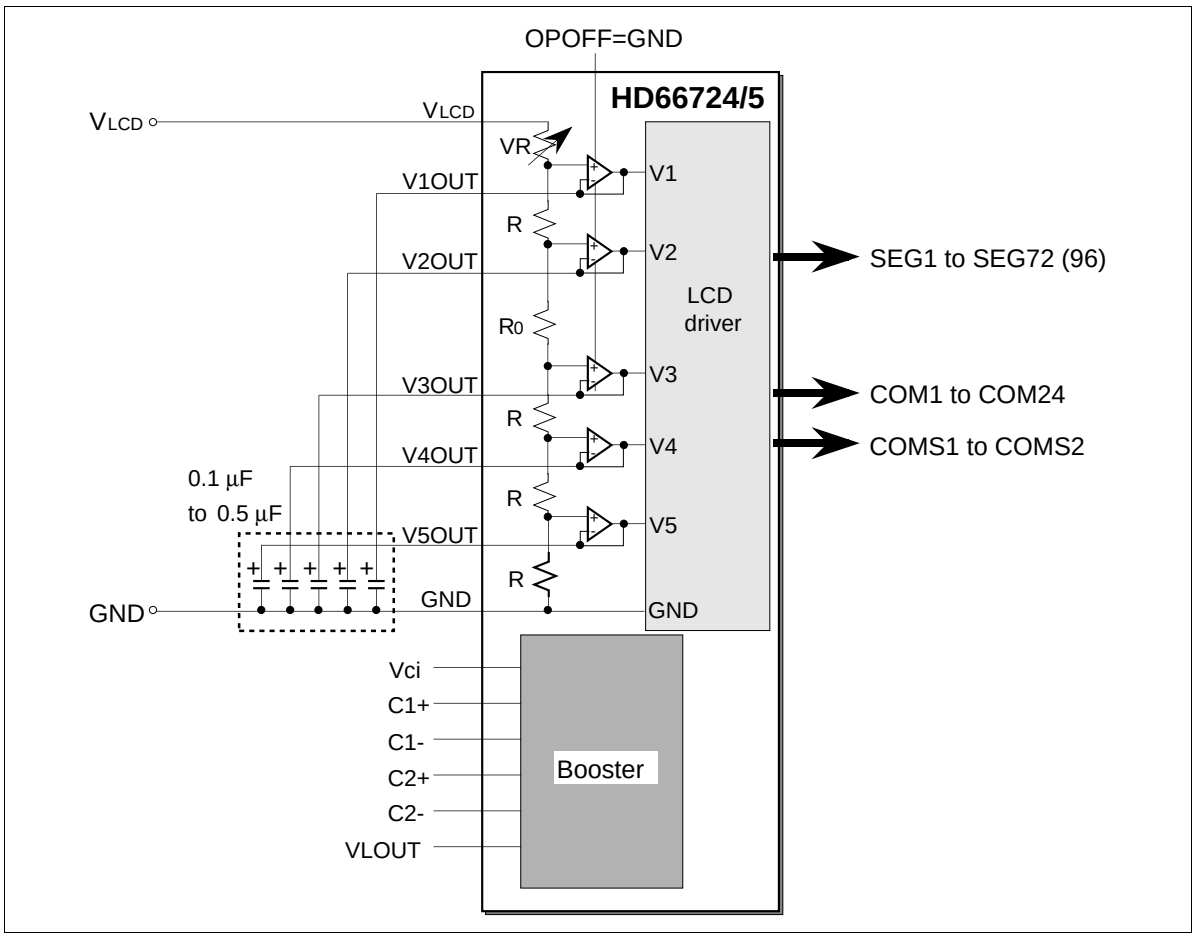


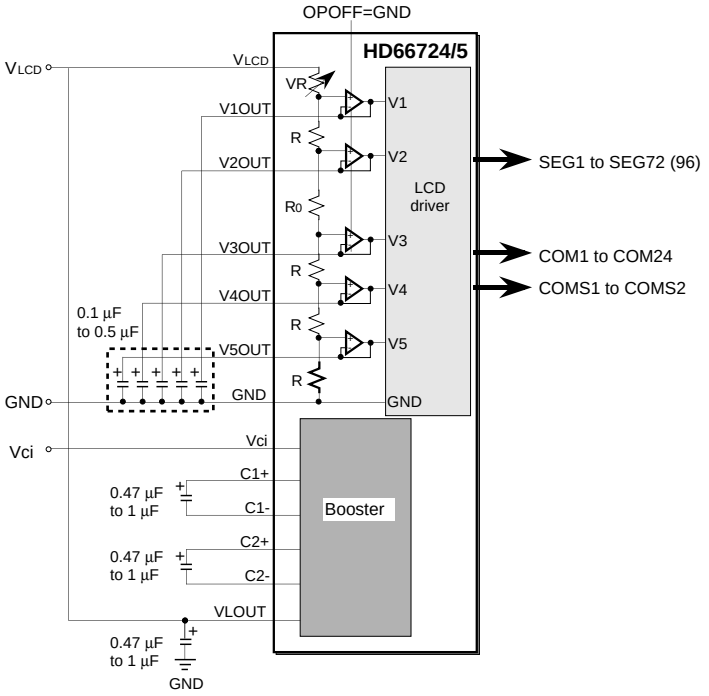
Figure 36 External Power Supply Circuit for LCD Drive Voltage Generation

When an Internal Booster and Internal Operational Amplifiers are Used

To supply LCD drive voltage using the internal booster, circuits should be connected as shown in figure 37. Here, contrast can be adjusted through the CT bits of the contrast control instruction. Temperature can be compensated either through the CT bits or by controlling the reference voltage for the booster (Vci pin) using a thermistor.

Note that Vci is both a reference voltage and power supply for the booster. The reference voltage must therefore be adjusted using an emitter-follower or a similar element so that sufficient current can be supplied. In this case, Vci must be equal to or smaller than the V_{CC} level.

The HD66724/HD66725 incorporate a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different liquid-crystal drive voltages. Thus, the potential differences between V_{LCD} and V1 and between V5 and GND must be 0.1 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.1 µF to 0.5 µF between each internal operational amplifier V1out to V5out output and GND and stabilize the output level of the operational amplifier.



Notes: 1. The reference voltage input (Vci) must be adjusted so that the output voltage after boosting will not exceed the absolute maximum rating for the liquid-crystal power supply voltage (7 V). Particularly, Vci must be 2.3 V or less for triple boosting.
2. Vci is both a reference voltage and power supply for the booster; connect it to Vcc directly or combine it with a transistor so that sufficient current can be obtained.
3. Vci must be smaller than Vcc.
4. When using up to the double booster, no capacitors are required between C2+ and C2–.
5. Polarized capacitors must be connected correctly.
6. Circuits for temperature compensation should be based on the sample circuit below.

Figure 37 Internal Booster Circuit for LCD Drive Voltage Generation

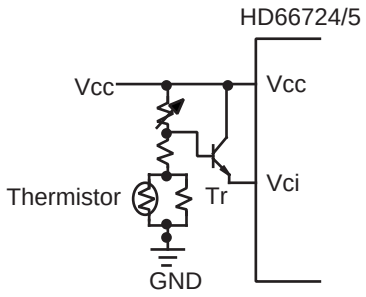
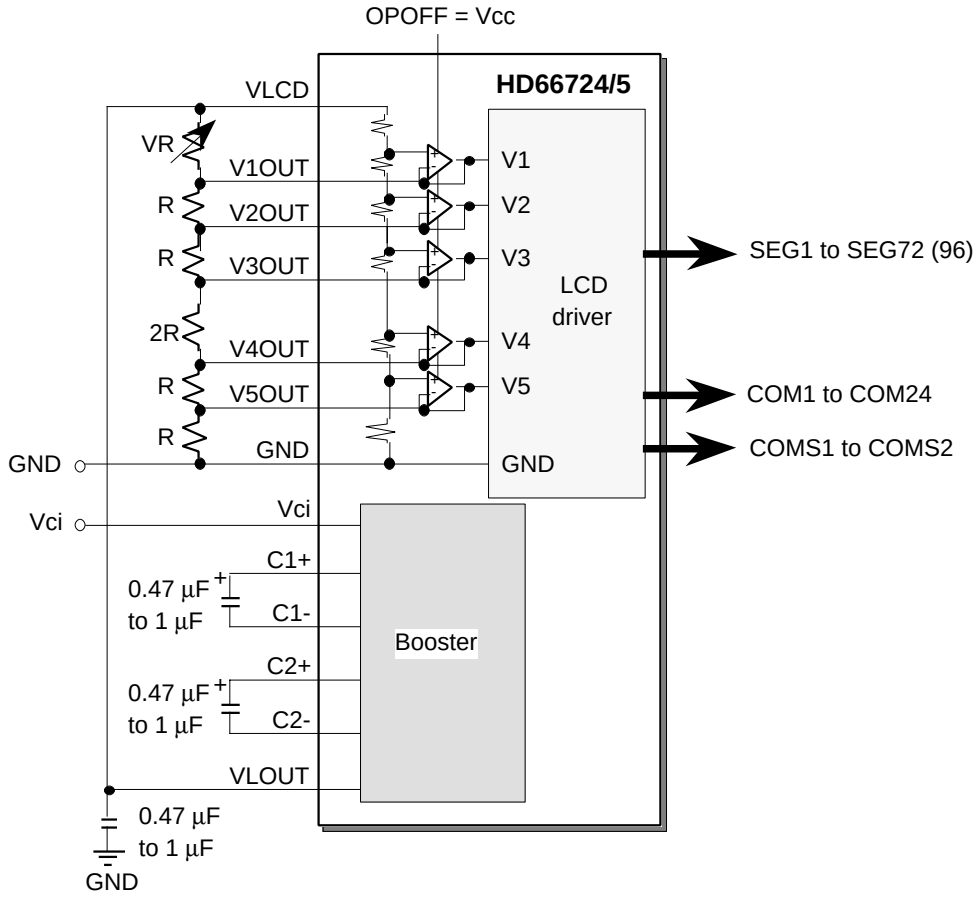


Figure 38 External Power Supply Circuit for LCD Drive Voltage Generation

When an Internal Booster and External Bleeder-Resistors are Used

When internal operational amplifiers cannot fully drive the LCD panel used, V1 to V5 voltages can be supplied through external bleeder-resistors (figure 39). Here, the OPOFF pin must be set to the V_{CC} level to turn off the internal operational amplifiers. Since the internal contrast adjuster is disabled, contrast must be adjusted externally. Connection of external bleeder-resistors can specify a given bias value from 1/2 to 1/6. Figure 39 shows connection for 1/6-bias drive voltage generation. Double- and triple-boosters can be used as they are.



Notes:
1. Resistance of each external bleeder resistor should be 4.7 kΩ to 25 kΩ.
2. The bias current value for driving LCDs can be varied by adjusting the resistance (2R) between the V3OUT and V4OUT pins.
3. The internal contrast adjuster is disabled; contrast must be adjusted either by controlling the external variable resistor between VLCD and V1 for the booster.
4. Vci is both a reference voltage and power supply for the booster; connect it to Vcc directly or combine it with a transistor so that sufficient current can be obtained.
5. Vci must be smaller than Vcc.

Figure 39 Circuit Using External Bleeder-Resistors

Contrast Adjuster

Contrast for an LCD can be adjusted by varying the liquid-crystal drive voltage (potential difference between V_{LCD} and V1) through the CT bits of the contrast control instruction (electron volume function). See figure 40 and table 37. The value of a variable resistor (VR) can be adjusted within a range from 0.1 x R through 3.2 x R, where R is a reference resistance obtained by dividing the total resistance between V_{LCD} and V1.

The HD66724/HD66725 incorporate a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different liquid-crystal drive voltages. Thus, CT4-0 bits must be adjusted so that the potential differences between V_{LCD} and V1 and between V5 and GND are 0.1 V or higher when liquid-crystal drives.

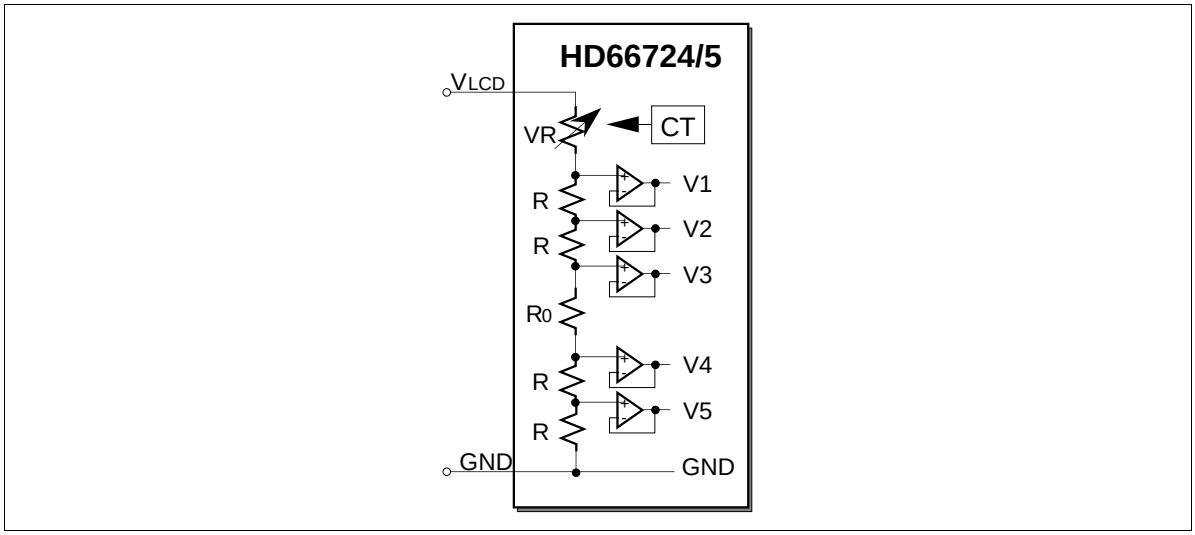


Figure 40 Contrast Adjuster

Table 37 Contrast-Adjust Bits (CT) and Variable Resistor Values

CT Set Value					Variable Resistor Value (VR)	Potential Difference between V1 and GND	Display Color
CT4	CT3	CT2	CT1	CT0			
0	0	0	0	0	3.2 x R	(Small)	(Light)
0	0	0	0	1	3.1 x R		
0	0	0	1	0	3.0 x R		
0	0	0	1	1	2.9 x R		
0	0	1	0	0	2.8 x R		
0	0	1	0	1	2.7 x R		
0	0	1	1	0	2.6 x R		
0	0	1	1	1	2.5 x R		
0	1	0	0	0	2.4 x R		
0	1	0	0	1	2.3 x R		
0	1	0	1	0	2.2 x R		
0	1	0	1	1	2.1 x R		
0	1	1	0	0	2.0 x R		
0	1	1	0	1	1.9 x R		
0	1	1	1	0	1.8 x R		
0	1	1	1	1	1.7 x R		
1	0	0	0	0	1.6 x R		
1	0	0	0	1	1.5 x R		
1	0	0	1	0	1.4 x R		
1	0	0	1	1	1.3 x R		
1	0	1	0	0	1.2 x R		
1	0	1	0	1	1.1 x R		
1	0	1	1	0	1.0 x R		
1	0	1	1	1	0.9 x R		
1	1	0	0	0	0.8 x R		
1	1	0	0	1	0.7 x R		
1	1	0	1	0	0.6 x R		
1	1	0	1	1	0.5 x R		
1	1	1	0	0	0.4 x R		
1	1	1	0	1	0.3 x R		
1	1	1	1	0	0.2 x R		
1	1	1	1	1	0.1 x R	(Large)	(Deep)

Table 38 Contrast Adjustment per Bias Drive Voltage

Bias	LCD drive voltage: V_{DR}	Contrast adjustment range
1/6.5 bias drive	$\frac{6.5 \times R}{6.5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.670 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.985 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{6.5 \times R + VR} \times (V_{LCD}-GND) \geq 0.1[V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{6.5 \times R + VR} \times (V_{LCD}-GND) \geq 0.1[V]$
1/6 bias drive	$\frac{6 \times R}{6 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.652 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.984 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{6 \times R + VR} \times (V_{LCD}-GND) \geq 0.1[V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{6 \times R + VR} \times (V_{LCD}-GND) \geq 0.1[V]$
1/5.5 bias drive	$\frac{5.5 \times R}{5.5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.632 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.982 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{5.5 \times R + VR} \times (V_{LCD}-GND) \geq 0.1[V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{5.5 \times R + VR} \times (V_{LCD}-GND) \geq 0.1[V]$
1/5 bias drive	$\frac{5 \times R}{5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.610 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.980 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{5 \times R + VR} \times (V_{LCD}-GND) \geq 0.1[V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{5 \times R + VR} \times (V_{LCD}-GND) \geq 0.1[V]$
1/4.5 bias drive	$\frac{4.5 \times R}{4.5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.556 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.978 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{4.5 \times R + VR} \times (V_{LCD}-GND) \geq 0.1[V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{4.5 \times R + VR} \times (V_{LCD}-GND) \geq 0.1[V]$
1/4 bias drive	$\frac{4 \times R}{4 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.556 \times (V_{LCD}-GND) \leq V_{DR} \leq 0.976 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{4 \times R + VR} \times (V_{LCD}-GND) \geq 0.1[V]$ - Limit if potential difference between VLCD and V1 : $\frac{VR}{4 \times R + VR} \times (V_{LCD}-GND) \geq 0.1[V]$

Liquid Crystal Display Drive Bias Selector Circuit

An optimum liquid crystal display bias value can be selected using BS2-0 bits, according to the liquid crystal drive duty ratio setting (NL2-0 bits). Liquid crystal display drive duty ratio and bias value can be displayed while switching software applications to match the LCD panel display status. The optimum bias value calculated using the following expression is an ideal value where the optimum contrast is obtained. Driving by using a lower value than the optimum bias value provides lower contrast and lower liquid crystal display voltage (potential difference between V1 and GND). When the liquid crystal display voltage is insufficient even if a triple booster is used or output voltage is lowered because the battery life has been reached, the display can be made easier to see by lowering the liquid crystal bias.

The liquid crystal display can be adjusted by using the contrast adjustment register (CT4-0 bits) and selecting the booster output level (BT1/0 bits).

$$\text{Optimum bias value for 1/N duty ratio drive voltage} = \frac{1}{\sqrt{N + 1}}$$

Table 39 Optimum Drive Bias Values

LCD drive duty ratio (NL2-0 set value)	1/26 duty ratio (NL2-0 = 011)	1/18 duty ratio (NL2-0 = 010)	1/10 duty ratio (NL2-0 = 001)	1/2 duty ratio (NL2-0 = 000)
Optimum drive bias value (BS2-0 set value)	1/6 bias (BS2-0 = 001)	1/5 bias (BS2-0 = 011)	1/4 bias (BS2-0 = 101)	1/4 bias (BS2-0 = 101)

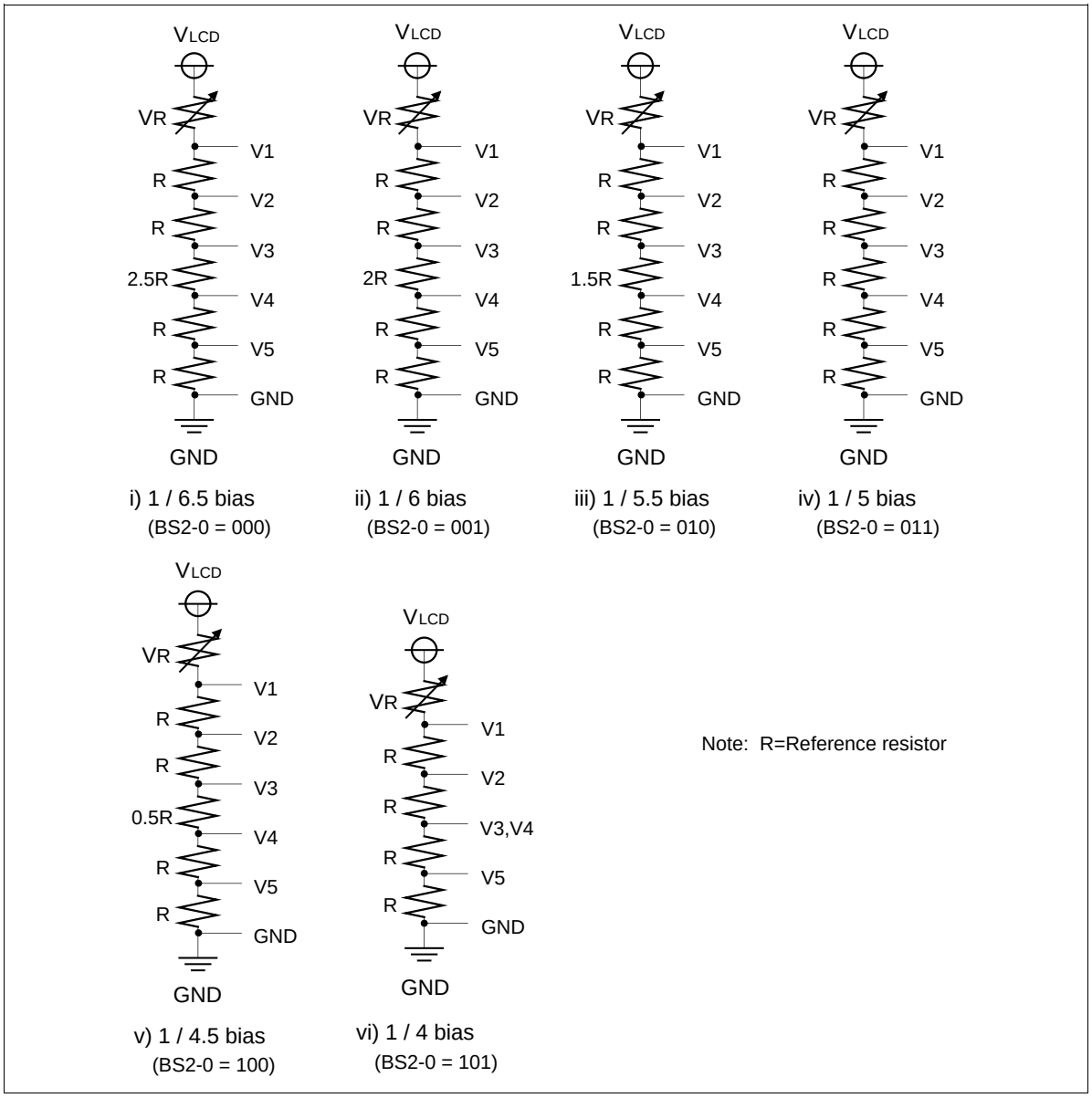


Figure 41 Liquid Crystal Display Drive Bias Circuit

LCD Panel Interface

The HD66724/HD66725 have a function for changing the common driver/segment driver output shift direction using the CMS bit and SGS bit to meet the chip mounting positions of the HD66724/HD66725. This is to facilitate the interface wiring to the LCD panel with COG or TCP installed.

Wiring for 3-Line Display (1/26 Duty Ratio)

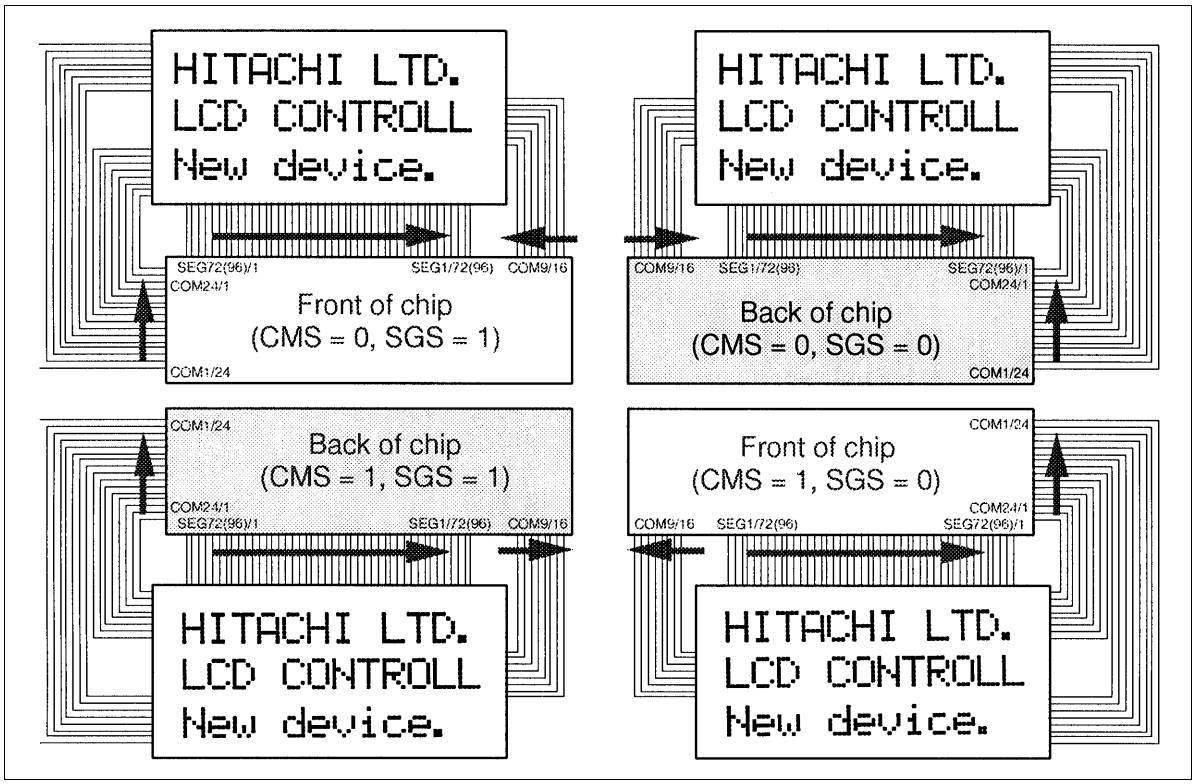


Figure 42 3-Line Display Pattern Wiring

Wiring for 2-Line Display (1/18 Duty Ratio)

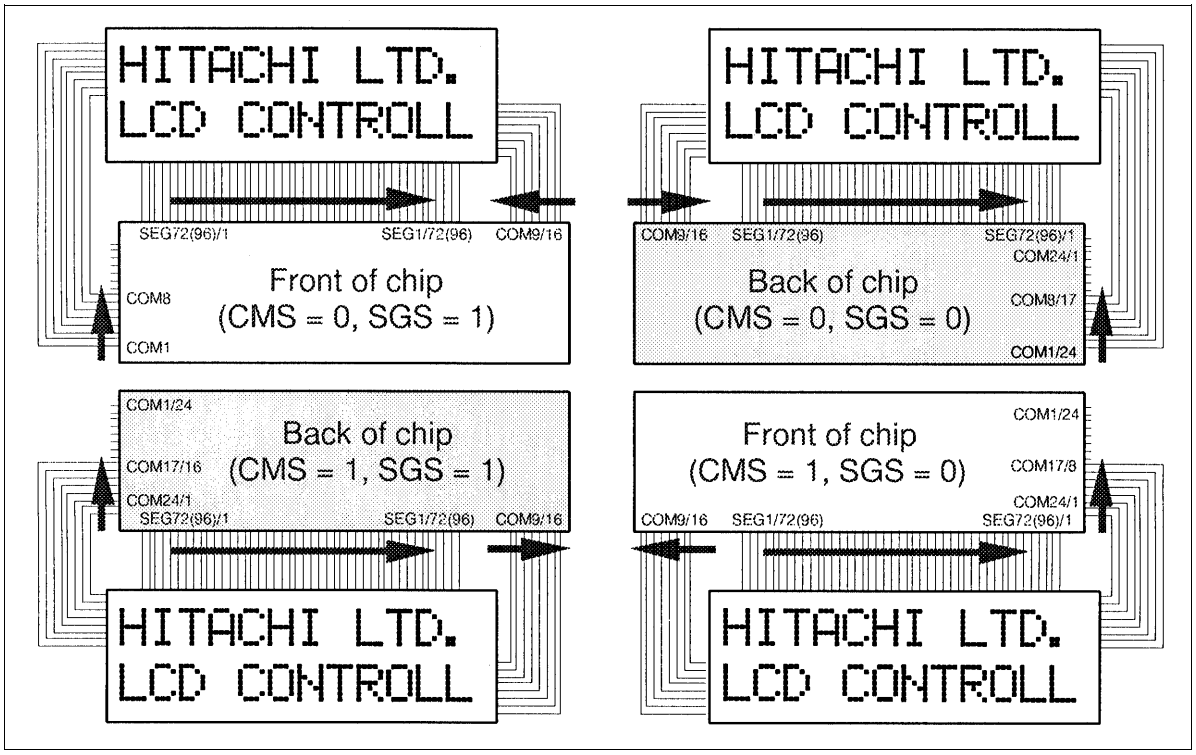


Figure 43 2-Line Display Pattern Wiring

CGROM Bank Switching Function

The HD66724/HD66725 incorporate two pages of CGROM. Switching the memory bank using the CGROM bank switching bit (ROM) can display a total of 432 font patterns. Multinational fonts, special symbols, and icons can be displayed. Note that the number of fonts simultaneously displayed is CGROM: 240 + CGRAM: 16 when memory bank 0 is selected, and CGROM: 192 + CGRAM: 64 when memory bank 1 is selected. Font displays for CGRAM (1) to (16) are used in common with memory bank 0 and memory bank 1.

Table 40 CGROM Bank Switching

Character Code	Memory Bank 0 (ROM = 0)	Memory Bank 1 (ROM = 1)
"00"H to "0F"H	***CGRAM (1) to (16)***	***CGRAM (1) to (16)***
"10"H to "1F"H	CGROM (1) to (16)	***CGRAM (17) to (32)***
"20"H to "2F"H	CGROM (17) to (32)	CGROM (241) to (256)
"30"H to "3F"H	CGROM (33) to (48)	CGROM (257) to (272)
"40"H to "4F"H	CGROM (49) to (64)	CGROM (273) to (288)
"50"H to "5F"H	CGROM (65) to (80)	CGROM (289) to (304)
"60"H to "6F"H	CGROM (81) to (96)	CGROM (305) to (320)
"70"H to "7F"H	CGROM (97) to (112)	CGROM (321) to (336)
"80"H to "8F"H	CGROM (113) to (128)	***CGRAM (33) to (48)***
"90"H to "9F"H	CGROM (129) to (144)	***CGRAM (49) to (64)***
"A0"H to "AF"H	CGROM (145) to (160)	CGROM (337) to (352)
"B0"H to "BF"H	CGROM (161) to (176)	CGROM (353) to (368)
"C0"H to "CF"H	CGROM (177) to (192)	CGROM (369) to (384)
"D0"H to "DF"H	CGROM (193) to (208)	CGROM (385) to (400)
"E0"H to "EF"H	CGROM (209) to (224)	CGROM (401) to (416)
"F0"H to "FF"H	CGROM (225) to (240)	CGROM (417) to (432)

Graphics Display Function

The HD66724/HD66725 have a character display mode (GR = 0) where CGRAM or CGROM is used to display font patterns, and a graphics display mode (GR = 1) where bit pattern data is set to CGRAM to display given patterns. In the character display mode, an LCD panel display can easily be provided by sending byte-per-character character codes to DDRAM, but any pattern not set to CGROM or CGRAM cannot be displayed. In the graphics display mode, all bit pattern data to be displayed must be sent although any pattern can be displayed. The HD66724/HD66725 support both of these modes which can easily be switched using the GR bit.

In the graphics display mode, kanji characters, special symbols, and graphic icons can be displayed. In the HD66724, up to a 72 x 26-dot display is allowed using CGRAM and SEGRAM. Thus, for a 12 x 12-dot kanji font, up to a 2-line x 6-character kanji display is allowed. In the HD66725, up to a 96 x 26-dot display is allowed, and up to a 2-line x 8-character kanji display is allowed for a 12 x 12-dot kanji font.

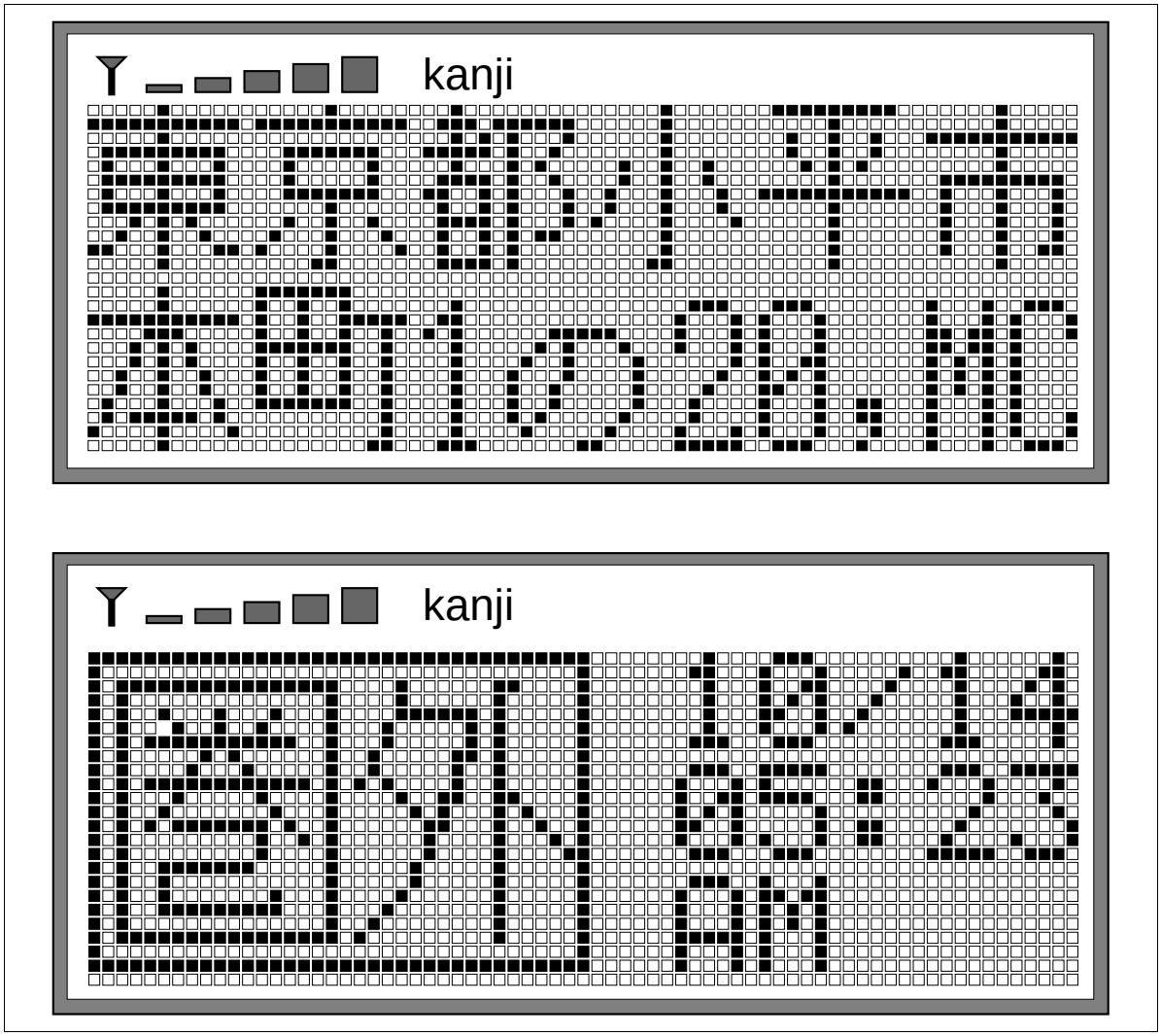


Figure 44 Kanji Display in Graphics Display Mode

Vertical Smooth Scroll

The HD66724/HD66725 can scroll vertically in units of raster-rows. In character display mode (GR = 0), this is achieved by writing character codes into a DDRAM area that is not being used for display. In other words, since DDRAM corresponds to a 5-line × 16-character display, two lines can be used to achieve continuous smooth vertical scroll even in a 3-line display. Here, after the fifth line is displayed, the first line is displayed again. In the graphics display mode (GR = 1), a 96 x 32-dot area is assigned as CGRAM. Thus a non-display area other than the 72 x 24-dot display area can be used to provide consecutive, smooth scroll display. Segment (mark) display is system-fixed and the scroll function cannot be used.

Specifically, this function is controlled by incrementing or decrementing the value in the display-start line bits (SL2 to SL0) and display-start raster-row bits (SN2/1/0) by 1. For example, to smoothly scroll up, first set line bits SN2 to SN0 to 000, and increment SL2 to SL0 by 1 from 000 to 111 to scroll seven raster-rows. Then increment line bits SN2 to SN0 to 001, and again increment SL2 to SL0 by 1 from 000 to 111. To start displaying and scrolling from the first raster-row of the second line, update the first line of DDRAM or CGRAM data as desired during its non-display period.

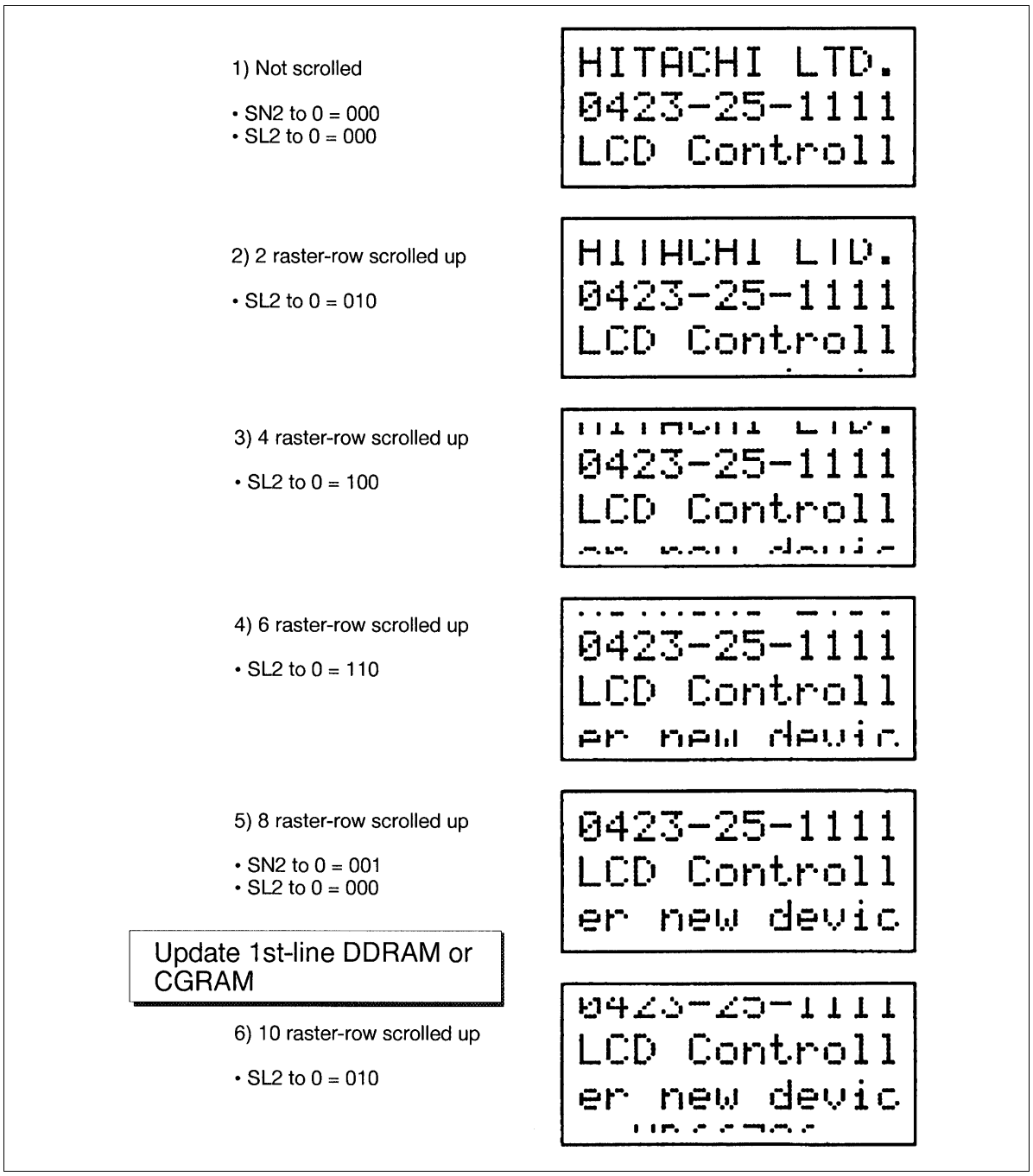


Figure 45 Vertical Smooth Scroll

Setting Instructions (Character Display Mode: GR = 0, 3-Line Display: NL2-0 = 011)

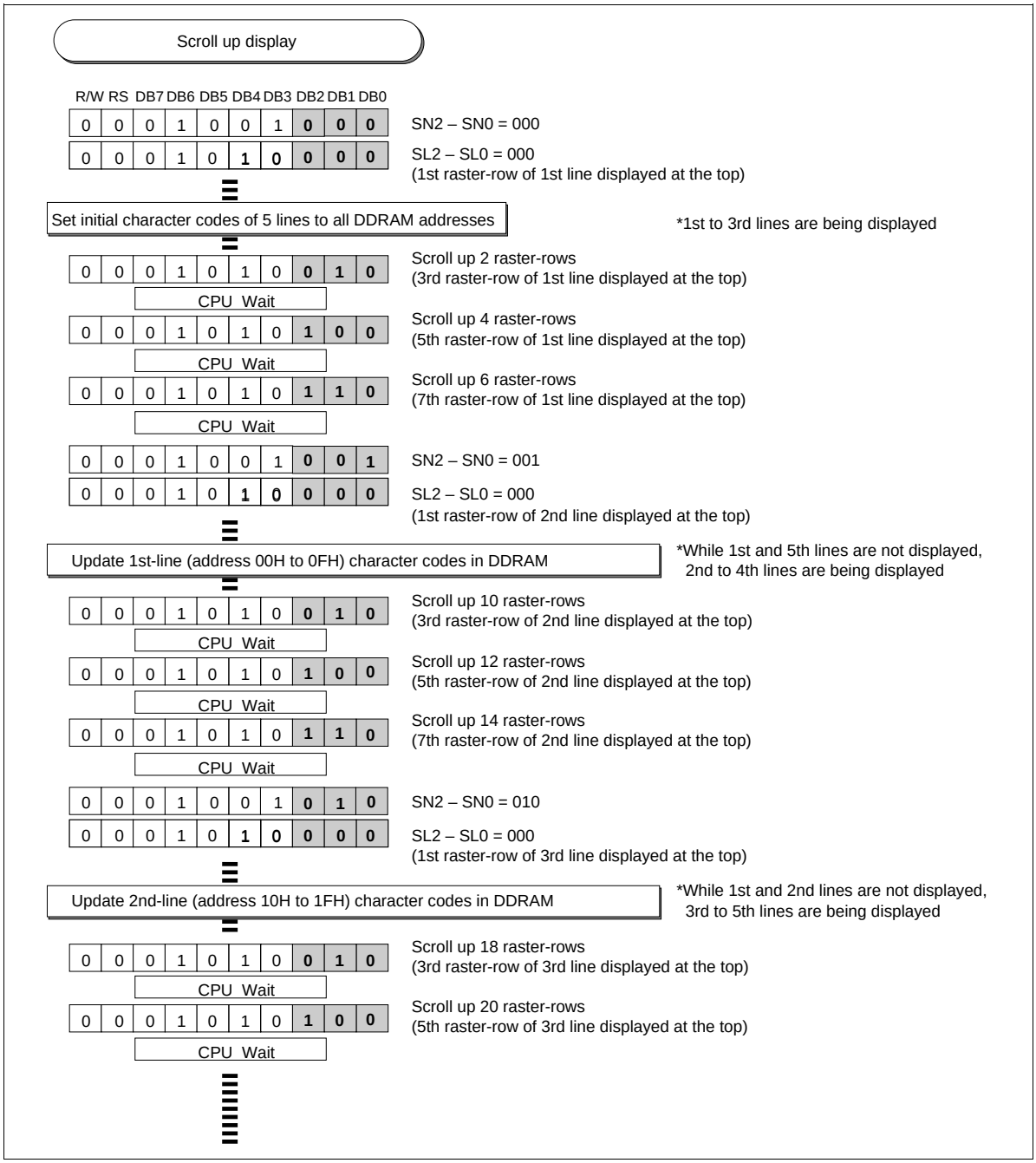


Figure46 Setting Instructions for Vertical Smooth Scroll (Character Display Mode)

Setting Instructions (Graphics Display Mode: GR = 1, 3-Line Display: NL2-0 = 011)

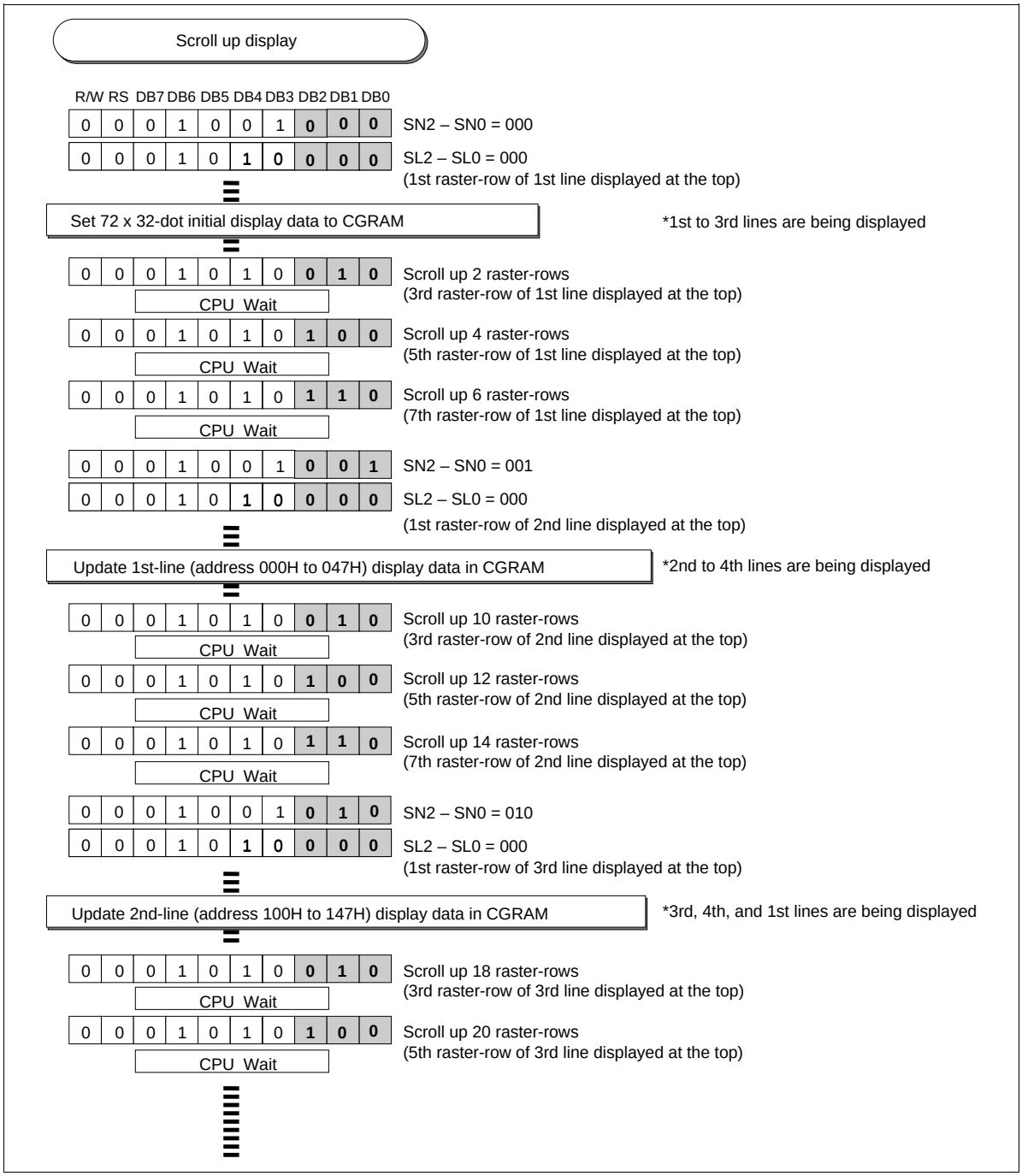


Figure 47 Setting Instructions for Vertical Smooth Scroll (Graphics Display Mode)

Horizontal Smooth Scroll

The HD66724/HD66725 perform the horizontal smooth scroll in 3-dot units. In the character display mode (GR = 0), an area of 16 characters x 5 lines is assigned as DDRAM. In the graphics display mode (GR = 1), a 96 x 32-dot area is assigned as CGRAM. These non-display areas are used to provide a horizontal smooth scroll display. When the HD66725 displays 16 characters or 96 dots, there are no non-display areas and horizontal scrolling cannot be done.

Display lines for horizontal scroll can be separately specified using the horizontal scroll bits (SE4-1), allowing a scroll of the whole display or specified lines. Horizontal scroll dots can be specified using the horizontal scroll dot bits (SQ2-0), allowing up to a 21-dot scroll at a time. For further scrolls, data in the DDRAM or CGRAM must be overwritten.

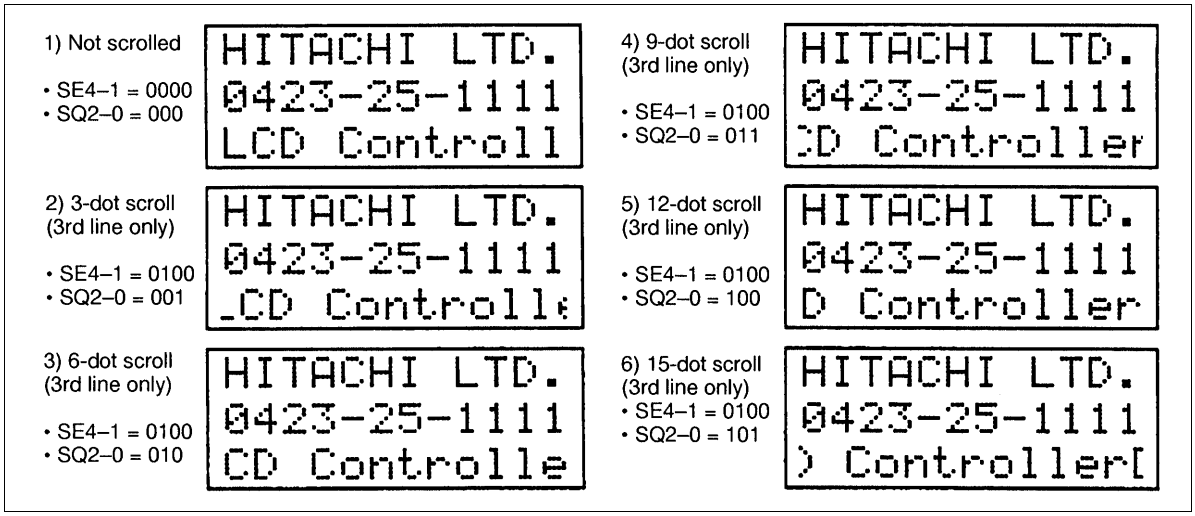


Figure 48 Horizontal Smooth Scroll Display

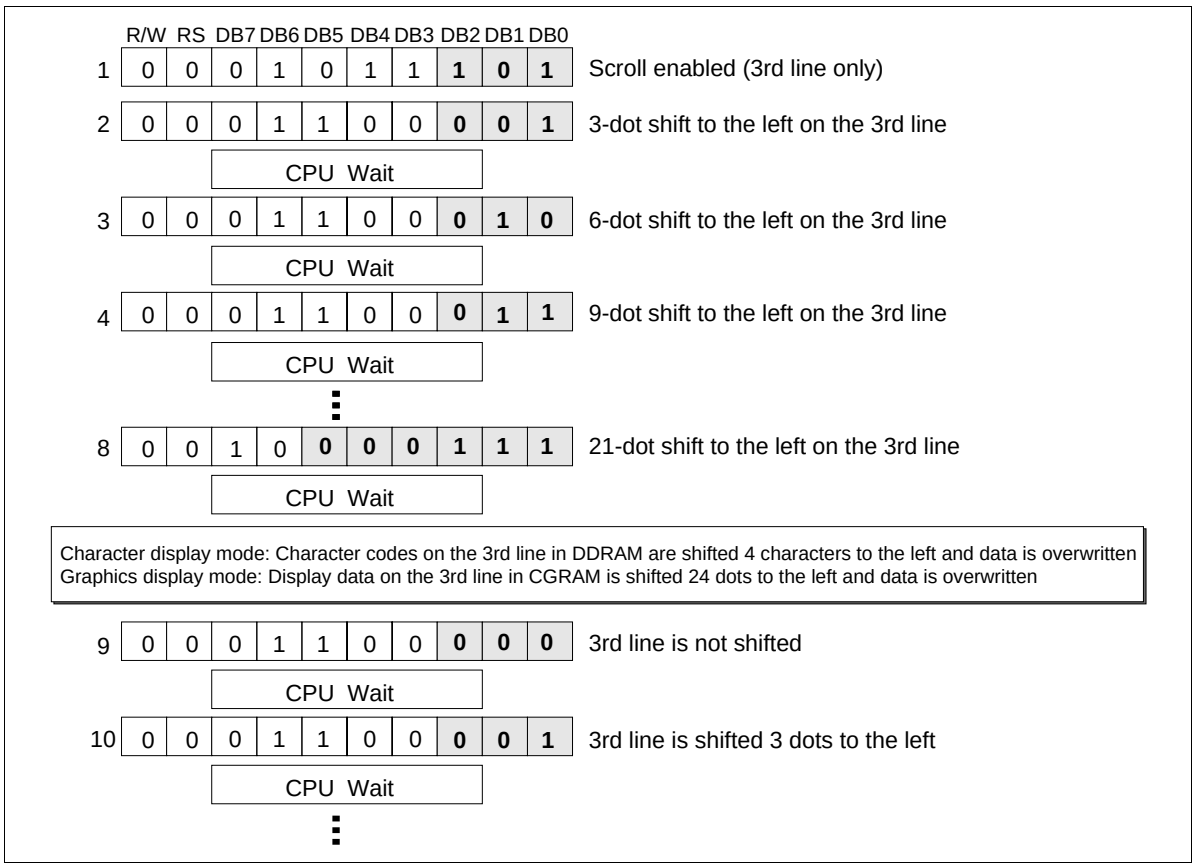


Figure 49 Smooth Scroll to the Left

Double-Height Display

The HD66724/HD66725 can double the height of any desired line from the first to third lines. A line can be selected by the DL3 to DL1 bits as listed in table 41. All the standard font characters stored in the CGROM and CGRAM can be doubled in height, allowing easy recognition. Note that there should be no space between the lines for double-height display (figure 50).

Table 41 Double-Height Display Specifications

DL3	DL2	DL1	2-Line Display (NL2-0 = 010)	3-Line Display (NL2-0 = 011)
0	0	0	1st & 2nd lines: normal	1st to 3rd lines: normal
0	0	1	1st line: double-height	1st line: double-height, 2nd line: normal
0	1	0	Disabled	2nd line: double-height, 1st line: normal
0	1	1	1st line: double-height	Disabled
1	0	0	1st & 2nd lines: normal	Disabled
1	0	1	1st line: double-height	1st line: double-height, 2nd line: normal
1	1	0	Disabled	2nd line: double-height, 1st line: normal
1	1	1	1st line: double-height	Disabled

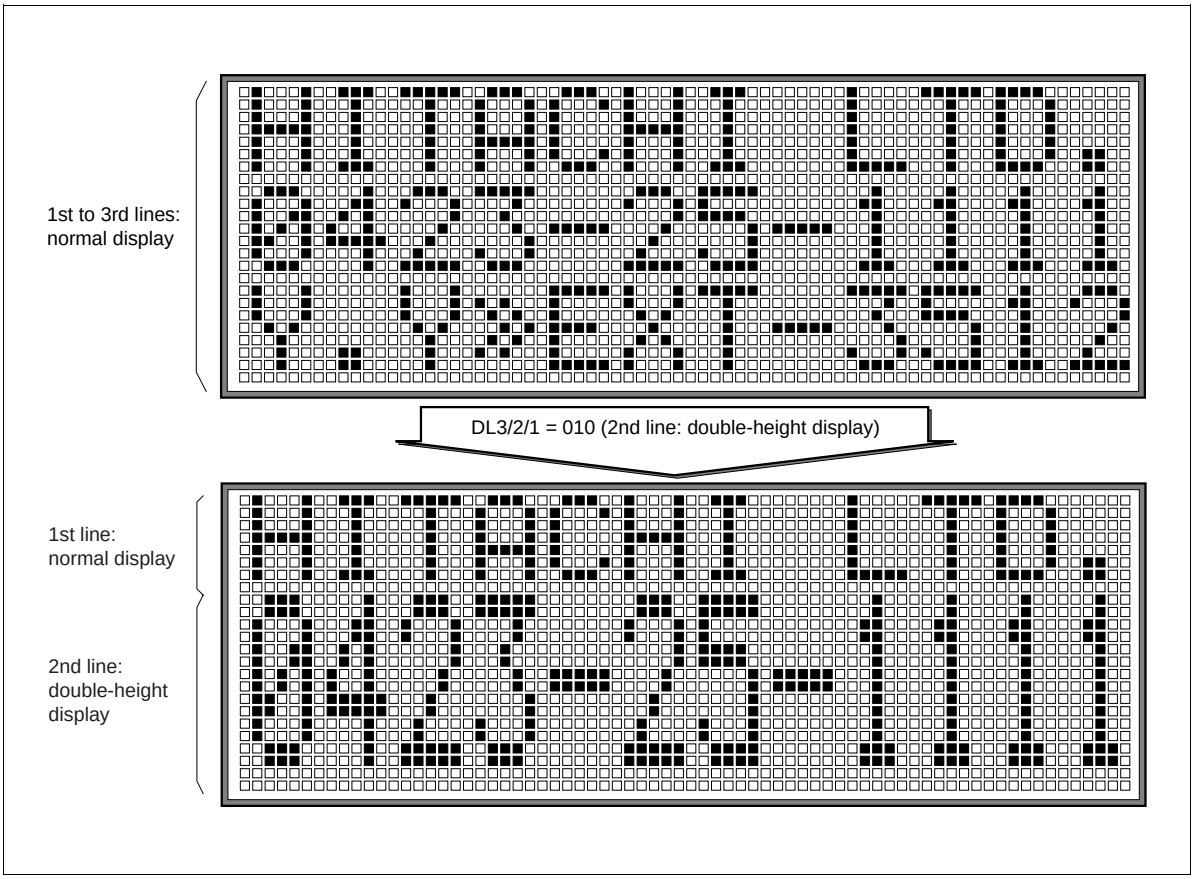


Figure 50 Double-Height Display

Blink Mark Display

The HD66724/HD66725 have a grayscale display and blink display based on 144 (192) individual segments (marks). Forty-eight (sixty-four) of these are for grayscale display and the remainder are for blink display.

These 48 (64) segments can also control a grayscale display, providing simple grayscale on specific pictograms or marks. For example, the battery no charge alarm uses this dispay. The above display uses a curtailed frame grayscale system, and flicker may result in quick-response liquid crystal materials. Tables 42 and 43 show the relationship between set data in SEGRAM and effective applied voltage during frame curtailing operation.

The remaining 96 (128) segments are resposible for normal blinking and double-speed blinking. Normal blinking (b & w) is achieved by repeatedly turning on each segment for 32 frames and turning it off for the next 32 frames. Double-speed blinking (b & w) is achieved by repeatedly turning on each segment for 16 frames and turning it off for the next 16 frames, that is, double the speed of normal blinking.

Table 42 Relationship between Segment Driver Output Pin and Segment Display Function (HD66724)

When SGS = 0	When SGS = 1	Segment Output Control
SEG1/72, SEG4/69, SEG7/66 SEG10/63, SEG13/60, SEG16/57 SEG19/54, SEG22/51, SEG25/48 SEG28/45, SEG31/42, SEG34/39 SEG37/36, SEG40/33, SEG43/30 SEG46/27, SEG49/24, SEG52/21 SEG55/18, SEG58/15, SEG61/12 SEG64/9, SEG67/6, SEG70/3	SEG72/1, SEG69/4, SEG66/7 SEG63/10, SEG60/13, SEG57/16 SEG54/19, SEG51/22, SEG48/25 SEG45/28, SEG42/31, SEG39/34 SEG36/37, SEG33/40, SEG30/43 SEG27/46, SEG24/49, SEG21/52 SEG18/55, SEG15/58, SEG12/61 SEG9/64, SEG6/67, SEG3/70	Grayscale segment display allowed
Output pins other than above	Output pins other than above	Segment blinking allowed

Table 43 Relationship between Segment Driver Output Pin and Segment Display Function (HD66725)

When SGS = 0	When SGS = 1	Segment Output Control
SEG1/96, SEG4/93, SEG7/90, SEG10/87, SEG13/84, SEG16/81, SEG19/78, SEG22/75, SEG25/72, SEG28/69, SEG31/66, SEG34/63, SEG37/60, SEG40/57, SEG43/54, SEG46/51, SEG49/48, SEG52/45, SEG55/42, SEG58/39, SEG61/36, SEG64/33, SEG67/30, SEG70/27, SEG73/24, SEG74/21, SEG79/18, SEG82/15, SEG85/12, SEG88/9, SEG91/6, SEG94/3	SEG96/1, SEG93/4, SEG90/7, SEG87/10, SEG84/13, SEG81/16, SEG78/19, SEG75/22, SEG72/25, SEG69/28, SEG66/31, SEG63/34, SEG60/37, SEG57/40, SEG54/43, SEG51/46, SEG48/49, SEG45/52, SEG42/55, SEG39/58, SEG36/61, SEG33/64, SEG30/67, SEG27/70, SEG24/73, SEG21/76, SEG18/79, SEG15/82, SEG12/85, SEG9/88, SEG6/91, SEG3/94	Grayscale segment display allowed
Output pins other than above	Output pins other than above	Segment blinking allowed

Table 44 Relationship between SEGRAM Data and Grayscale Segment Display (Grayscale Control Segment Driver)

SEGRAM Data Setting				Effective Applied Voltage	SEGRAM Data Setting				Effective Applied Voltage
DB3	DB2	DB1	DB0	for COMS1 Segment	DB7	DB6	DB5	DB4	for COMS2 Segment
0	0	0	0	0 (Always unlit)	0	0	0	0	0 (Always unlit)
0	0	0	1	1 (Always lit)	0	0	0	1	1 (Always lit)
0	0	1	0	0.34 (Grayscale display)	0	0	1	0	0.34 (Grayscale display)
0	0	1	1	0.38 (Grayscale display)	0	0	1	1	0.38 (Grayscale display)
0	1	0	0	0.41 (Grayscale display)	0	1	0	0	0.41 (Grayscale display)
0	1	0	1	0.44 (Grayscale display)	0	1	0	1	0.44 (Grayscale display)
0	1	1	0	0.47 (Grayscale display)	0	1	1	0	0.47 (Grayscale display)
0	1	1	1	0.50 (Grayscale display)	0	1	1	1	0.50 (Grayscale display)
1	0	0	0	(Blink display) *	1	0	0	0	(Blink display) *
1	0	0	1	0.53 (Grayscale display)	1	0	0	1	0.53 (Grayscale display)
1	0	1	0	0.56 (Grayscale display)	1	0	1	0	0.56 (Grayscale display)
1	0	1	1	0.59 (Grayscale display)	1	0	1	1	0.59 (Grayscale display)
1	1	0	0	0.63 (Grayscale display)	1	1	0	0	0.63 (Grayscale display)
1	1	0	1	0.66 (Grayscale display)	1	1	0	1	0.66 (Grayscale display)
1	1	1	0	0.69 (Grayscale display)	1	1	1	0	0.69 (Grayscale display)
1	1	1	1	0.72 (Grayscale display)	1	1	1	1	0.72 (Grayscale display)

Note: Blinking is achieved by repeatedly turning on the segment for 32 frames and turning it off for the next 32 frames.

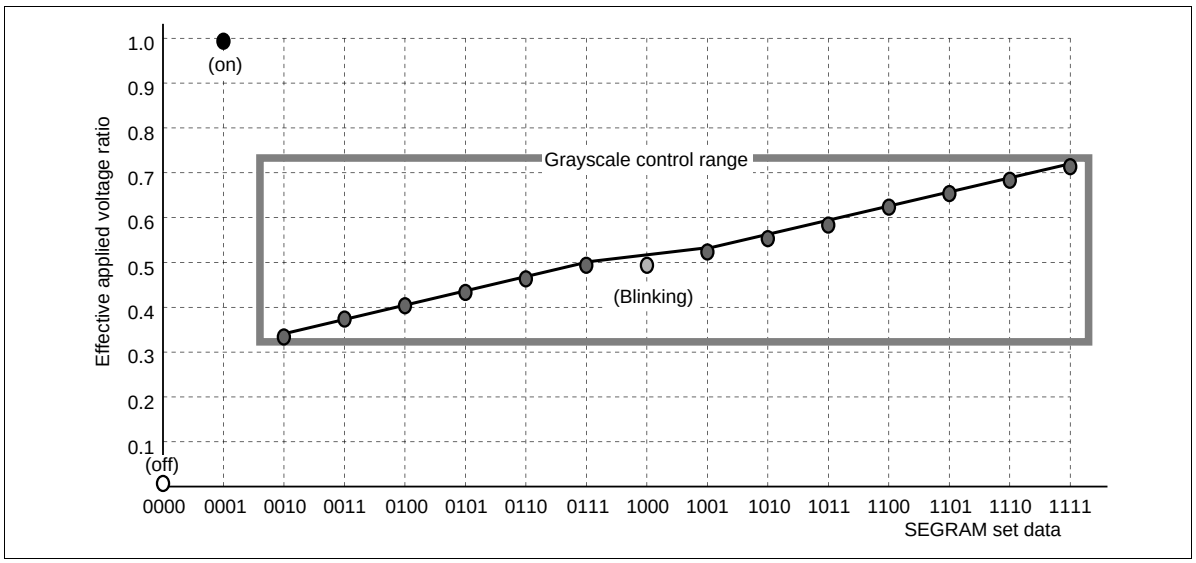


Figure 51 Relationship between SEGRAM Set Data and Effective Applied Voltage

Table 45 Relationship between SEGRAM Data and Blinking Control Segment Display (Blinking Control Segment Driver)

SEGRAM Data Setting				LCD Display Control for	SEGRAM Data Setting				LCD Display Control for
DB3	DB2	DB1	DB0	COMS1 Segment	DB7	DB6	DB5	DB4	COMS2 Segment
0	*1	*1	0	0 (Always unlit)	0	*1	*1	0	0 (Always unlit)
0	*1	*1	1	1 (Always lit)	0	*1	*1	1	1 (Always lit)
1	*1	*1	0	Blinking display *2	1	*1	*1	0	Blinking display *2
1	*1	*1	1	Double-speed blinking display *3	1	*1	*1	1	Double-speed blinking display *3

Notes: 1. 0 or 1.

2. Blinking is achieved by repeatedly turning on the segment for 32 frames and turning it off for the next 32 frames.
3. Double-speed blinking is achieved by repeatedly turning on the segment for16 frames and turning it off for the next 16 frames.

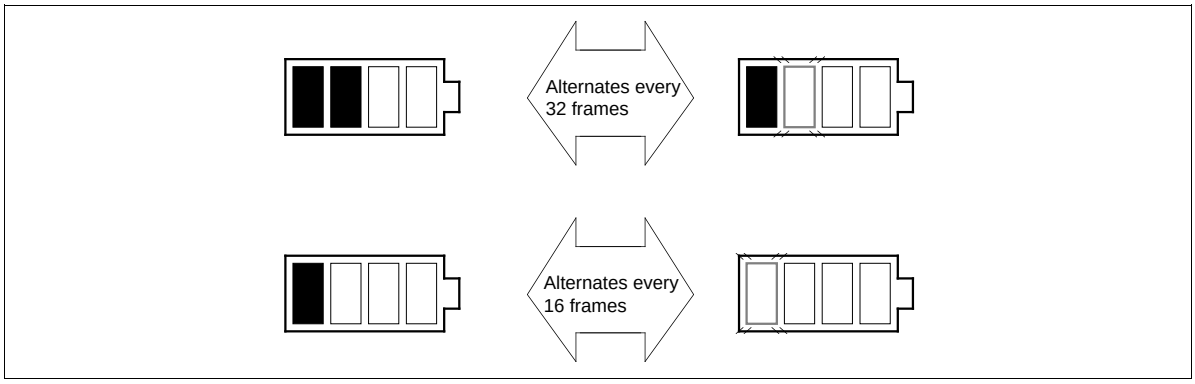


Figure 52 Blinking Control Segment Display

Line-Cursor Display

The HD66724/HD66725 can assign a cursor attribute to an entire line corresponding to the address counter value by setting the LC bit to 1. One of three line-cursor modes can be selected: a black-white inverting cursor (B/W = 1), an underline cursor (C = 1), and a blink cursor (B = 1). The cycle for a blink cursor is 32 frames. These line-cursors are suitable for highlighting an index and/or marker, or for indicating an item in a menu with a cursor or an underline.

Table 46 Address Counter Value and Line-Cursor

Address Counter Value (AC)	Selected Line for Line-Cursor
00H to 0FH	Entire 1st line (16 characters)
10H to 1FH	Entire 2nd line (16 characters)
20H to 2FH	Entire 3rd line (16 characters)
30H to 3FH	Entire 4th line (16 characters)
40H to 4FH	Entire 5th line (16 characters)

Normal Display (LC = 0)

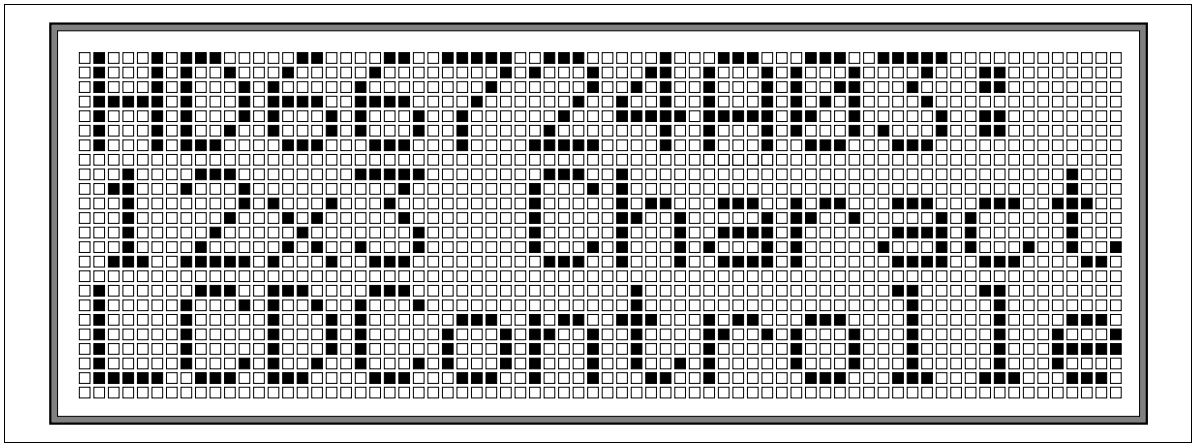


Figure 53 Normal Display

Black-White Reversed Cursor (LC = 1, B/W = 1)

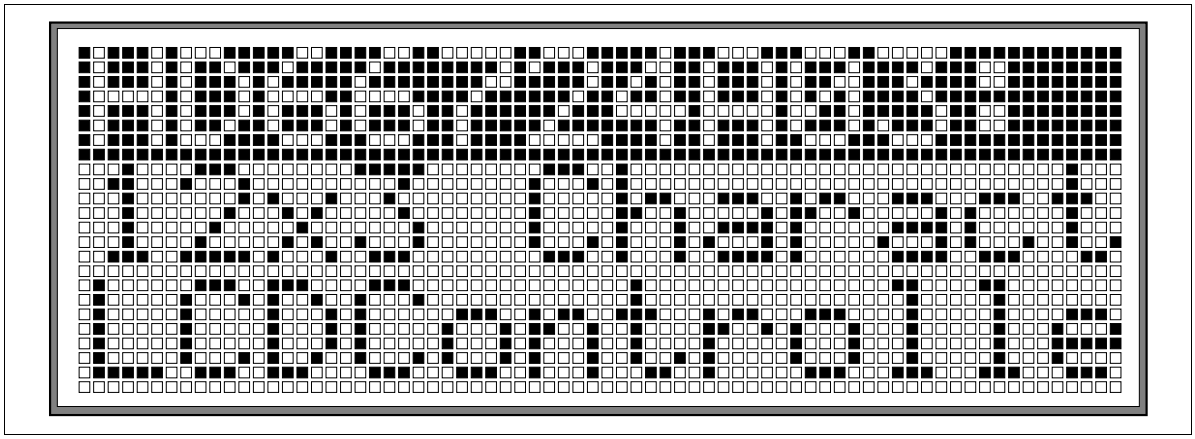


Figure 54 Black-White Reversed Cursor

Underline Cursor (LC = 1, C = 1)

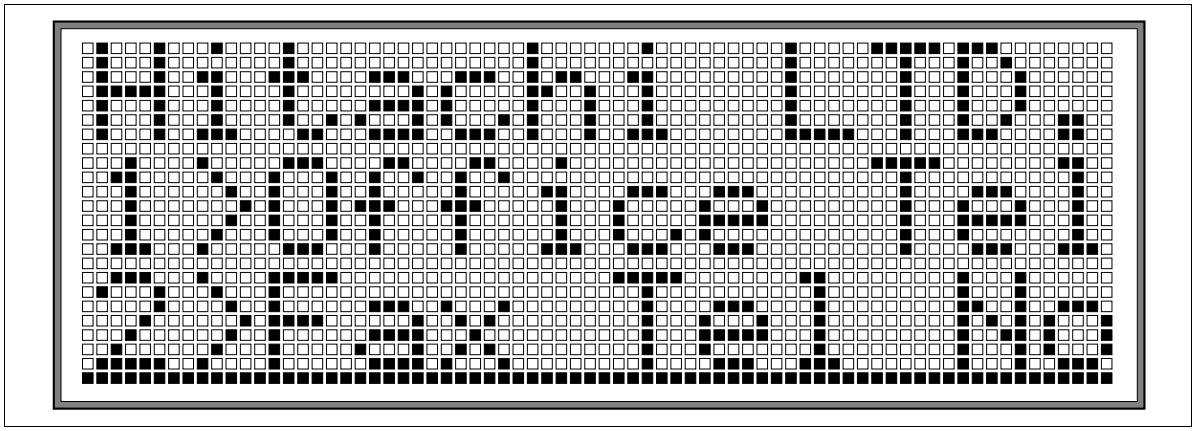


Figure 55 Underline Cursor

Blink Cursor (LC = 1, B = 1)

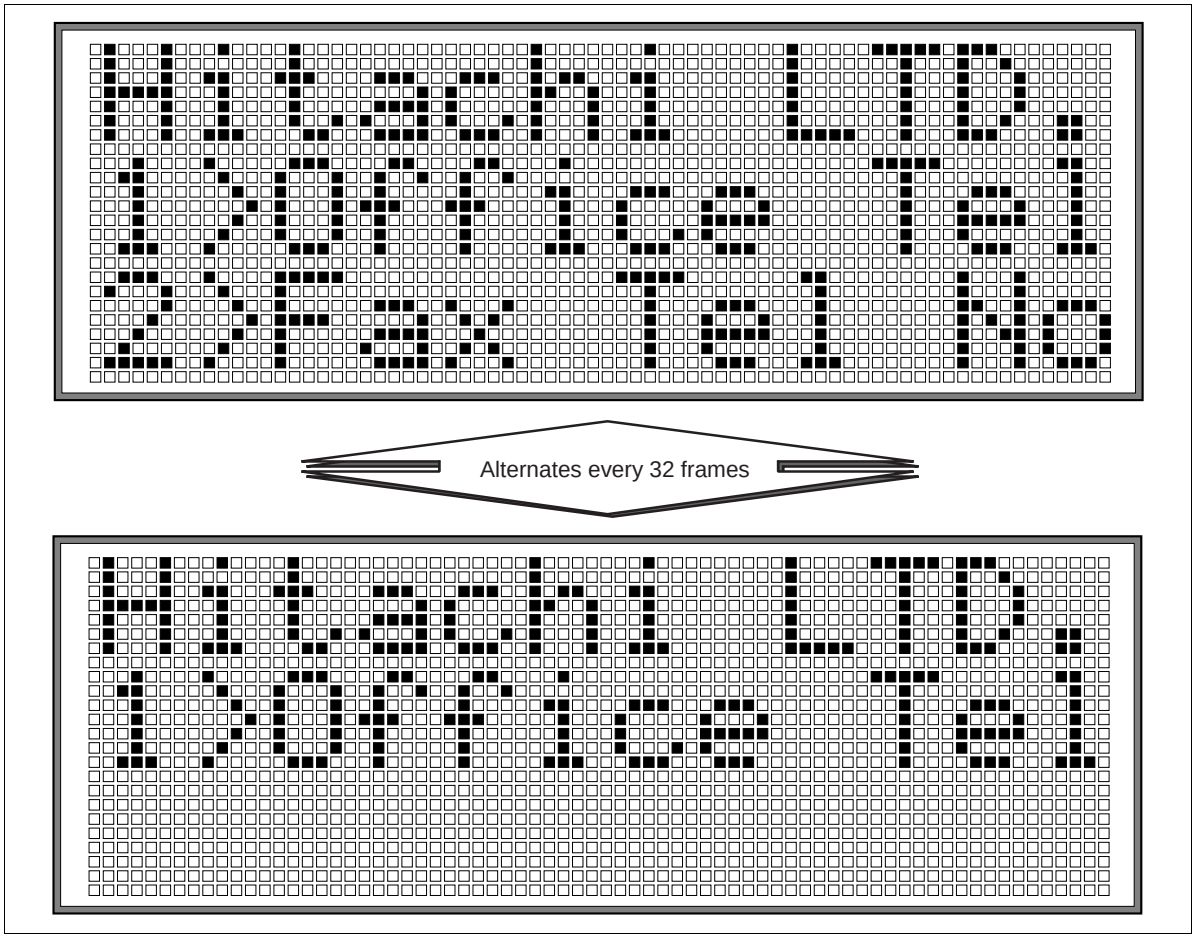


Figure 56 Blink Cursor

Partial-Display-On Function

The HD66724/HD66725 can program the liquid crystal display drive duty ratio setting (NL2-0 bits), liquid crystal display drive bias value selection (BS2-0 bits), boost output level selection (BT1/0 bit) and contrast adjustment (CT4-0 bits). In the three-line display mode (1/26 duty ratio), the HD66724/HD66725 can drive only one line in the center of the screen by combining these register functions and the centering display (CEN bit) function. This is called partial-display-on. Lowering the liquid crystal display drive duty ratio as required saves the liquid crystal display drive voltage, thus reducing internal current consumption. This is suitable for calendar or time display, which needs to be continuous in the system standby state with minimal current consumption. Here, the non-displayed lines are constantly driven by the deselection level voltage, thus turning off the LCD for the lines.

In general, lowering the liquid crystal display drive duty ratio decreases the optimum liquid crystal display drive voltage and liquid crystal display drive bias value.

Table 47 Partial-Display-On Function

Item	Normal 3-Line Display	Partially-On Display
Character display	1st to 3rd lines displayed	Only one line in the center of the screen
Segment display	Possible (144)	Possible (144)
Centering display	Not necessary (CEN = 0)	Possible (CEN = 1)
LCD drive duty ratio	1/26 (NL2/1/0 = 011)	1/10 (NL2/1/0 = 001) possible
LCD drive bias value (optimum)	1/6 (BS2-0 = 001)	1/4 (BS2-0 = 101)
LCD drive voltage	Adjustable using BT1/0 and CT4-0	Adjustable using BT1/0 and CT4-0
Frame frequency (fosc = 32 kHz)	77 Hz	80 kHz

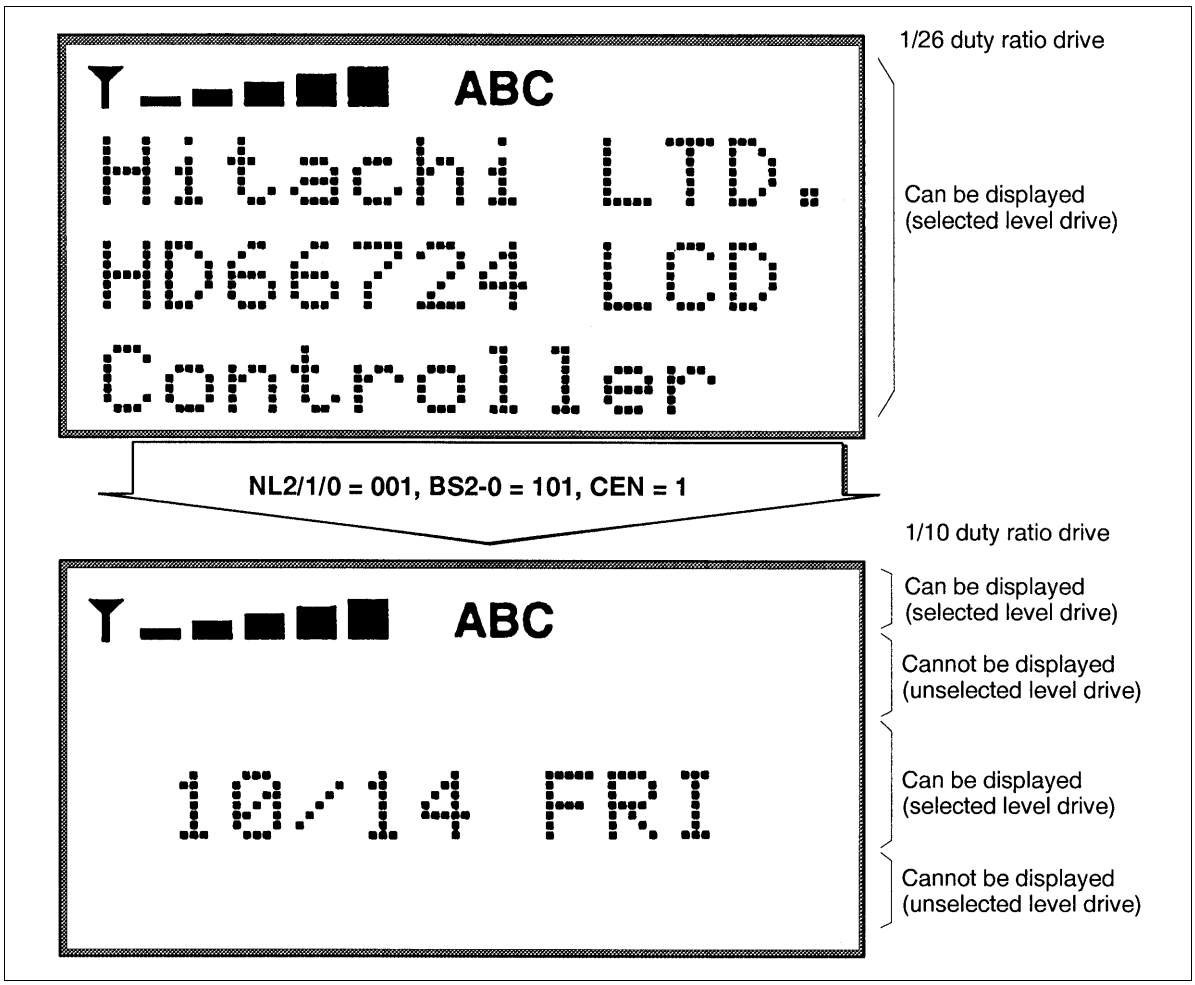


Figure 57 Partial-On Display (Date and Time Indicated)

Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66724/HD66725 in the sleep mode, where the device stops all internal display operations except for key scan operations, thus reducing current consumption. Specifically, LCD drive is completely halted. Here, all the SEG (SEG1 to SEG72 (96)) and COM (COM1 to COM24, COMS1/2) pins output the GND level, resulting in no display. If the AMP bit is set to 0 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

The key scan circuit operates normally in the sleep mode, thus allowing normal key scan and key scan interrupt generation. For details, refer to the Key Scan Control section and Key Scan Interrupt (Wake-up Function) section.

Table 48 Comparison of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)
Character display	Turned off	Turned off
Segment display	Turned off	Turned off
R-C oscillation	Operates normally	Halted
Key scan	Can operate normally	Halted but IRQ* can be generated

Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66724/HD66725 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillator, thus further reducing current consumption compared to that in the sleep mode. Specifically, character and segment displays, which are controlled by the multiplexing drive method, are completely halted. Here, all the SEG (SEG1 to SEG72 (96)) and COM (COM1 to COM24, COMS1/2) pins output the GND level, resulting in no display. If the AMP bit is set to 0 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than those for the start-oscillator instruction and the key scan interrupt generation enable instruction. To cancel the standby mode, issue the start oscillator instruction to stabilize R-C oscillation before setting the STB bit to 0.

Although key scan is halted in the standby mode, the HD66724/HD66725 can detect eight key inputs connected with strobe signal KST0, thus generating key scan interrupt (IRQ*). This means, the system can be activated from a completely inactive state. For details, refer to the Key Scan Interrupt (Wake-Up Function) section.

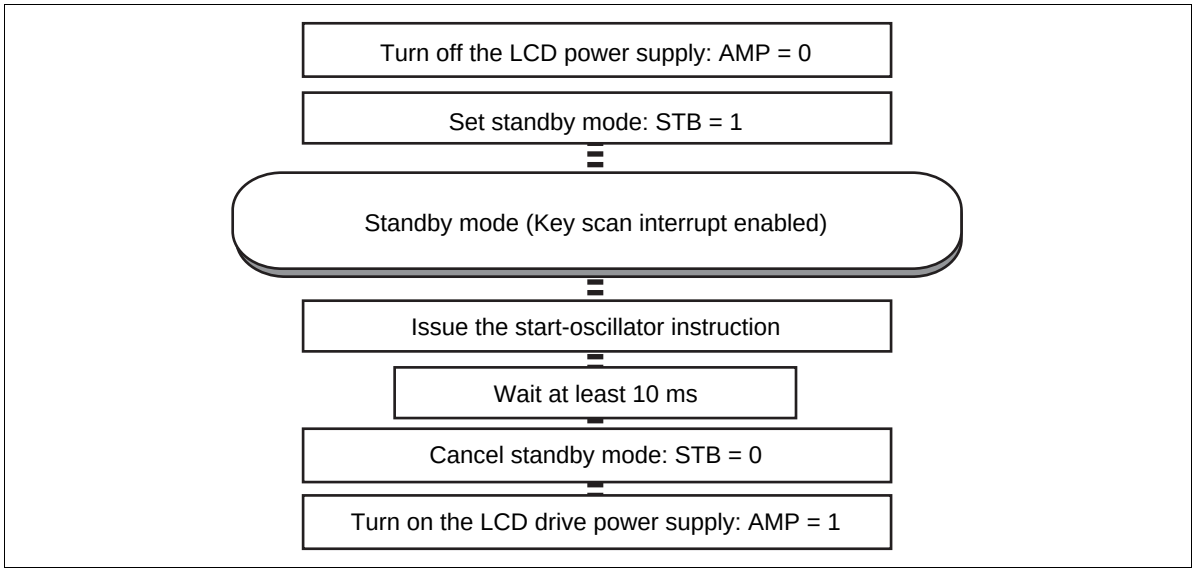


Figure 58 Procedure for Setting and Canceling Standby Mode

Absolute Maximum Ratings *

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	V_{LCD} – GND	V	–0.3 to +7.0	1, 2
Input voltage	Vt	V	–0.3 to V_{CC} + 0.3	1
Operating temperature	Topr	°C	–40 to +85	
Storage temperature	Tstg	°C	–55 to +110	4

Note: If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 1.8 to 5.5 V, Ta = –40 to +85°C*[3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V		5, 6
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 1.8 to 2.7 V	5, 6
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V	5, 6
Output high voltage (1) (SDA, DB0-7 pins)	V_{OH1}	0.75 V_{CC}	—	—	V	I_{OH} = –0.1 mA	5, 7
Output low voltage (1) (SDA,DB0-7 pins)	V_{OL1}	—	—	0.2 V_{CC}	V	V_{CC} = 1.8 to 2.7 V, I_{OL} = 0.1 mA	5
Output low voltage (1) (SDA,DB0-7 pins)	V_{OL1}	—	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V, I_{OL} = 0.1 mA	5
Output high voltage (2) (KST0-7, IRQ* pins)	V_{OH2}	0.7 V_{CC}	—	—	V	$-I_{OH}$ = 0.5 µA, V_{CC} = 3 V	5
Output low voltage (2) (KST0-7, IRQ* pins)	V_{OL2}	—	—	0.2 V_{CC}	V	I_{OL} = 0.1 mA	5
Output high voltage (3) (PORT0-2 pins)	V_{OH3}	0.75 V_{CC}	—	—	V	$-I_{OH}$ = 0.1mA	5
Output low voltage (3) (PORT0-2 pins)	V_{OL3}	—	—	0.2 V_{CC}	V	I_{OL} = 0.1mA	5
Driver ON resistance (COM pins)	R_{COM}	—	3	20	kΩ	±Id = 0.05 mA, V_{LCD} = 5 V	8
Driver ON resistance (SEG pins)	R_{SEG}	—	3	30	kΩ	±Id = 0.05 mA, V_{LCD} = 5 V	8
I/O leakage current	I_{Li}	–1	—	1	µA	Vin = 0 to V_{CC}	9
Pull-up MOS current (KIN0-7, DB0-7, SDA pins)	$-I_p$	1	10	40	µA	V_{CC} = 3 V, Vin = 0 V	5
Current consumption during normal operation (V_{CC}–GND)	I_{OP}	—	20	35	µA	R-C oscillation, V_{CC} = 3 V, f_{OSC} = 32 kHz (1/26 duty)	10, 11
Current consumption during sleep mode (V_{CC}–GND)	I_{SL}	—	11	—	µA	R-C oscillation, V_{CC} = 3 V, f_{OSC} = 32 kHz (1/26 duty)	10, 11
Current consumption during standby mode (V_{CC}–GND)	I_{ST}	—	0.1	5	µA	No R-C oscillation, V_{CC} = 3 V, Ta = 25°C	10, 11
LCD drive power supply current (V_{LCD}–GND)	I_{EE}	—	17	35	µA	V_{LCD} – GND = 5.5 V, f_{OSC} = 32 kHz	11
LCD drive voltage (V_{LCD} – GND)	V_{LCD}	3.0	—	6.5	V		12

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Double-boost output voltage (VLOUT pin)	V_{UP2}	5.5	5.9	—	V	V_{CC} = Vci = 3.0 V, I_O = 0.03 mA, C = 1 µF, f_{OSC} = 32 kHz, Ta = 25°C	15
Triple-boost output voltage (VLOUT pin)	V_{UP3}	6.1	6.5	—	V	V_{CC} = Vci = 2.2 V, I_O = 0.03 mA, C = 1 µF, f_{OSC} = 32 kHz, Ta = 25°C	15
Maximum boost output voltage	V_{UP2} V_{UP3}	V_{CC}	—	6.5	V		15

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 1.8 to 5.5 V, Ta = –40 to +85°C*[3])

Clock Characteristics (V_{CC} = 1.8 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	fcp	15	32	100	kHz		13
External clock duty ratio	Duty	45	50	55	%		13
External clock rise time	trcp	—	—	0.2	µs		13
External clock fall time	tfcp	—	—	0.2	µs		13
CR oscillation frequency with external Rf	f_{OSC1}	25	32	40		Rf = 620 kΩ, V_{CC} = 3 V	14
CR oscillation frequency with internal Rf	f_{OSC2}	19	32	45		R1-osc2: short circuited V_{CC} = 3 V	

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

68-System Bus Interface Timing Characteristics

(Vcc = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	800	—	—	ns	Figure 65
	Read		1200	—	—		
Enable high-level pulse width	Write	PW_{EH}	150	—	—	ns	Figure 65
	Read		450	—	—		
Enable low-level pulse width	Write	PW_{EL}	300	—	—	ns	Figure 65
	Read		450	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 65
Setup time (RS, R/W, to E, CS*)		t_{ASE}	60	—	—	ns	Figure 65
Address hold time		t_{AHE}	20	—	—	ns	Figure 65
Write data set-up time		t_{DSWE}	60	—	—	ns	Figure 65
Write data hold time		t_{HE}	20	—	—	ns	Figure 65
Read data delay time		t_{DDRE}	—	—	400	ns	Figure 65
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 65

(Vcc = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	500	—	—	ns	Figure 65
	Read		700	—	—		
Enable high-level pulse width	Write	PW_{EH}	80	—	—	ns	Figure 65
	Read		300	—	—		
Enable low-level pulse width	Write	PW_{EL}	250	—	—	ns	Figure 65
	Read		300	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 65
Setup time (RS, R/W, to E, CS*)		t_{ASE}	60	—	—	ns	Figure 65
Address hold time		t_{AHE}	20	—	—	ns	Figure 65
Write data set-up time		t_{DSWE}	60	—	—	ns	Figure 65
Write data hold time		t_{HE}	20	—	—	ns	Figure 65
Read data delay time		t_{DDRE}	—	—	250	ns	Figure 65
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 65

80-System Bus Interface Timing Characteristics

(Vcc = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	800	—	—	ns	Figure 66
	Read	t_{CYCR}	1200	—	—	ns	Figure 66
Write low-level pulse width		PW_{LW}	150	—	—	ns	Figure 66
Read low-level pulse width		PW_{LR}	450	—	—	ns	Figure 66
Write high-level pulse width		PW_{HW}	300	—	—	ns	Figure 66
Read high-level pulse width		PW_{HR}	450	—	—	ns	Figure 66
Write/Read rise/fall time		t_{WRr} , $_{WRf}$	—	—	25	ns	Figure 66
Setup time (RS to CS*, WR*, RD*)		t_{AS}	60	—	—	ns	Figure 66
Address hold time		t_{AH}	20	—	—	ns	Figure 66
Write data set-up time		t_{DSW}	60	—	—	ns	Figure 66
Write data hold time		t_{H}	20	—	—	ns	Figure 66
Read data delay time		t_{DDR}	—	—	400	ns	Figure 66
Read data hold time		t_{DHR}	5	—	—	ns	Figure 66

(Vcc = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	500	—	—	ns	Figure 66
	Read	t_{CYCR}	700	—	—	ns	Figure 66
Write low-level pulse width		PW_{LW}	80	—	—	ns	Figure 66
Read low-level pulse width		PW_{LR}	300	—	—	ns	Figure 66
Write high-level pulse width		PW_{HW}	250	—	—	ns	Figure 66
Read high-level pulse width		PW_{HR}	300	—	—	ns	Figure 66
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns	Figure 66
Setup time (RS to CS*, WR*, RD*)		t_{AS}	60	—	—	ns	Figure 66
Address hold time		t_{AH}	20	—	—	ns	Figure 66
Write data set-up time		t_{DSW}	60	—	—	ns	Figure 66
Write data hold time		t_{H}	20	—	—	ns	Figure 66
Read data delay time		t_{DDR}	—	—	250	ns	Figure 66
Read data hold time		t_{DHR}	5	—	—	ns	Figure 66

Clock-Synchronized Serial Interface Timing Characteristics (V_{CC} = 1.8 to 5.5 V)

(V_{CC} = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	Write	t_{SCYC}	0.5	—	20	µs	Figure 67
	Read	t_{SCYC}	1	—	20	µs	Figure 67
Serial clock high-level width	Write	t_{SCH}	230	—	—	ns	Figure 67
	Read	t_{SCH}	480	—	—	ns	Figure 67
Serial clock low-level width	Write	t_{SCL}	230	—	—	ns	Figure 67
	Read	t_{SCL}	480	—	—	ns	Figure 67
Serial clock rise/fall time		t_{SCf}, t_{SCr}	—	—	20	ns	Figure 67
Chip select set-up time		t_{CSU}	60	—	—	ns	Figure 67
Chip select hold time		t_{CH}	200	—	—	ns	Figure 67
Serial input data set-up time		t_{SISU}	100	—	—	ns	Figure 67
Serial input data hold time		t_{SIH}	100	—	—	ns	Figure 67
Serial output data delay time		t_{SOD}		—	400	ns	Figure 67
Serial output hold time		t_{SOH}	5	—	—	ns	Figure 67

(V_{CC} = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	Write	t_{SCYC}	0.2	—	20	µs	Figure 67
	Read	t_{SCYC}	0.5	—	20	µs	Figure 67
Serial clock high-level width	Write	t_{SCH}	80	—	—	ns	Figure 67
	Read	t_{SCH}	230	—	—	ns	Figure 67
Serial clock low-level width	Write	t_{SCL}	80	—	—	ns	Figure 67
	Read	t_{SCL}	230	—	—	ns	Figure 67
Serial clock rise/fall time		t_{SCf}, t_{SCr}	—	—	20	ns	Figure 67
Chip select setup time		t_{CSU}	60	—	—	ns	Figure 67
Chip select hold time		t_{CH}	200	—	—	ns	Figure 67
Serial input data set-up time		t_{SISU}	40	—	—	ns	Figure 67
Serial input data hold time		t_{SIH}	40	—	—	ns	Figure 67
Serial output data delay time		t_{SOD}		—	200	ns	Figure 67
Serial output hold time		t_{SOH}	5	—	—	ns	Figure 67

Reset Timing Characteristics (V_{CC} = 1.8 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	1	—	—	ms	Figure 68

Electrical Characteristics Notes

1. All voltage values are referred to GND = 0 V. If the LSI is used above the absolute maximum ratings, it may become permanently damaged. Using the LSI within the given electrical characteristic is strongly recommended to ensure normal operation. If these electrical characteristics are exceeded, the LSI may malfunction or exhibit poor reliability.
2. VLCD > GND must be maintained.
3. For bare die products, specified at 85˚C.
4. For bare die products, specified by the common die shipment specification.
5. The following three circuits are I/O pin configurations (figure 59).

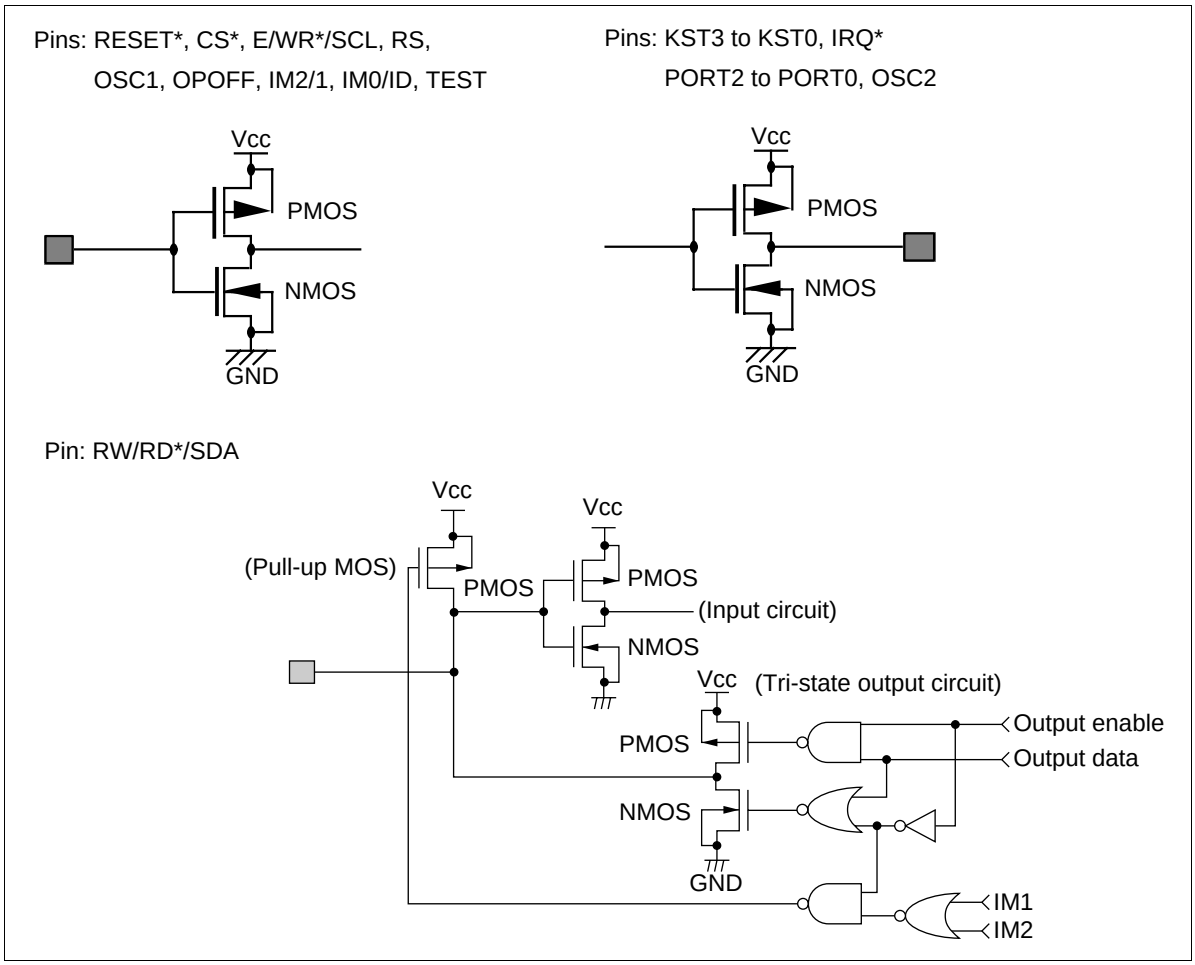


Figure 59 I/O Pin Configuration

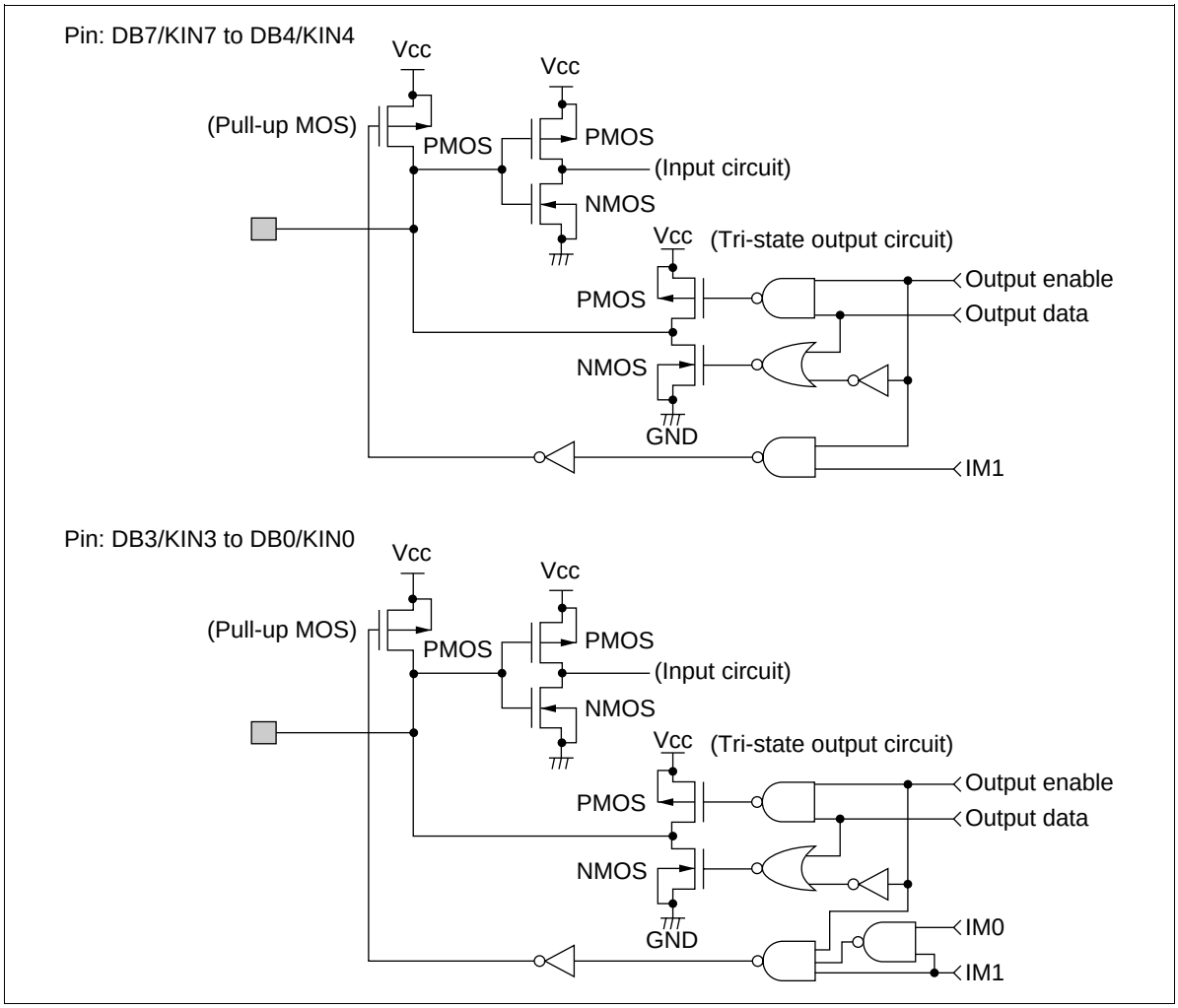


Figure 59 I/O Pin Configuration (cont)

6. The TEST pin must be grounded and the IM2/1, IM0/ID, and OPOFF pins must be grounded or connected to Vcc.
7. Corresponds to the high output for clock-synchronized serial interface.
8. Applies to the resistor value (RCOM) between power supply pins V1OUT, V2OUT, V5OUT, GND and common signal pins (COM1 to COM24, COMS1 and COMS2), and resistor value (RSEG) between power supply pins V1OUT, V3OUT, V4OUT, GND and segment signal pins (SEG1 to SEG72 (96)), when current Id is flown through all driver output pins.
9. This excludes the current flowing through pull-up MOSs and output drive MOSs.
10. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating.
11. The following shows the relationship between the operation frequency (fosc) and current consumption (Icc) (figure 60).

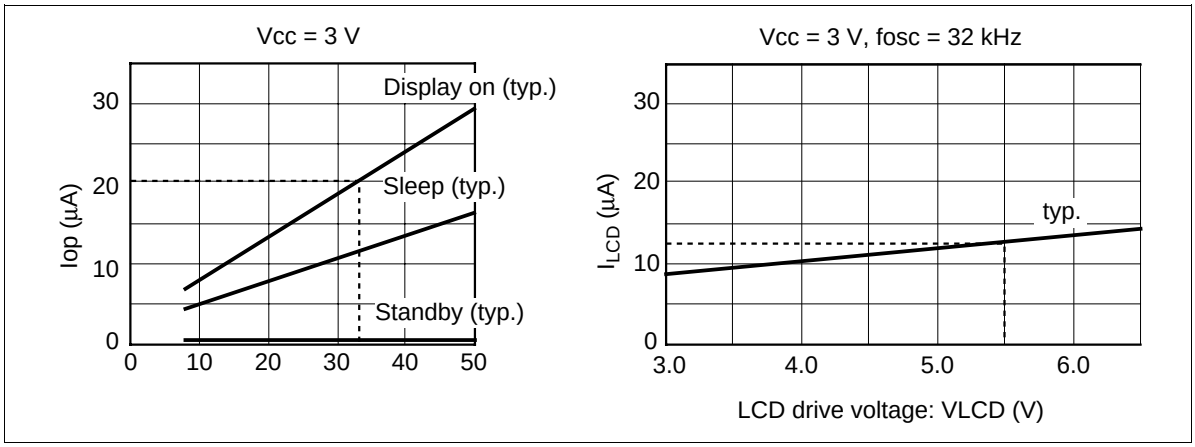


Figure 60 Relationship between the Operation Frequency and Current Consumption

12. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (Vcc, V1, V2, V3, V4, V5) when there is no load.

13. Applies to the external clock input (figure 61).

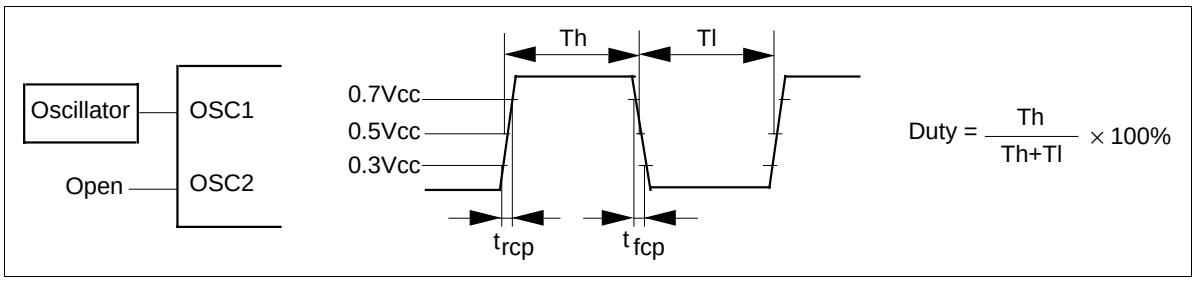
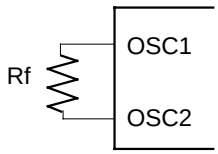


Figure 61 External Clock Supply

14. Applies to the internal oscillator operations using oscillation resistor Rf (figure 62).



Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

External resistance (Rf)	CR oscillation frequency : fosc				
	Vcc = 1.8 V	Vcc = 2.2 V	Vcc = 3.0 V	Vcc = 4.0 V	Vcc = 5.0 V
390 kΩ	40 kHz	45 kHz	48 kHz	50 kHz	51 kHz
510 kΩ	33 kHz	36 kHz	38 kHz	40 kHz	41 kHz
560 kΩ	30 kHz	33 kHz	35 kHz	36 kHz	37 kHz
620 kΩ	28 kHz	30 kHz	32 kHz	33 kHz	33 kHz
680 kΩ	26 kHz	29 kHz	30 kHz	31 kHz	31 kHz
750 kΩ	24 kHz	27 kHz	28 kHz	29 kHz	29 kHz

Figure 62 Internal Oscillation

15. Booster characteristics test circuits are shown in figure 63.

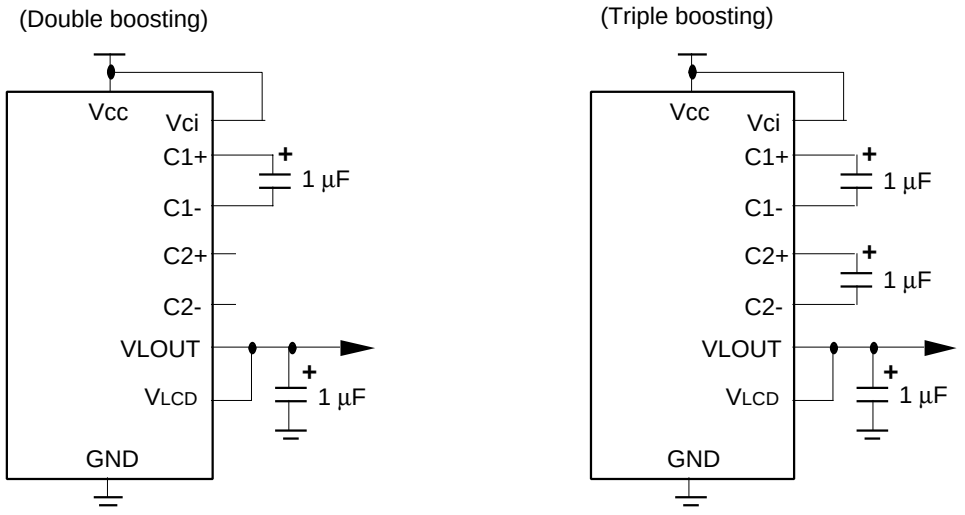
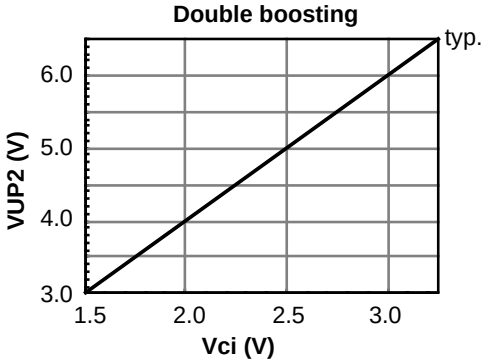


Figure 63 Booster

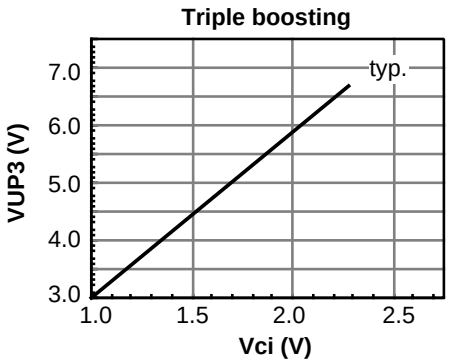
Referential data

VUP2 = VLCD – GND; VUP3 = VLCD – GND

(i) Relation between the obtained voltage and input voltage

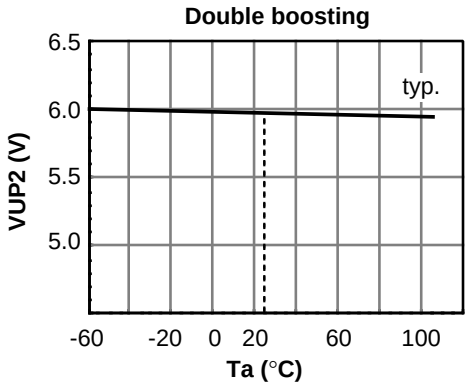


Vci = Vcc, fosc = 32 kHz, Ta = 25˚C

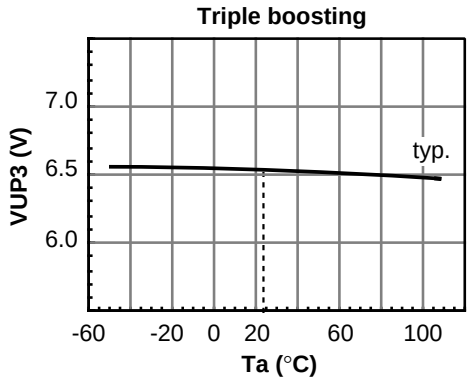


Vci = Vcc, fosc = 32 kHz, Ta = 25˚C

(ii) Relation between the obtained voltage and temperature <T.B.D.>



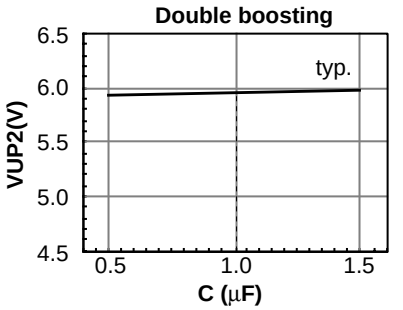
Vci = Vcc = 3.0 V, fosc = 32 kHz, Io = 30 µA



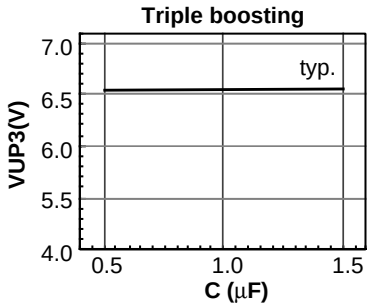
Vci = Vcc = 2.2 V, fosc = 32 kHz, Io = 30 µA

Figure 63 Booster (cont)

(iii) Relation between the obtained voltage and capacitance

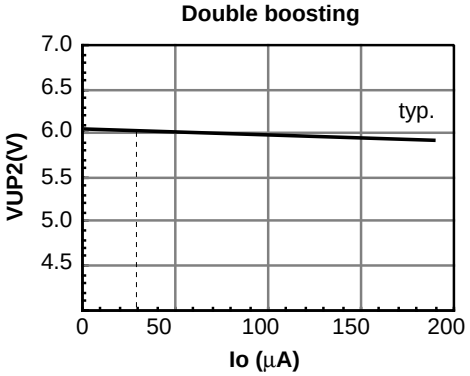


Vci = Vcc = 3.0 V, fosc = 32 kHz, Io = 30 μA

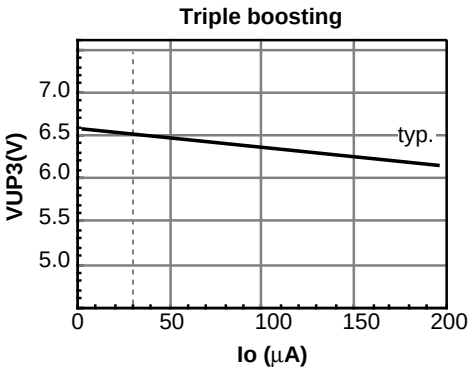


Vci = Vcc = 2.2 V, fosc = 32 kHz, Io = 30 μA

(iv) Relation between the obtained voltage and current <T.B.D.>



Vci = Vcc = 2.2 V, fosc = 32 kHz, Ta = 25°C



Vci = Vcc = 2.2 V, fosc = 32 kHz, Ta = 25°C

Figure 63 Booster (cont)

Load Circuits

AC Characteristics Test Load Circuits

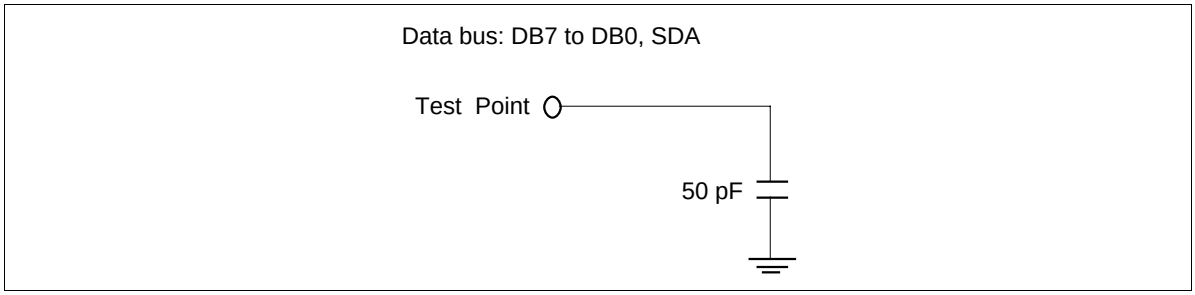
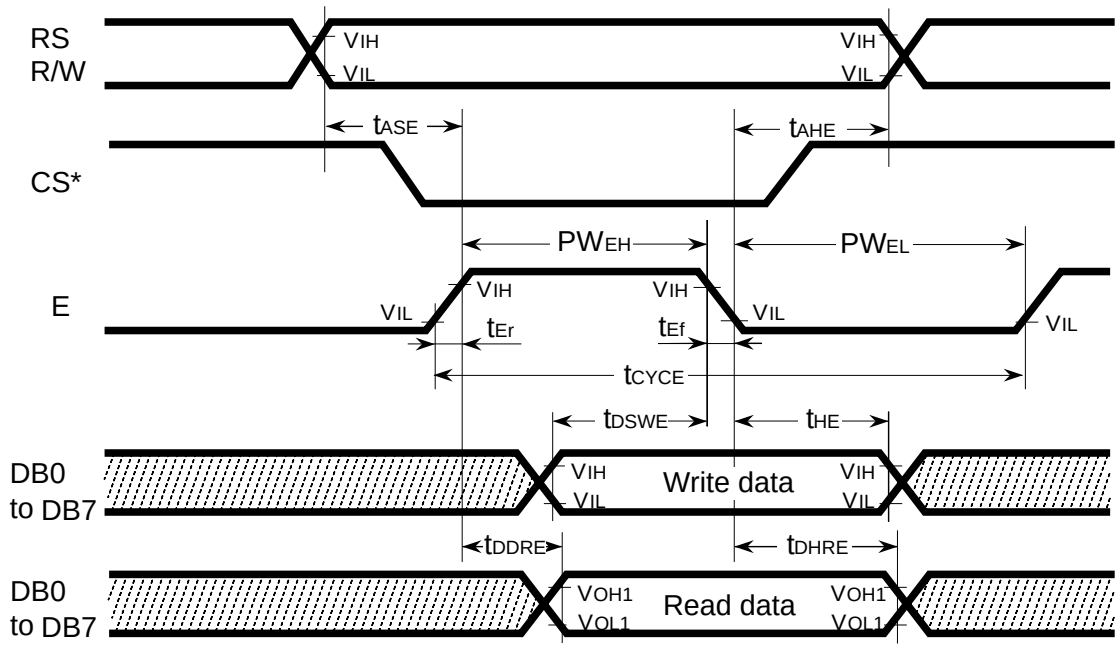


Figure 64 Load Circuit

Timing Characteristics

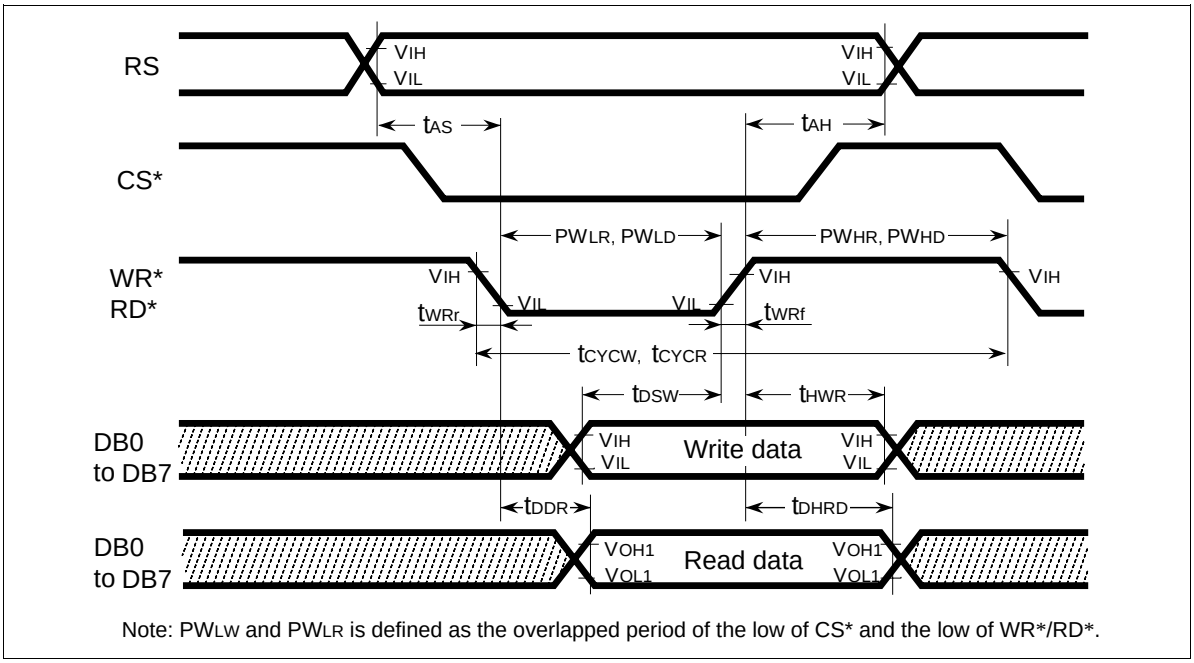
68-System Bus Operation



Note: PW_{EH} is defined as the overlapped period of the Low of CS* and the high of E.

Figure 65 68-System Bus Timing

80-System Bus Operation



Note: PWLW and PWLR is defined as the overlapped period of the low of CS* and the low of WR*/RD*.

Figure 66 80-System Bus Timing

Clock-Synchronized Serial Operation

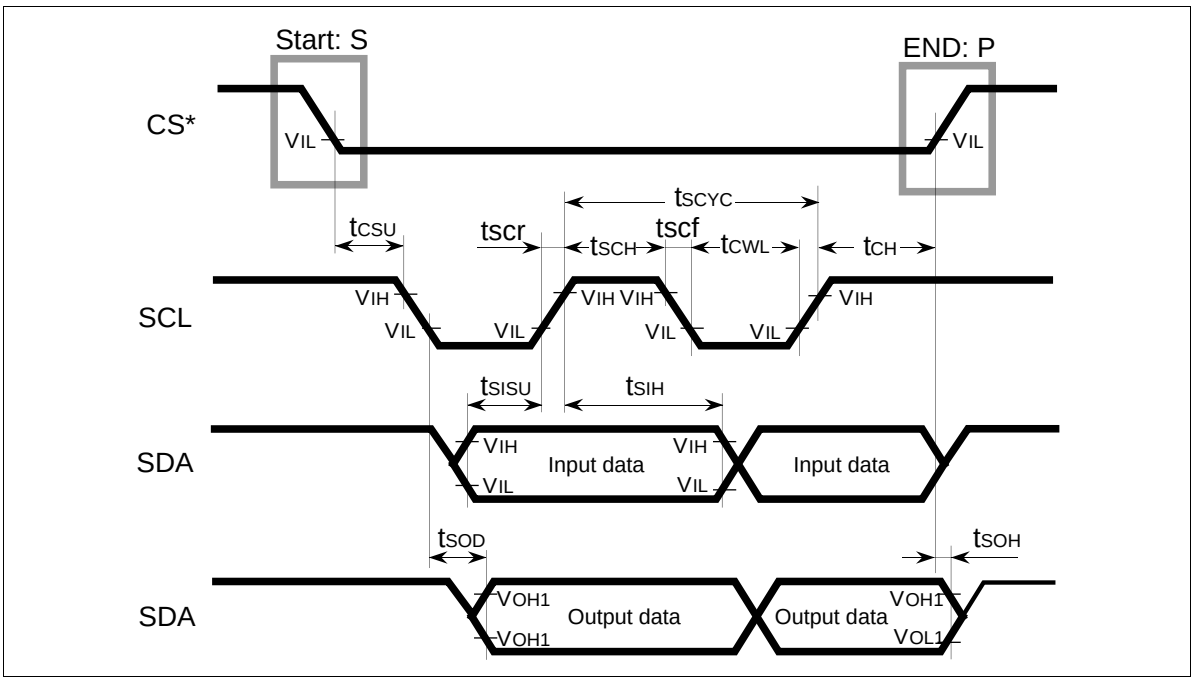


Figure 67 Clock-synchronized Serial Interface Timing

Reset Operation

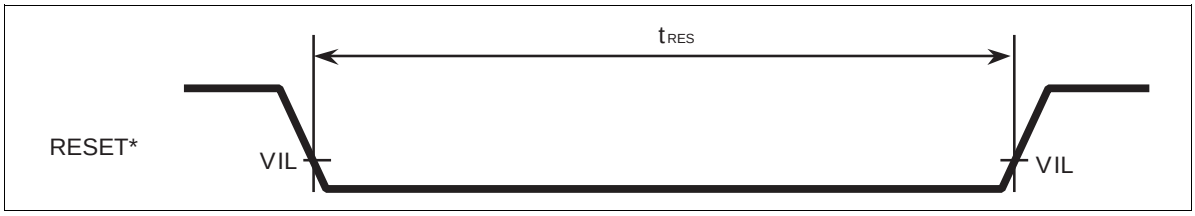


Figure 68 Reset Timing

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