

To all our customers

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**Information regarding change of names mentioned  
within this document, to Renesas Technology Corp.**

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On April 1<sup>st</sup> 2003 the following semiconductor operations were transferred to Renesas Technology Corporation: operations covering microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.).

Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have all been changed to Renesas Technology Corporation.

Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Thank you for your understanding.

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Renesas Technology Corp.  
April 1, 2003

# HD66762

(128 x 136-dot Graphics LCD Controller/Driver for 256 Colors)

# HITACHI

Rev 1.0  
October, 2001

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## Description

The HD66762, color-graphics LCD controller and driver LSI, displays 128-by-136-dot graphics for 256 STN colors. The HD66762's bit-operation functions and a 16-bit high-speed bus interface enable efficient data transfer and high-speed rewriting of data to the graphics RAM.

The HD66762 has various functions for reducing the power consumption of an LCD system, such as low-voltage operation of 1.8 V/min., a step-up circuit to generate a maximum of 12-times the LCD drive voltage from the supplied voltage, and voltage-followers to decrease the direct current flow in the LCD drive bleeder-resistors. Combining these hardware functions with software functions, such as a partial display with low-duty drive and standby and sleep modes, allows precise power control. The HD66762 is suitable for any mid-sized or small portable battery-driven product requiring long-term driving capabilities, such as digital cellular phones supporting a WWW browser, bi-directional pagers, and small PDAs.

## Features

- 128 × 136-dot graphics display LCD controller/driver for 256 STN colors
- Flickerless PWM grayscale drive
- 16/8-bit high-speed bus interface and clock synchronized serial interface
- Bit-operation functions for graphics processing:
  - Write-data mask function in bit units
  - Swap function of upper and lower bytes
  - Logical operation in pixel unit and conditional write function
- Various color-display control functions:
  - 256 out of 4,096 possible colors can be displayed at the same time (grayscale palette incorporated)
  - Vertical scroll display function in raster-row units
- Low-power operation supports:
  - V<sub>cc</sub> = 1.8 to 3.6 V (low voltage)
  - Common driving voltage = 10 to 38 V
  - Segment driving voltage = 2 to 4 V

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## HD66762

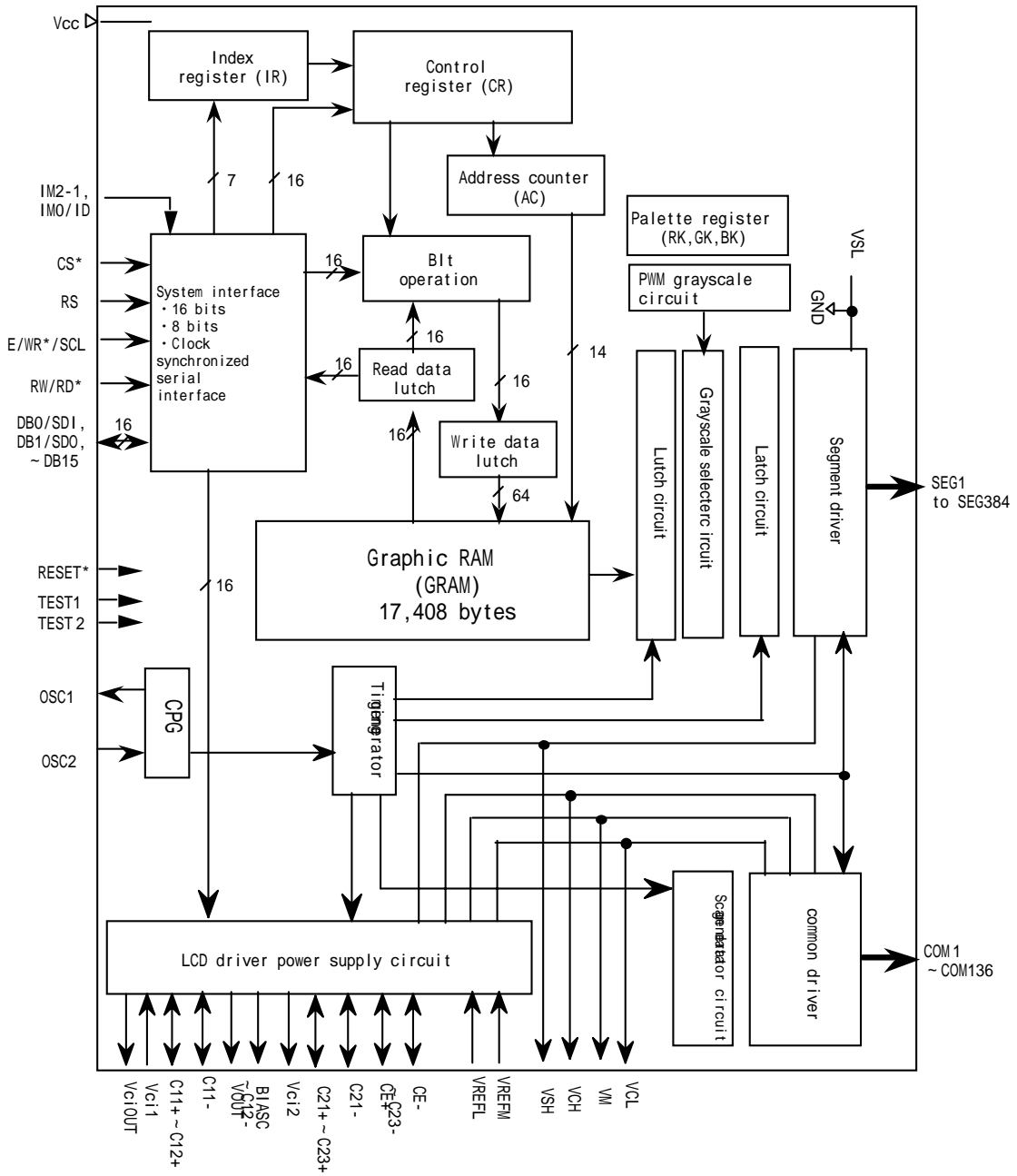
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- Maximum 12-times step-up circuit for liquid crystal drives voltage and voltage inverting circuit
- 128-step contrast adjuster and voltage followers to decrease direct current flow in the LCD drive bleeder-resistors
- Power-save functions such as the standby mode and sleep mode
- Partial LCD drive of two screens in any position
- Programmable drive duty ratios (1/16–1/136) and bias values (1/2–1/12) displayed on LCD
- Internal RAM capacity: 17,408 bytes
- 384-segment × 136-common liquid crystal display driver
- n-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Internal oscillation and hardware reset
- Shift change of segment and common drivers

### Type Name

<b>Types</b>	<b>External Dimensions</b>
HCD66762BP	Au-bumped chip
HD66762TB0	TCP

HD66762 Block Diagram

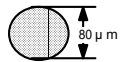


# HD66762

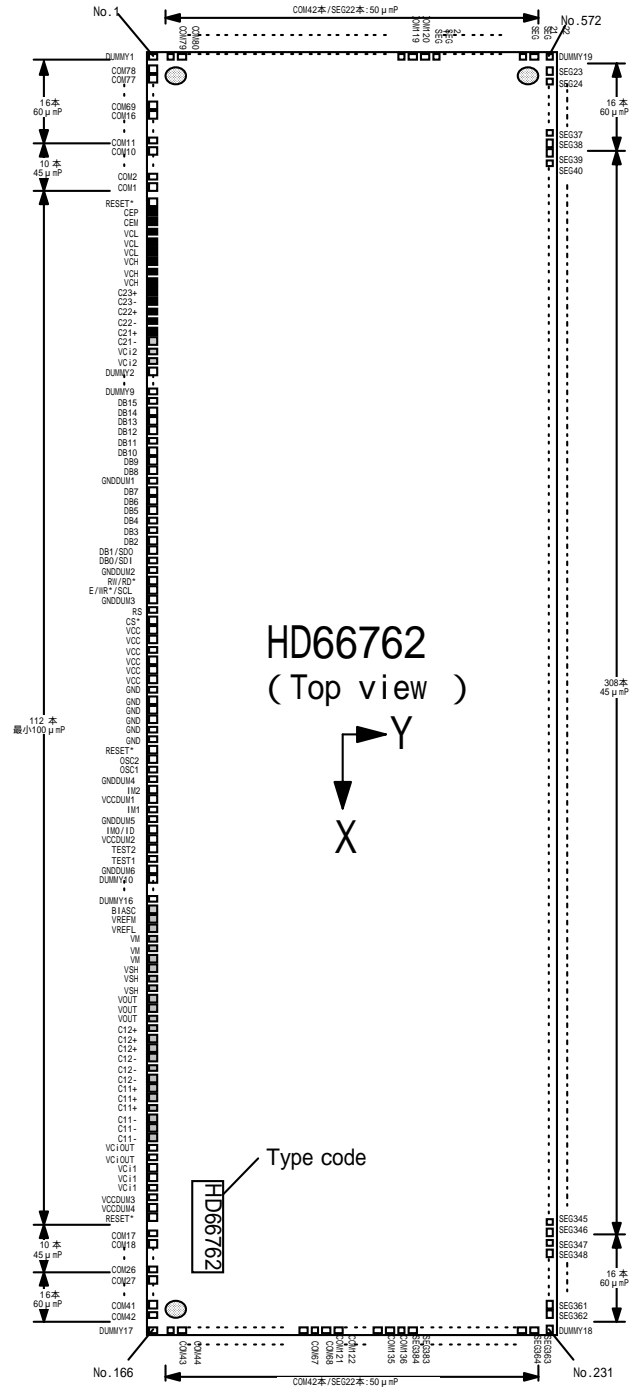
## HD66762 PAD Arrangement

Rev 0.5  
22.Aug.2001.

- Chip size : 16.40mm x 3.84mm
- Chip thickness : 550 μm (typ.)
- PAD coordinates : PAD center
- Coordinate origin : Chip center
- Au bump size (PAD number is shown in the bracket)
- (1) 80 μm x 80 μm  
DUMMY1, RESET\*, CEP ~ VCCDUM4, RESET\*, DUMMY17, DUMMY18, DUMMY19
- (2) 45 μm x 80 μm  
COM78 ~ COM11, COM27 ~ COM42, SEG362 ~ SEG347, SEG38 ~ SEG23
- (3) 30 μm x 80 μm  
COM10 ~ COM1, COM17 ~ COM26, SEG346 ~ SEG39
- (4) 80 μm x 35 μm  
COM43 ~ SEG363, SEG22 ~ COM79
- Au bump pitch : Refer to the PAD coordinates
- Au bump height : 15 μm (typ.)
- Numbers in figure corresponding PAD coordinate number
- Alloyment mark
- (1) A shape
- (2) Arrangement : 3 point
- (3) Coordinates (X, Y)  
(-7910, -1586) (-7910, 1586)  
(7910, -1586)



- High compressor 40V system
- ▣ Middle compressor 5 V system
- Normal compressor 3V system



HD66762 PAD Coordinate

HD66762PAD座標

ver0.0 2000.02.15作成

No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y
1	DUMMY1	-8047	-1728	81	VCC	-142	-1728	161	COM38	7646	-1728	241	SEG353	7346	1767
2	COM78	-7887	-1728	82	GND	-12	-1728	162	COM39	7706	-1728	242	SEG352	7286	1767
3	COM77	-7826	-1728	83	GND	88	-1728	163	COM40	7766	-1728	243	SEG351	7226	1767
4	COM76	-7766	-1728	84	GND	188	-1728	164	COM41	7826	-1728	244	SEG350	7166	1767
5	COM75	-7706	-1728	85	GND	288	-1728	165	COM42	7887	-1728	245	SEG349	7106	1767
6	COM74	-7646	-1728	86	GND	388	-1728	166	DUMMY17	8047	-1728	246	SEG348	7046	1767
7	COM73	-7586	-1728	87	GND	489	-1728	167	COM43	8047	-1573	247	SEG347	6986	1767
8	COM72	-7526	-1728	88	RESET*	683	-1728	168	COM44	8047	-1523	248	SEG346	6933	1767
9	COM71	-7466	-1728	89	OSC2	821	-1728	169	COM45	8047	-1473	249	SEG345	6883	1767
10	COM70	-7406	-1728	90	OSC1	958	-1728	170	COM46	8047	-1423	250	SEG344	6843	1767
11	COM69	-7346	-1728	91	GNDDUM4	1058	-1728	171	COM47	8047	-1373	251	SEG343	6798	1767
12	COM16	-7286	-1728	92	IM2	1159	-1728	172	COM48	8047	-1323	252	SEG342	6753	1767
13	COM15	-7226	-1728	93	VCCDUM1	1259	-1728	173	COM49	8047	-1273	253	SEG341	6708	1767
14	COM14	-7166	-1728	94	IM1	1359	-1728	174	COM50	8047	-1223	254	SEG340	6663	1767
15	COM13	-7106	-1728	95	GNDDUM5	1459	-1728	175	COM51	8047	-1173	255	SEG339	6618	1767
16	COM12	-7046	-1728	96	IM0/ID	1559	-1728	176	COM52	8047	-1123	256	SEG338	6573	1767
17	COM11	-6986	-1728	97	VCCDUM2	1659	-1728	177	COM53	8047	-1073	257	SEG337	6528	1767
18	COM10	-6933	-1728	98	TEST2	1759	-1728	178	COM54	8047	-1023	258	SEG336	6483	1767
19	COM9	-6883	-1728	99	TEST1	1859	-1728	179	COM55	8047	-973	259	SEG335	6438	1767
20	COM8	-6843	-1728	100	GNDDUM6	1959	-1728	180	COM56	8047	-923	260	SEG334	6393	1767
21	COM7	-6798	-1728	101	DUMMY10	2114	-1728	181	COM57	8047	-873	261	SEG333	6348	1767
22	COM6	-6753	-1728	102	DUMMY11	2214	-1728	182	COM58	8047	-823	262	SEG332	6303	1767
23	COM5	-6708	-1728	103	DUMMY12	2314	-1728	183	COM59	8047	-773	263	SEG331	6258	1767
24	COM4	-6663	-1728	104	DUMMY13	2414	-1728	184	COM60	8047	-723	264	SEG330	6213	1767
25	COM3	-6618	-1728	105	DUMMY14	2514	-1728	185	COM61	8047	-673	265	SEG329	6168	1767
26	COM2	-6573	-1728	106	DUMMY15	2614	-1728	186	COM62	8047	-623	266	SEG328	6123	1767
27	COM1	-6528	-1728	107	DUMMY16	2714	-1728	187	COM63	8047	-573	267	SEG327	6078	1767
28	RESET*	-6288	-1728	108	BIASC	2869	-1728	188	COM64	8047	-523	268	SEG326	6033	1767
29	CEP	-6158	-1728	109	VREFM	2969	-1728	189	COM65	8047	-473	269	SEG325	5988	1767
30	CEM	-6058	-1728	110	VREFL	3069	-1728	190	COM66	8047	-423	270	SEG324	5943	1767
31	VCL	-5864	-1728	111	VM	3169	-1728	191	COM67	8047	-373	271	SEG323	5898	1767
32	VCL	-5764	-1728	112	VM	3269	-1728	192	COM68	8047	-323	272	SEG322	5852	1767
33	VCL	-5663	-1728	113	VM	3370	-1728	193	COM121	8047	-273	273	SEG321	5807	1767
34	VCH	-5533	-1728	114	VSH	3470	-1728	194	COM122	8047	-222	274	SEG320	5762	1767
35	VCH	-5433	-1728	115	VSH	3570	-1728	195	COM123	8047	-172	275	SEG319	5717	1767
36	VCH	-5333	-1728	116	VSH	3670	-1728	196	COM124	8047	-122	276	SEG318	5672	1767
37	C23+	-5203	-1728	117	VOUT	3811	-1728	197	COM125	8047	-72	277	SEG317	5627	1767
38	C23-	-5103	-1728	118	VOUT	3911	-1728	198	COM126	8047	-22	278	SEG316	5582	1767
39	C22+	-5003	-1728	119	VOUT	4011	-1728	199	COM127	8047	28	279	SEG315	5537	1767
40	C22-	-4903	-1728	120	C12+	4153	-1728	200	COM128	8047	78	280	SEG314	5492	1767
41	C21+	-4803	-1728	121	C12+	4253	-1728	201	COM129	8047	128	281	SEG313	5447	1767
42	C21-	-4664	-1728	122	C12+	4353	-1728	202	COM130	8047	178	282	SEG312	5402	1767
43	VC12	-4564	-1728	123	C12-	4453	-1728	203	COM131	8047	228	283	SEG311	5357	1767
44	VC12	-4464	-1728	124	C12-	4553	-1728	204	COM132	8047	278	284	SEG310	5312	1767
45	DUMMY2	-4305	-1728	125	C12-	4653	-1728	205	COM133	8047	328	285	SEG309	5267	1767
46	DUMMY3	-4205	-1728	126	C11+	4753	-1728	206	COM134	8047	378	286	SEG308	5222	1767
47	DUMMY4	-4105	-1728	127	C11+	4853	-1728	207	COM135	8047	428	287	SEG307	5177	1767
48	DUMMY5	-4005	-1728	128	C11+	4953	-1728	208	COM136	8047	478	288	SEG306	5132	1767
49	DUMMY6	-3905	-1728	129	C11-	5053	-1728	209	SEG384	8047	568	289	SEG305	5087	1767
50	DUMMY7	-3805	-1728	130	C11-	5153	-1728	210	SEG383	8047	618	290	SEG304	5042	1767
51	DUMMY8	-3705	-1728	131	C11-	5254	-1728	211	SEG382	8047	668	291	SEG303	4997	1767
52	DUMMY9	-3605	-1728	132	VC1OUT	5442	-1728	212	SEG381	8047	718	292	SEG302	4952	1767
53	DB15	-3446	-1728	133	VC1OUT	5542	-1728	213	SEG380	8047	768	293	SEG301	4907	1767
54	DB14	-3308	-1728	134	VC1I	5731	-1728	214	SEG379	8047	818	294	SEG300	4862	1767
55	DB13	-3171	-1728	135	VC1I	5831	-1728	215	SEG378	8047	868	295	SEG299	4817	1767
56	DB12	-3033	-1728	136	VC1I	5931	-1728	216	SEG377	8047	918	296	SEG298	4772	1767
57	DB11	-2896	-1728	137	VCCDUM3	6061	-1728	217	SEG376	8047	968	297	SEG297	4727	1767
58	DB10	-2758	-1728	138	VCCDUM4	6161	-1728	218	SEG375	8047	1018	298	SEG296	4682	1767
59	DB9	-2621	-1728	139	RESET*	6291	-1728	219	SEG374	8047	1068	299	SEG295	4637	1767
60	DB8	-2483	-1728	140	COM17	6528	-1728	220	SEG373	8047	1118	300	SEG294	4592	1767
61	GNDDUM1	-2383	-1728	141	COM18	6573	-1728	221	SEG372	8047	1168	301	SEG293	4547	1767
62	DB7	-2283	-1728	142	COM19	6618	-1728	222	SEG371	8047	1218	302	SEG292	4502	1767
63	DB6	-2183	-1728	143	COM20	6663	-1728	223	SEG370	8047	1268	303	SEG291	4457	1767
64	DB5	-2071	-1728	144	COM21	6708	-1728	224	SEG369	8047	1318	304	SEG290	4412	1767
65	DB4	-1933	-1728	145	COM22	6753	-1728	225	SEG368	8047	1368	305	SEG289	4367	1767
66	DB3	-1796	-1728	146	COM23	6798	-1728	226	SEG367	8047	1418	306	SEG288	4322	1767
67	DB2	-1658	-1728	147	COM24	6843	-1728	227	SEG366	8047	1468	307	SEG287	4277	1767
68	DB1/SDO	-1521	-1728	148	COM25	6888	-1728	228	SEG365	8047	1518	308	SEG286	4232	1767
69	DB0/SDI	-1383	-1728	149	COM26	6933	-1728	229	SEG364	8047	1568	309	SEG285	4187	1767
70	GNDDUM2	-1283	-1728	150	COM27	6986	-1728	230	SEG363	8047	1618	310	SEG284	4142	1767
71	RW/RD*	-1183	-1728	151	COM28	7046	-1728	231	DUMMY18	8047	1767	311	SEG283	4097	1767
72	E/WR*/SCL	-1083	-1728	152	COM29	7106	-1728	232	SEG362	7887	1767	312	SEG282	4052	1767
73	GNDDUM3	-983	-1728	153	COM30	7166	-1728	233	SEG361	7826	1767	313	SEG281	4007	1767
74	RS	-883	-1728	154	COM31	7226	-1728	234	SEG360	7766	1767	314	SEG280	3962	1767
75	CS*	-783	-1728	155	COM32	7286	-1728	235	SEG359	7706	1767	315	SEG279	3917	1767
76	VCC	-642	-1728	156	COM33	7346	-1728	236	SEG358	7646	1767	316	SEG278	3872	1767
77	VCC	-542	-1728	157	COM34	7406	-1728	237	SEG357	7586	1767	317	SEG277	3827	1767
78	VCC	-442	-1728	158	COM35	7466	-1728	238	SEG356	7526	1767	318	SEG276	3782	1767
79	VCC	-342	-1728	159	COM36	7526	-1728	239	SEG355	7466	1767	319	SEG275	3737	1767
80	VCC	-242	-1728	160	COM37	7586	-1728	240	SEG354	7406	1767	320	SEG274	3692	1767

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ver0.0 2000.02.15作成

No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y
921	SEG273	3647	1767	401	SEG193	45	1767	481	SEG113	-3602	1767	561	SEG33	-7286	1767
922	SEG272	3602	1767	402	SEG192	-45	1767	482	SEG112	-3647	1767	562	SEG32	-7346	1767
923	SEG271	3557	1767	403	SEG191	-90	1767	483	SEG111	-3692	1767	563	SEG31	-7406	1767
924	SEG270	3511	1767	404	SEG190	-135	1767	484	SEG110	-3737	1767	564	SEG30	-7466	1767
925	SEG269	3466	1767	405	SEG189	-180	1767	485	SEG109	-3782	1767	565	SEG29	-7526	1767
926	SEG268	3421	1767	406	SEG188	-225	1767	486	SEG108	-3827	1767	566	SEG28	-7586	1767
927	SEG267	3376	1767	407	SEG187	-270	1767	487	SEG107	-3872	1767	567	SEG27	-7646	1767
928	SEG266	3331	1767	408	SEG186	-315	1767	488	SEG106	-3917	1767	568	SEG26	-7706	1767
929	SEG265	3286	1767	409	SEG185	-360	1767	489	SEG105	-3962	1767	569	SEG25	-7766	1767
930	SEG264	3241	1767	410	SEG184	-405	1767	490	SEG104	-4007	1767	570	SEG24	-7826	1767
931	SEG263	3196	1767	411	SEG183	-450	1767	491	SEG103	-4052	1767	571	SEG23	-7887	1767
932	SEG262	3151	1767	412	SEG182	-495	1767	492	SEG102	-4097	1767	572	DUMMY19	-8047	1767
933	SEG261	3106	1767	413	SEG181	-540	1767	493	SEG101	-4142	1767	573	SEG22	-8047	1618
934	SEG260	3061	1767	414	SEG180	-585	1767	494	SEG100	-4187	1767	574	SEG21	-8047	1568
935	SEG259	3016	1767	415	SEG179	-630	1767	495	SEG99	-4232	1767	575	SEG20	-8047	1518
936	SEG258	2971	1767	416	SEG178	-675	1767	496	SEG98	-4277	1767	576	SEG19	-8047	1468
937	SEG257	2926	1767	417	SEG177	-720	1767	497	SEG97	-4322	1767	577	SEG18	-8047	1418
938	SEG256	2881	1767	418	SEG176	-765	1767	498	SEG96	-4367	1767	578	SEG17	-8047	1368
939	SEG255	2836	1767	419	SEG175	-810	1767	499	SEG95	-4412	1767	579	SEG16	-8047	1318
940	SEG254	2791	1767	420	SEG174	-855	1767	500	SEG94	-4457	1767	580	SEG15	-8047	1268
941	SEG253	2746	1767	421	SEG173	-900	1767	501	SEG93	-4502	1767	581	SEG14	-8047	1218
942	SEG252	2701	1767	422	SEG172	-945	1767	502	SEG92	-4547	1767	582	SEG13	-8047	1168
943	SEG251	2656	1767	423	SEG171	-990	1767	503	SEG91	-4592	1767	583	SEG12	-8047	1118
944	SEG250	2611	1767	424	SEG170	-1035	1767	504	SEG90	-4637	1767	584	SEG11	-8047	1068
945	SEG249	2566	1767	425	SEG169	-1080	1767	505	SEG89	-4682	1767	585	SEG10	-8047	1018
946	SEG248	2521	1767	426	SEG168	-1125	1767	506	SEG88	-4727	1767	586	SEG9	-8047	968
947	SEG247	2476	1767	427	SEG167	-1170	1767	507	SEG87	-4772	1767	587	SEG8	-8047	918
948	SEG246	2431	1767	428	SEG166	-1216	1767	508	SEG86	-4817	1767	588	SEG7	-8047	868
949	SEG245	2386	1767	429	SEG165	-1261	1767	509	SEG85	-4862	1767	589	SEG6	-8047	818
950	SEG244	2341	1767	430	SEG164	-1306	1767	510	SEG84	-4907	1767	590	SEG5	-8047	768
951	SEG243	2296	1767	431	SEG163	-1351	1767	511	SEG83	-4952	1767	591	SEG4	-8047	718
952	SEG242	2251	1767	432	SEG162	-1396	1767	512	SEG82	-4997	1767	592	SEG3	-8047	668
953	SEG241	2206	1767	433	SEG161	-1441	1767	513	SEG81	-5042	1767	593	SEG2	-8047	618
954	SEG240	2161	1767	434	SEG160	-1486	1767	514	SEG80	-5087	1767	594	SEG1	-8047	568
955	SEG239	2116	1767	435	SEG159	-1531	1767	515	SEG79	-5132	1767	595	COM120	-8047	478
956	SEG238	2071	1767	436	SEG158	-1576	1767	516	SEG78	-5177	1767	596	COM119	-8047	428
957	SEG237	2026	1767	437	SEG157	-1621	1767	517	SEG77	-5222	1767	597	COM118	-8047	378
958	SEG236	1981	1767	438	SEG156	-1666	1767	518	SEG76	-5267	1767	598	COM117	-8047	328
959	SEG235	1936	1767	439	SEG155	-1711	1767	519	SEG75	-5312	1767	599	COM116	-8047	278
960	SEG234	1891	1767	440	SEG154	-1756	1767	520	SEG74	-5357	1767	600	COM115	-8047	228
961	SEG233	1846	1767	441	SEG153	-1801	1767	521	SEG73	-5402	1767	601	COM114	-8047	178
962	SEG232	1801	1767	442	SEG152	-1846	1767	522	SEG72	-5447	1767	602	COM113	-8047	128
963	SEG231	1756	1767	443	SEG151	-1891	1767	523	SEG71	-5492	1767	603	COM112	-8047	78
964	SEG230	1711	1767	444	SEG150	-1936	1767	524	SEG70	-5537	1767	604	COM111	-8047	28
965	SEG229	1666	1767	445	SEG149	-1981	1767	525	SEG69	-5582	1767	605	COM110	-8047	-22
966	SEG228	1621	1767	446	SEG148	-2026	1767	526	SEG68	-5627	1767	606	COM109	-8047	-72
967	SEG227	1576	1767	447	SEG147	-2071	1767	527	SEG67	-5672	1767	607	COM108	-8047	-122
968	SEG226	1531	1767	448	SEG146	-2116	1767	528	SEG66	-5717	1767	608	COM107	-8047	-172
969	SEG225	1486	1767	449	SEG145	-2161	1767	529	SEG65	-5762	1767	609	COM106	-8047	-222
970	SEG224	1441	1767	450	SEG144	-2206	1767	530	SEG64	-5807	1767	610	COM105	-8047	-272
971	SEG223	1396	1767	451	SEG143	-2251	1767	531	SEG63	-5852	1767	611	COM104	-8047	-322
972	SEG222	1351	1767	452	SEG142	-2296	1767	532	SEG62	-5897	1767	612	COM103	-8047	-372
973	SEG221	1306	1767	453	SEG141	-2341	1767	533	SEG61	-5942	1767	613	COM102	-8047	-422
974	SEG220	1261	1767	454	SEG140	-2386	1767	534	SEG60	-5987	1767	614	COM101	-8047	-472
975	SEG219	1216	1767	455	SEG139	-2431	1767	535	SEG59	-6032	1767	615	COM100	-8047	-522
976	SEG218	1171	1767	456	SEG138	-2476	1767	536	SEG58	-6077	1767	616	COM99	-8047	-572
977	SEG217	1126	1767	457	SEG137	-2521	1767	537	SEG57	-6122	1767	617	COM98	-8047	-622
978	SEG216	1081	1767	458	SEG136	-2566	1767	538	SEG56	-6167	1767	618	COM97	-8047	-672
979	SEG215	1036	1767	459	SEG135	-2611	1767	539	SEG55	-6212	1767	619	COM96	-8047	-722
980	SEG214	991	1767	460	SEG134	-2656	1767	540	SEG54	-6257	1767	620	COM95	-8047	-772
981	SEG213	946	1767	461	SEG133	-2701	1767	541	SEG53	-6302	1767	621	COM94	-8047	-822
982	SEG212	901	1767	462	SEG132	-2746	1767	542	SEG52	-6347	1767	622	COM93	-8047	-872
983	SEG211	856	1767	463	SEG131	-2791	1767	543	SEG51	-6392	1767	623	COM92	-8047	-922
984	SEG210	811	1767	464	SEG130	-2836	1767	544	SEG50	-6437	1767	624	COM91	-8047	-972
985	SEG209	766	1767	465	SEG129	-2881	1767	545	SEG49	-6482	1767	625	COM90	-8047	-1022
986	SEG208	721	1767	466	SEG128	-2926	1767	546	SEG48	-6527	1767	626	COM89	-8047	-1072
987	SEG207	676	1767	467	SEG127	-2971	1767	547	SEG47	-6572	1767	627	COM88	-8047	-1122
988	SEG206	631	1767	468	SEG126	-3016	1767	548	SEG46	-6617	1767	628	COM87	-8047	-1172
989	SEG205	586	1767	469	SEG125	-3061	1767	549	SEG45	-6662	1767	629	COM86	-8047	-1222
990	SEG204	541	1767	470	SEG124	-3106	1767	550	SEG44	-6707	1767	630	COM85	-8047	-1272
991	SEG203	496	1767	471	SEG123	-3151	1767	551	SEG43	-6752	1767	631	COM84	-8047	-1322
992	SEG202	451	1767	472	SEG122	-3196	1767	552	SEG42	-6797	1767	632	COM83	-8047	-1372
993	SEG201	406	1767	473	SEG121	-3241	1767	553	SEG41	-6842	1767	633	COM82	-8047	-1422
994	SEG200	361	1767	474	SEG120	-3286	1767	554	SEG40	-6887	1767	634	COM81	-8047	-1472
995	SEG199	316	1767	475	SEG119	-3331	1767	555	SEG39	-6932	1767	635	COM80	-8047	-1522
996	SEG198	271	1767	476	SEG118	-3376	1767	556	SEG38	-6977	1767	636	COM79	-8047	-1572
997	SEG197	226	1767	477	SEG117	-3421	1767	557	SEG37	-7022	1767				
998	SEG196	181	1767	478	SEG116	-3466	1767	558	SEG36	-7106	1767				
999	SEG195	136	1767	479	SEG115	-3511	1767	559	SEG35	-7166	1767				
1000	SEG194	91	1767	480	SEG114	-3556	1767	560	SEG34	-7226	1767				

Pin Functions

Table 1 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions																								
IM2-1, IM0/ID	3	I	GND or V <sub>CC</sub>	<p>Selects the MPU interface mode:</p> <table border="1"> <thead> <tr> <th>IM2</th> <th>IM1</th> <th>IM0/ID</th> <th>MPU interface mode</th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>GND</td> <td>GND</td> <td>68-system 16-bit bus interface</td> </tr> <tr> <td>GND</td> <td>GND</td> <td>V<sub>CC</sub></td> <td>68-system 8-bit bus interface</td> </tr> <tr> <td>GND</td> <td>V<sub>CC</sub></td> <td>GND</td> <td>80-system 16-bit bus interface</td> </tr> <tr> <td>GND</td> <td>V<sub>CC</sub></td> <td>V<sub>CC</sub></td> <td>80-system 8-bit bus interface</td> </tr> <tr> <td>V<sub>CC</sub></td> <td>GND</td> <td>ID</td> <td>Clock synchronized serial interface</td> </tr> </tbody> </table> <p>When a serial interface is selected, the IM0 pin is used as the ID setting for a device code.</p>	IM2	IM1	IM0/ID	MPU interface mode	GND	GND	GND	68-system 16-bit bus interface	GND	GND	V <sub>CC</sub>	68-system 8-bit bus interface	GND	V <sub>CC</sub>	GND	80-system 16-bit bus interface	GND	V <sub>CC</sub>	V <sub>CC</sub>	80-system 8-bit bus interface	V <sub>CC</sub>	GND	ID	Clock synchronized serial interface
IM2	IM1	IM0/ID	MPU interface mode																									
GND	GND	GND	68-system 16-bit bus interface																									
GND	GND	V <sub>CC</sub>	68-system 8-bit bus interface																									
GND	V <sub>CC</sub>	GND	80-system 16-bit bus interface																									
GND	V <sub>CC</sub>	V <sub>CC</sub>	80-system 8-bit bus interface																									
V <sub>CC</sub>	GND	ID	Clock synchronized serial interface																									
CS*	1	I	MPU	<p>Selects the HD66762:</p> <p>Low: HD66762 is selected and can be accessed</p> <p>High: HD66762 is not selected and cannot be accessed</p> <p>Must be fixed at GND level when not in use.</p>																								
RS	1	I	MPU	<p>Selects the register.</p> <p>Low: Index/status                      High: Control</p> <p>Must be fixed at GND level when not in use.</p>																								
E/WR*/SCL	1	I	MPU	<p>For a 68-system bus interface, serves as an enable signal to activate data read/write operation.</p> <p>For an 80-system bus interface, serves as a write strobe signal and writes data at the low level.</p> <p>For a synchronous clock interface, serves as the synchronous clock signal.</p>																								
RW/RD*	1	I	MPU	<p>For a 68-system bus interface, serves as a signal to select data read/write operation.</p> <p>Low: Write                      High: Read</p> <p>For an 80-system bus interface, serves as a read strobe signal and reads data at the low level.</p>																								
DB0/SDI	1	I/O	MPU	<p>Serves as a 16-bit bidirectional data bus.</p> <p>For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the V<sub>CC</sub> or GND level.</p> <p>For a clock-synchronous serial interface, serves as the serial data input pin (SDI). The input level is read on the rising edge of the SCL signal.</p>																								
DB1/SDO	1	I/O	MPU	<p>Serves as a 16-bit bidirectional data bus.</p> <p>For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the V<sub>CC</sub> or GND level.</p> <p>For a clock-synchronous serial interface, serves as a serial data output pin (SDO). Successive bit values are output on the falling edge of the SCL signal.</p>																								

## HD66762

**Table 1 Pin Functional Description (cont.)**

Signals	Number of Pins	I/O	Connected to	Functions
DB2-DB15	14	I/O	MPU	Serves as a 16-bit bidirectional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level.
SEG1–SEG384	384	O	LCD	Output signals for segment drive. In the display-off period (D1–0 = 00, 01) or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, RAM address 0000 is output from SEG1. If SGS = 1, it is output from SEG384. SEG1, SEG4, SEG7, ... display red (R), SEG2, SEG5, SEG8, ... display green (G), and SEG3, SEG6, SEG9, ... display blue (B) (SGS = 0).
COM1–COM136	136	O	LCD	Output signals for common drive. In the display-off period (D1–0 = 00, 01) or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, driver outputs from COM1 to COM136. If CMS = 1, driver outputs COM136 to COM1. Note that start position of the common driver output is changed by screen driving position function.
VCH, VCL	2	—	Capacitor for stabilization or external power supply	Selection level for the common signal. When internal power supply is used, connect the capacitors for stabilization. When internal power supply is not used, supply external voltage.
VM	1	—	Capacitor for stabilization or external power supply	Non-selection level for the common signal. When internal operational amplifier is used, it is output of the internal operational amplifier and connect the capacitors for stabilization. When internal operational amplifier is not used, supply external voltage.
VSH	1	—	Capacitor for stabilization or external power supply	Selection level for the segment signal. When internal operational amplifier is used, it is output of the internal operational amplifier and connect the capacitors for stabilization. When internal operational amplifier is not used, supply external voltage.
VciOUT	1	—	Vci1 and capacitor for stabilization	Outputs a regulated voltage derived from Vcc. Connect a capacitor for stabilization. When this pin is not used, leave it open.
Vci1	1	—	VciOUT or power supply	Voltage-input pin for step-up circuit 1. When the Vci adjuster is used, input the power supply from VciOUT. When not used, input the external power supply.

Table 1 Pin Functional Description (cont.)

Signals	Number of Pins	I/O	Connected to	Functions
Vci2	1	—	Capacitor for stabilization or open	Connect capacitor for stabilization. When the internal step-up circuit is not used, leave this pin open.
VOU	1	—	Capacitor for step-up circuit	A voltage that doubles or between Vci1 and GND is output here. The step-up factor can be set in an internal register.
C11+, C11-	2	—	Step-up capacitance	When step-up circuit is used, connect a step-up capacitor.
C12+, C12-	2	—	Step-up capacitance	When step-up circuit is used, connect a step-up capacitor.
C21+, C21-	2	—	Step-up capacitance	When step-up circuit is used, connect a step-up capacitor.
C22+, C22-	2	—	Step-up capacitance	When step-up circuit is used, connect a step-up capacitor.
C23+, C23-	2	—	Step-up capacitance	When step-up circuit is used, connect a step-up capacitor.
CEP, CEM	2	—	Step-up capacitance or open	Connect a step-up capacitor to generate VCL level by VCH and VM. When step-up circuit is not used, leave this pin open.
V <sub>s</sub> REFL	1	—	VOU or external power supply	Inputs reference voltage. Input Vcc or external reference power supply.
VREFM	1	—	Capacitor for stabilization or external power supply	LCD driving voltage which is boosted by VREFL level. Connect capacitor for stabilization. When internal amplifier is not used, input external power supply.
BIASC	1	—	Capacitor for stabilization or open	Connect capacitor for stabilization for internal power supply. When the internal power supply is not used, leave this pin open.
V <sub>CC</sub> , GND	2	—	Power supply	V <sub>CC</sub> : + 1.8 V to + 3.6 V; GND (logic): 0
OSC1, OSC2	2	I/O	Oscillation-resistor	Connect an external resistor for R-C oscillation. When providing clocks from outside, input clock to OSC1 and leave OSC2 open.
RESET*	3	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low. Must be reset after power-on. Connect signal to one of three RESET* pins, and leave the other pins open.
VccDUM		O	Input pins	Outputs the internal V <sub>CC</sub> level; shorting this pin sets the adjacent input pin to the V <sub>CC</sub> level.
GNDDUM		O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy		—	—	Dummy pad. Must be left disconnected.
TEST1, TEST2	2	I	GND	Test pin. Must be fixed at GND level.

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## HD66762

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### Block Function Description

#### System Interface

The HD66762 has five high-speed system interfaces: an 80-series 16-bit/8-bit bus, a 68-series 16-bit/8-bit bus, and a Clock synchronized serial interface. The interface mode is selected by the IM2-0 pins.

The HD66762 has three 16-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information from the control registers and the GRAM. The WDR temporarily stores data to be written into control registers and the GRAM, and the RDR temporarily stores data read from the GRAM. Data written into the GRAM from the MPU is first written into the WDR and then is automatically written into the GRAM by internal operation. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are normal. When a logic operation is performed inside of the HD66762 by using the display data set in the GRAM and the data written from the MPU, the data read through the RDR is used. Accordingly, the MPU does not need to read data twice nor to fetch the read data into the MPU. This enables high-speed processing.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

**Table 2 Register Selection**

80-series Bus		68-series Bus		Operations
WR	RD	R/W	RS	
0	1	0	0	Writes indexes into IR
1	0	1	0	Reads internal status
0	1	0	1	Writes into control registers and GRAM through WDR
1	0	1	1	Reads from GRAM through RDR

**Table 3 Register Selection (Clock synchronized Serial Interface)**

Start bytes		
R/W Bit	RS Bit	Operations
0	0	Writes indexes into IR
1	0	Reads internal status
0	1	Writes into control registers and GRAM through WDR
1	1	Reads from GRAM through RDR

**Bit Operation**

The HD66762 supports the following functions: a swap function that writes the data written from the MPU into the GRAM by reversing the display position vertically in byte units, a write data mask function that selects and writes data into the GRAM in bit units, and a logic operation function that performs logic operations or conditional determination on the display data set in the GRAM and writes into the GRAM. With the 16-bit bus interface, these functions can greatly reduce the processing loads of the MPU graphics software and can rewrite the display data in the GRAM at high speed. For details, see the Graphics Operation Function section.

**Address Counter (AC)**

The address counter (AC) assigns addresses to the GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the AC is not updated.

**Graphics RAM (GRAM)**

The graphics RAM (GRAM) has eight bits/pixel and stores the bit-pattern data of 128 x 136 bytes.

**PWM Grayscale Palette Circuit**

The grayscale palette generates a PWM signal which corresponds specified grayscale level. Any 256 out of the 4,096 possible colors can be displayed at the same time.

**Grayscale Control Circuit**

The grayscale control circuit performs 16-grayscale control with the pulse width modulation (PWM) method for grayscale display for each color.

**Timing Generator**

The timing generator generates timing signals for the operation of internal circuits such as the GRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another.

**Oscillation Circuit (OSC)**

The HD66762 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced.

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## **HD66762**

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### **Liquid Crystal Display Driver Circuit**

The liquid crystal display driver circuit consists of 136 common signal drivers (COM1 to COM136) and 384 segment signal drivers (SEG1 to SEG384).

Display pattern data from GRAM is latched to the 384-bit latch circuit. The latched data then enables the segment signal drivers to generate drive waveform outputs. The common driver outputs one of the VCH, VM or VCL voltage level. The shift direction of 384-bit data for segment can be changed by the SGS bit. The shift direction for the common driver can also be changed by the CMS bit by selecting an appropriate direction for the device mounting configuration.

When display is off, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

### **LCD drive power supply circuit**

LCD drive power supply circuit generates VCH, VSH, VM and VCL voltage level to drive LCD panel.

**Table 4 Relationship between GRAM address and display position (SGS=0, SWP=0)**

SEG/COM pins		SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	.....	SEG373	SEG374	SEG375	SEG376	SEG377	SEG378	SEG379	SEG380	SEG381	SEG382	SEG383	SEG384
CMS=0	CMS=1	DB 0	DB 7	DB 8	DB 15	DB 0	DB 7	DB 8	DB 15	DB 0	DB 7	DB 8	DB 15		DB 0	DB 7	DB 8	DB 15	DB 0	DB 7	DB 8	DB 15	DB 0	DB 7	DB 8	DB 15
COM1	COM136	"0000"H				"0001"H				.....	"003E"H				"003F"H											
COM2	COM135	"0100"H				"0101"H				.....	"013E"H				"013F"H											
COM3	COM134	"0200"H				"0201"H				.....	"023E"H				"023F"H											
COM4	COM133	"0300"H				"0301"H				.....	"033E"H				"033F"H											
COM5	COM132	"0400"H				"0401"H				.....	"043E"H				"043F"H											
COM6	COM131	"0500"H				"0501"H				.....	"053E"H				"053F"H											
COM7	COM130	"0600"H				"0601"H				.....	"063E"H				"063F"H											
COM8	COM129	"0700"H				"0701"H				.....	"073E"H				"073F"H											
COM9	COM128	"0800"H				"0801"H				.....	"083E"H				"083F"H											
COM10	COM127	"0900"H				"0901"H				.....	"093E"H				"093F"H											
COM11	COM126	"0A00"H				"0A01"H				.....	"0A3E"H				"0A3F"H											
COM12	COM125	"0B00"H				"0B01"H				.....	"0B3E"H				"0B3F"H											
COM13	COM124	"0C00"H				"0C01"H				.....	"0C3E"H				"0C3F"H											
COM14	COM123	"0D00"H				"0D01"H				.....	"0D3E"H				"0D3F"H											
COM15	COM122	"0E00"H				"0E01"H				.....	"0E3E"H				"0E3F"H											
COM16	COM121	"0F00"H				"0F01"H				.....	"0F3E"H				"0F3F"H											
COM17	COM120	"1000"H				"1001"H				.....	"103E"H				"103F"H											
COM18	COM119	"1100"H				"1101"H				.....	"113E"H				"113F"H											
COM19	COM118	"1200"H				"1201"H				.....	"123E"H				"123F"H											
COM20	COM117	"1300"H				"1301"H				.....	"133E"H				"133F"H											
⋮	⋮	⋮				⋮					⋮				⋮											
COM129	COM8	"8000"H				"8001"H				.....	"803E"H				"803F"H											
COM130	COM7	"8100"H				"8101"H				.....	"813E"H				"813F"H											
COM131	COM6	"8200"H				"8201"H				.....	"823E"H				"823F"H											
COM132	COM5	"8300"H				"8301"H				.....	"833E"H				"833F"H											
COM133	COM4	"8400"H				"8401"H				.....	"843E"H				"843F"H											
COM134	COM3	"8500"H				"8501"H				.....	"853E"H				"853F"H											
COM135	COM2	"8600"H				"8601"H				.....	"863E"H				"863F"H											
COM136	COM1	"8700"H				"8701"H				.....	"873E"H				"873F"H											

**Table 5 Relationship between GRAM data and output pin (SGS=0)**

GRAM data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selected palette	RK palette			GK palette			BK palette		RK palette			GK palette			BK palette	
Output pin	SEG (6n+1)			SEG (6n+2)			SEG (6n+3)		SEG (6n+4)			SEG (6n+5)			SEG (6n+6)	

n = Lower 6-bits address (0 to 63)

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SEG/COM pins		SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	.....	SEG373	SEG374	SEG375	SEG376	SEG377	SEG378	SEG379	SEG380	SEG381	SEG382	SEG383	SEG384
CMS=0	CMS=1	DB 0	DB 7	DB 8	DB 15	DB 0	DB 7	DB 8	DB 15	DB 0	DB 7	DB 8	DB 15	.....	DB 0	DB 7	DB 8	DB 15	DB 0	DB 7	DB 8	DB 15	DB 0	DB 7	DB 8	DB 15
COM1	COM136	"003F"H				"003E"H				.....	"0001"H				"0000"H											
COM2	COM135	"013F"H				"013E"H				.....	"0101"H				"0100"H											
COM3	COM134	"023F"H				"023E"H				.....	"0201"H				"0200"H											
COM4	COM133	"033F"H				"033E"H				.....	"0301"H				"0300"H											
COM5	COM132	"043F"H				"043E"H				.....	"0401"H				"0400"H											
COM6	COM131	"053F"H				"053E"H				.....	"0501"H				"0500"H											
COM7	COM130	"063F"H				"063E"H				.....	"0601"H				"0600"H											
COM8	COM129	"073F"H				"073E"H				.....	"0701"H				"0700"H											
COM9	COM128	"083F"H				"083E"H				.....	"0801"H				"0800"H											
COM10	COM127	"093F"H				"093E"H				.....	"0901"H				"0900"H											
COM11	COM126	"0A3F"H				"0A3E"H				.....	"0A01"H				"0A00"H											
COM12	COM125	"0B3F"H				"0B3E"H				.....	"0B01"H				"0B00"H											
COM13	COM124	"0C3F"H				"0C3E"H				.....	"0C01"H				"0C00"H											
COM14	COM123	"0D3F"H				"0D3E"H				.....	"0D01"H				"0D00"H											
COM15	COM122	"0E3F"H				"0E3E"H				.....	"0E01"H				"0E00"H											
COM16	COM121	"0F3F"H				"0F3E"H				.....	"0F01"H				"0F00"H											
COM17	COM120	"103F"H				"103E"H				.....	"1001"H				"1000"H											
COM18	COM119	"113F"H				"113E"H				.....	"1101"H				"1100"H											
COM19	COM118	"123F"H				"123E"H				.....	"1201"H				"1200"H											
COM20	COM117	"133F"H				"133E"H				.....	"1301"H				"1300"H											
⋮	⋮	⋮				⋮				.....	⋮				⋮											
COM129	COM8	"803F"H				"803E"H				.....	"8001"H				"8000"H											
COM130	COM7	"813F"H				"813E"H				.....	"8101"H				"8100"H											
COM131	COM6	"823F"H				"823E"H				.....	"8201"H				"8200"H											
COM132	COM5	"833F"H				"833E"H				.....	"8301"H				"8300"H											
COM133	COM4	"843F"H				"843E"H				.....	"8401"H				"8400"H											
COM134	COM3	"853F"H				"853E"H				.....	"8501"H				"8500"H											
COM135	COM2	"863F"H				"863E"H				.....	"8601"H				"8600"H											
COM136	COM1	"873F"H				"873E"H				.....	"8701"H				"8700"H											

**Table 6 Relationship between CGRAM address and display position (SGS=1, SWP=0)**

**Table 7 Relationship between CGRAM data and output pin (SGS=1)**

GRAM data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selected palette	RK palette			GK palette			BK palette		RK palette			GK palette			BK palette	
Output pin	SEG (384-6n)			SEG (383-6n)			SEG (382-6n)		SEG (381-6n)			SEG (380-6n)			SEG (379-6n)	

n = Lower 6-bits address (0 to 63)

## **Instructions**

### **Outline**

The HD66762 uses the 16-bit bus architecture. Before the internal operation of the HD66762 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the HD66762 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB15 to DB0), make up the HD66762 instructions. There are eight categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale palette table

Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load.

Because instructions are executed in 0 cycles, they can be written in succession.

## Instruction Descriptions

### Index (IR)

The index instruction specifies the RAM control indexes (R00h to R39h). It sets the register number in the range of 00000 to 111001 in binary form. However, R40h to R44h are disabled since they are test registers.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 1 Index Instruction

### Status Read (SR)

The status read instruction reads the internal status of the HD66762.

**L7-0:** Indicate the driving raster-row position where the liquid crystal display is being driven.

**C6-0:** Read the contrast setting values (CT6-0).

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0

Figure 2 Status Read Instruction

### Start Oscillation (R00h)

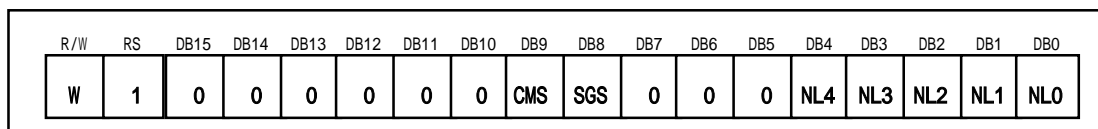
The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly, "0762"H is read.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0

Figure 3 Start Oscillation Instruction

**Driver Output Control (R01h)**



**Figure 4 Driver Output Control Instruction**

**CMS:** Selects the output shift direction of a common driver. When CMS = 0, COM1 shifts to COM136. When CMS = 1, COM136 shifts to COM1.

**SGS:** Selects the output shift direction of a segment driver by using with the SWP bit. When SGS = 0 and SWP = 0, the data at address “0000”H outputs to SEG1. When SGS = 1 and SWP=1, the data at address “0000”H outputs to SEG384. When SGS = 0 and SWP = 0, the SEG1 pin assigns the color display to R (SEG2=G, SEG3=B). When SGS = 1 and SWP = 1, the SEG384 pin assigns R (SEG383=G, SEG382=B). Re-write to the RAM when intending to change the SGS bit.

**NL4-0:** Specify the LCD drive duty ratio. The duty ratio can be adjusted for every eight raster-rows. GRAM address mapping does not depend on the setting value of the drive duty ratio.

**Table 8 NL Bits and Drive Duty**

NL	NL3	NL2	NL1	NL0	Display resolution	LCD drive duty	Common Driver Used	
							CMS="0"	CMS="1"
4	0	0	0	0	Setting disabled	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	384 x 16 dots	1/16 Duty	COM1–COM16	COM136–COM120
0	0	0	1	0	384 x 24 dots	1/24 Duty	COM1–COM24	COM136–COM112
0	0	0	1	1	384 x 32 dots	1/32 Duty	COM1–COM32	COM136–COM104
0	0	1	0	0	384 x 40 dots	1/40 Duty	COM1–COM40	COM136–COM96
0	0	1	0	1	384 x 48 dots	1/48 Duty	COM1–COM48	COM136–COM88
0	0	1	1	0	384 x 56 dots	1/56 Duty	COM1–COM56	COM136–COM80
0	0	1	1	1	384 x 64 dots	1/64 Duty	COM1–COM64	COM136–COM72
0	1	0	0	0	384 x 72 dots	1/72 Duty	COM1–COM72	COM136–COM64
0	1	0	0	1	384 x 80 dots	1/80 Duty	COM1–COM80	COM136–COM56
0	1	0	1	0	384 x 88 dots	1/88 Duty	COM1–COM88	COM136–COM48
0	1	0	1	1	384 x 96 dots	1/96 Duty	COM1–COM96	COM136–COM40
0	1	1	0	0	384 x 104 dots	1/104 Duty	COM1–COM104	COM136–COM32
0	1	1	0	1	384 x 112 dots	1/112 Duty	COM1–COM112	COM136–COM24
0	1	1	1	0	384 x 120 dots	1/120 Duty	COM1–COM120	COM136–COM16
0	1	1	1	1	384 x 128 dots	1/128 Duty	COM1–COM128	COM136–COM8
1	0	0	0	0	384 x 136 dots	1/136 Duty	COM1–COM136	COM136–COM1

**LCD-Driving-Waveform Control (R02h)**

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	RST	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

**Figure 5 LCD-Driving-Waveform Control Instruction**

**RST:** When RST = 1, software reset function is started. This function is same as hardware RESET\* pin. It takes 10 clock cycle period. This bit is automatically cleared after reset function is completed. Therefore, after 10 clock cycle other instruction can not be issued. Do not set the RST bit during stand-by mode.

**B/C:** When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a C-pattern waveform is generated and alternates in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

**EOR:** When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

**NW5–0:** Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW5–NW0 alternate for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected.

**Power Control 1 (R03h)**

**Power Control 2 (R0Ch)**

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	BS3	BS2	BS1	BS0	BT3	BT2	BT1	BT0	0	DC2	DC1	DC0	AP1	AP0	SLP	STB
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0

**Figure 6 Power Control Instruction**

**BS3–0:** The LCD drive bias value is set. The LCD drive bias value can be selected according to its drive duty ratio and voltage.

**BT2–0:** The output factor of step-up is switched. The LCD drive voltage level can be selected according to its drive duty ratio and bias. Lower amplification of the step-up circuit consumes less current.

**BT3:** The polarity inversion circuit is controlled. When BT3=0, the polarity inversion circuit stops working. When BT3=1, starts working. Refer “Power on-off sequence” section.

**DC2–0:** The operating frequency in the step-up circuit is selected. When the step-up

operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

**AP1-0:** The amount of fixed current from the fixed current source in the operational amplifier for the LCD is adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption.

During no display, when AP1-0 = 00, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

**VC2-0:** Sets an adjustment factor for the Vci voltage (VC2-0).

**SLP:** When SLP = 1, the HD66762 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. Only the following instructions can be executed during the sleep mode.

Power control (BS3-0, BT3-0, DC2-0, AP1-0, SLP, and STB bits)

During the sleep mode, the other GRAM data and instructions cannot be updated although they are retained.

**STB:** When STB = 1, the HD66762 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

- a. Standby mode cancel (STB = 0)
- b. Start oscillation

During the standby mode, the GRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

Table 9 Display bias setting table

LCD driving bias	Booster ratio of the step-up circuit 2 (ND2)	BS3	BS2	BS1	BS0	Bias ratio (NB)	Vci2 (Vci2=4.8V)	Recommended value of the VCH=20V
1/2	x 2	0	0	1	0	0.75	1.50 x VSH	Vci2 x 2
	x 3	0	0	0	0	0.50	1.0 x VSH	Vci2 x 3
	x 4	-	-	-	-	N/A	-	-
1/4	x 2	0	1	1	1	1.25	2.5 x VSH	Vci2 x 2
	x 3	0	0	1	1	0.835	1.65 x VSH	Vci2 x 3
	x 4	0	0	0	1	0.625	1.25 x VSH	Vci2 x 4
1/6	x 2	1	1	0	0	1.75	3.5 x VSH	Vci2 x 2
	x 3	0	1	1	0	1.165	2.33 x VSH	Vci2 x 3
	x 4	0	1	0	0	0.875	1.75 x VSH	Vci2 x 4
1/8	x 2	-	-	-	-	N/A	-	-
	x 3	1	0	0	1	1.50	3.0 x VSH	Vci2 x 3
	x 4	0	1	0	1	1.125	2.25 x VSH	Vci2 x 4
1/9	x 2	-	-	-	-	N/A	-	-
	x 3	1	0	1	1	1.665	3.35 x VSH	Vci2 x 3
	x 4	0	1	1	1	1.25	2.5 x VSH	Vci2 x 4
1/10	x 2	-	-	-	-	N/A	-	-
	x 3	1	1	0	1	1.835	3.65 x VSH	Vci2 x 3
	x 4	1	0	0	0	1.375	2.75 x VSH	Vci2 x 4
1/11	x 2	-	-	-	-	N/A	-	-
	x 3	1	1	1	0	2.00	4.0 x VSH	Vci2 x 3
	x 4	1	0	0	1	1.50	3.0 x VSH	Vci2 x 4
1/12	x 2	-	-	-	-	N/A	-	-
	x 3	1	1	1	1	2.165	4.33 x VSH	Vci2 x 3
	x 4	1	0	1	0	1.625	3.25 x VSH	Vci2 x 4

The VSH voltage level should be controlled to be less than supply voltage or device proof voltage level since VCH voltage level is generated by bias amplifier ratio correspond to LCD driving bias value and boosting ration of the step-up circuit 2.

**Table 10 Display bias setting table**

VC2	VC1	VC0	Vci1 control range
0	0	0	0.92 x Vcc
0	0	1	0.87 x Vcc
0	1	0	0.83 x Vcc
0	1	1	0.8 x Vcc
1	0	0	0.76 x Vcc
1	0	1	0.73 x Vcc
1	1	0	0.68 x Vcc
1	1	1	Vci control amplifier suspends. (Vci can be supplied externally)

**Table 11 Output voltage ratio of the booster 1 and 2**

BT2	BT1	BT0	VOUT output of the booster 1	VCH output of the booster 2
0	0	0	2 x Vci1	2 x Vci2
0	0	1	3 x Vci1	2 x Vci2
0	1	0	2 x Vci1	3 x Vci2
0	1	1	3 x Vci1	3 x Vci2
1	0	0	2 x Vci1	4 x Vci2
1	0	1	3 x Vci1	4 x Vci2
1	1	0	2 x Vci1	Booster stops

**Table 11 Control Polarity inversion circuit**

BT3	VCL output of the polarity inversion circuit
0	Booster stops
1	Polarity inverted voltage between VCH and VM

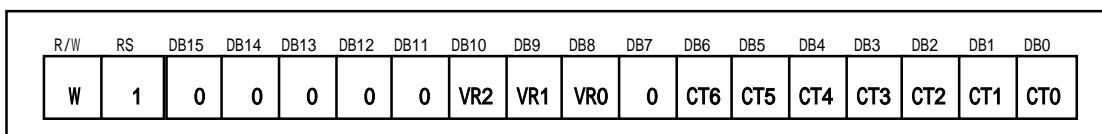
**Table 12 Operating clock frequency of the Booster 1 and 2**

DC2	DC1	DC0	Operating clock frequency in the booster 1	Operating clock frequency in the booster 2
0	0	0	15 divided clock	15 divided clock
0	0	1	30 divided clock	15 divided clock
0	1	0	15 divided clock	30 divided clock
0	1	1	30 divided clock	30 divided clock
1	0	0	15 divided clock	45 divided clock
1	0	1	30 divided clock	45 divided clock
1	1	0	15 divided clock	60 divided clock
1	1	1	30 divided clock	60 divided clock

**Table 13 AP bits and amount of fixed current**

AP1	AP0	Amount of fixed current in the operational amplifier
0	0	Operational amplifier and booster do not operate.
0	1	Small
1	0	Middle
1	1	Large

**Contrast Control (R04h)**



**Figure 7 Contrast Control Instruction**

**CT6-0:** These bits control the LCD drive voltage to adjust 128-step contrast.

**Table 14 Contrast control**

CT6	CT5	CT4	CT3	CT2	CT1	CT0	Contrast
0	0	0	0	0	0	0	1.016R (Minimum)
0	0	0	0	0	0	1	1.008R
0	0	0	0	0	1	0	1.000R
0	0	0	0	0	1	1	0.992R
0	0	0	0	1	0	0	0.984R
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	0.008R
1	1	1	1	1	1	1	0.000R (Maximum)

**VR2-0:** These bits control the step-up level of the VREFM, generated by VREFL. The VREFM should be smaller than VOUT level.

**Table 15 Contrast control**

VR2	VR1	VR0	VREFM voltage
0	0	0	VREFL x 1.1
0	0	1	VREFL x 1.3
0	1	0	VREFL x 1.4
0	1	1	VREFL x 1.5
1	0	0	VREFL x 1.7
1	0	1	VREFL x 1.8
1	1	0	VREFL x 3.4
1	1	1	Inhibited

**Entry Mode (R05h)**

**Compare Register (R06h)**

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	HWM	SWP	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
W	1	0	0	0	0	0	0	0	0	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

**Figure 8 Entry Mode and Compare Register Instruction**

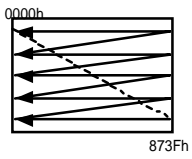
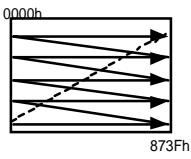
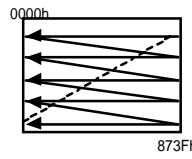
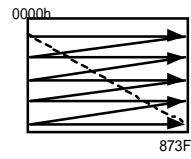
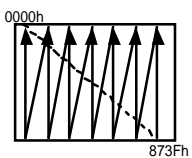
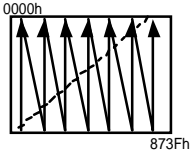
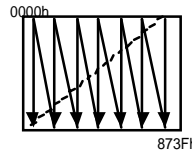
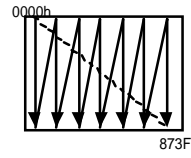
The write data sent from the microcomputer is modified in the HD66762 and written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

**HWM:** When HWM=1, data can be written to the GRAM at high speed. In high-speed write mode, four words of data are written to the GRAM in a single operation after writing to RAM four times. Write to RAM four times, otherwise the four words cannot be written to the GRAM. Thus, set the lower 2 bits to 0 when setting the RAM address. For details, see High-Speed RAM Write Mode section.

**SWP:** When SWP = 1, the upper and lower bytes in the two-byte data sent from the microcomputer are swapped and written to the GRAM. When SWP = 0, this bit directly writes the two-byte data sent from the microcomputer to the GRAM. This swap processing is performed only for the data sent from the microcomputer before logical operation. When SWP = 1, the upper and lower bytes in the write data mask (WM15-0) are swapped to be executed with the write data.

**I/D1-0:** When I/D1-0 = 1, the address counter (AC) is automatically incremented by 1 after the data is written to the GRAM. When I/D1-0 = 0, the AC is automatically decremented by 1 after the data is written to the GRAM. The increment/decrement setting of the address counter by I/D1-0 is done independently for the upper (AD15-8) and lower (AD5-0) addresses. The direction of moving through the addresses when the GRAM is written to is set by the AM bit.

**AM:** Set the automatic update method of the AC after the data is written to the GRAM. When AM = 0, the data is continuously written in parallel. When AM = 1, the data is continuously written vertically. When window address range is specified, the GRAM in the window address range can be written to according to the I/D1-0 and AM settings.

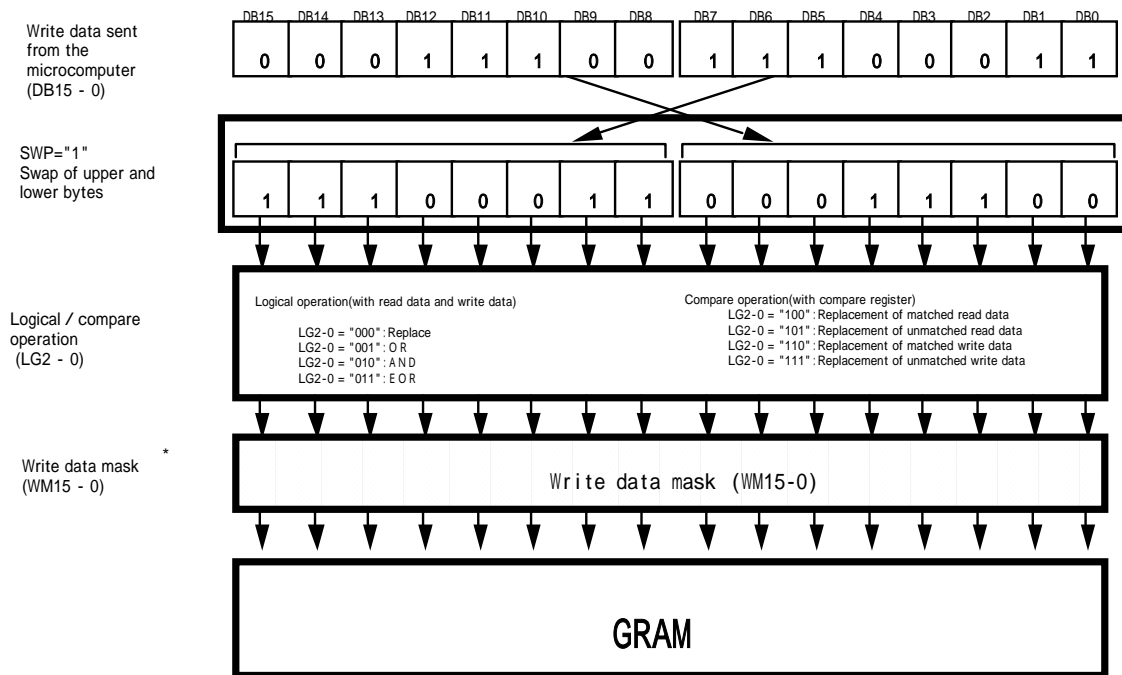
Direction settings	I/D1-0 = "00" X direction: Decrement Y direction: Decrement	I/D1-0="01" X direction: Increment Y direction: Decrement	I/D1-0="10" X direction: Decrement Y direction: Increment	I/D1-0="11" X direction: Increment Y direction: Increment
AM="0" Horizontal				
AM="1" Vertical				

Note : When a window address range has been set, the GRAM can only be written to within that range.

Figure 9 Address Direction Settings

**LG2-0:** Compare the data read from the GRAM by the microcomputer with the compare registers (CP7-0) by a compare/logical operation and write the results to GRAM. For details, see the Logical/Compare Operation Function.

**CP7-0:** Set the compare register for the compare operation with the data read from the GRAM or written by the microcomputer.



Note: 1. The write data mask(WM15-0) is set by the register in the RAM Write Data Mask section.  
 2. When SWP = "1", the upper and lower bytes in the write data mask are swapped to be executed with the write data

**Figure 10 Logical/Compare Operation and Swapping for the GRAM**

**Display Control (R07h)**

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	VLE 2	VLE 1	SPT	0	0	0	0	B/W	REV	D1	D0

**Figure 11 Display Control Instruction**

**VLE2-1:** When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = 1, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens can be independently controlled.

**SPT:** When SPT = 1, the 2-division LCD drive is performed. For details, see the Screen-division Driving Function section.

**B/W:** When B/W = 1, displayed data can be "all on" or "all off" regardless GRAM contents. (B/W =

1, REV = 0 : all pixel on, B/W = 1, REV = 1 : all pixel off) When B/W = 1, grayscale palette (from R30h to R39h) has to be default value.

**REV:** Displays all character and graphics display sections with reversal when REV = 1. For details, see the Reversed Display Function section. Since the grayscale level can be reversed, display of the same data is enabled on normally-white and normally-black panels.

**D1-0:** Display is on when D1 = 1 and off when D1 = 0. When off, the display data remains in the GRAM, and can be displayed instantly by setting D1 = 1. When D1 is 0, the display is off with all of the SEG/COM pin outputs set to the GND level. Because of this, the HD66762 can control the charging current for the LCD with AC driving.

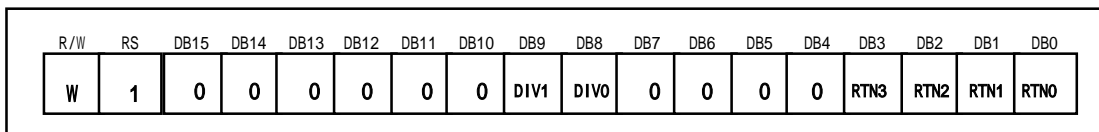
When D1-0 = 01, the internal display of the HD66762 is performed although the display is off. When D1-0 = 00, the internal display operation halts and the display is off.

**Table 16 D Bits and Operation**

D1	D0	SEG/COM Output	HD66762 Internal Display Operation
0	0	GND	Halt
0	1	GND	Operate
1	0	Unlit display	Operate
1	1	Display	Operate

- Notes: 1. Writing from the microcomputer to the GRAM is independent from D1-0.  
 2. In the sleep and standby modes, D1-0 = 00. However, the register contents of D1-0 are not modified.

**Frame Cycle Control (R0Bh)**



**Figure 12 Frame Cycle Control Instruction**

**DIV1-0:** Set the division ratio of clocks for internal operation (DIV1-0). Internal operations are driven by clocks which are frequency divided according to the DIV1-0 setting. Frame frequency can be adjusted along with the line retrace period (RTN3-0). When changing the drive-duty cycle, adjust the frame frequency. For details, see the Frame Frequency Adjustment Function section.

**RTN3-0:** Set the line retrace period (RTN3-0) to be added to raster-row cycles. The raster-row cycle becomes longer according to the number of clocks set at RTN3-0.

**Table 17 RTN Bits and Clock Cycles**

RTN3	RTN2	RTN1	RTN0	Line Retrace Period (Clock Cycles)	Clock Cycles per one raster-row
0	0	0	0	0 clock	17 clock
0	0	0	1	1 clock	18 clock
0	0	1	0	2 clock	19 clock
0	0	1	1	3 clock	20 clock
:	:	:	:	:	:
1	1	1	0	14 clock	31 clock
1	1	1	1	15 clock	32 clock

**Table 18 DIV Bits and Clock Frequency**

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

\* fosc = R-C oscillation frequency

**Formula for the frame frequency**

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times 1/\text{duty cycle}} \quad [\text{Hz}]$$

fosc: R-C oscillation frequency  
 Duty: drive duty (NL bit)  
 Division ratio: DIV bit  
 Clock cycles per raster-row: (RTN + 17) clock cycles

**Vertical Scroll Control (R11h)**

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	VL	VL	VL	VL	VL	VL	VL	VL	VL	VL	VL	VL	VL	VL	VL	VL
		27	26	25	24	23	22	21	20	17	16	15	14	13	12	11	10

**Figure 13 Vertical Scroll Control Instruction**

**VL17–10:** Specify the display-start raster-row at the 1st screen display for vertical smooth scrolling. Any raster-row from the first to 136th can be selected. After the 136th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL17–10) is valid only when VLE1 = 1. The raster-row display is fixed when VLE1 = 0. (VLE1 is the 1st-screen vertical-scroll enable bit.)

**VL27–20:** Specify the display-start raster-row at the 2nd screen display. The display-start raster-row (VL27–20) is valid only when VLE2 = 1. The raster-row display is fixed when VLE2 = 0. (VLE2 is the 2nd-screen vertical-scroll enable bit.) The vertical scroll for the 1st and 2nd screens can be independently set.

**Table 19 VL Bits and Display-start Raster-row**

VL27 VL17	VL26 VL16	VL25 VL15	VL24 VL14	VL23 VL13	VL22 VL12	VL21 VL11	VL20 VL10	Display-start Raster-row
0	0	0	0	0	0	0	0	1 <sup>st</sup> raster-row
0	0	0	0	0	0	0	1	2 <sup>nd</sup> raster-row
0	0	0	0	0	0	1	0	3 <sup>rd</sup> raster-row
:	:	:	:	:	:	:	:	:
1	0	0	0	0	1	1	0	135 <sup>th</sup> raster-row
1	0	0	0	0	1	1	1	136 <sup>th</sup> raster-row

Note: Do not set over the 136<sup>th</sup> ("87"h) raster-row.

**1st Screen Driving Position (R14h)**

**2nd Screen Driving Position (R15h)**

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

**Figure 14 1st Screen Driving Position and 2nd Screen Driving Position Instructions**

**SS17–0:** Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value + 1' common driver.

**SE17–0:** Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SS17–10 = "07" H and SE17–10 = "10" H are set, the LCD driving is performed from COM8 to COM17, and non-selection driving is performed for COM1 to COM7, COM18, and others. Ensure that SS17–10 ≤ SE17–10 ≤ AFH. For details, see the Screen-division Driving Function section.

**SS27–0:** Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' common driver. The second screen is driven when SPT = 1.

**SE27-0:** Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SPT = 1, SS27-20 = "20"H, and SE27-20 = "4F"H are set, the LCD driving is performed from COM33 to COM80. Ensure that SS17-10 ≤ SE17-10 ≤ SS27-20 ≤ SE27-20 ≤ "87"H. For details, see the Screen-division Driving Function section.

**Horizontal RAM Address Position (R16h)**

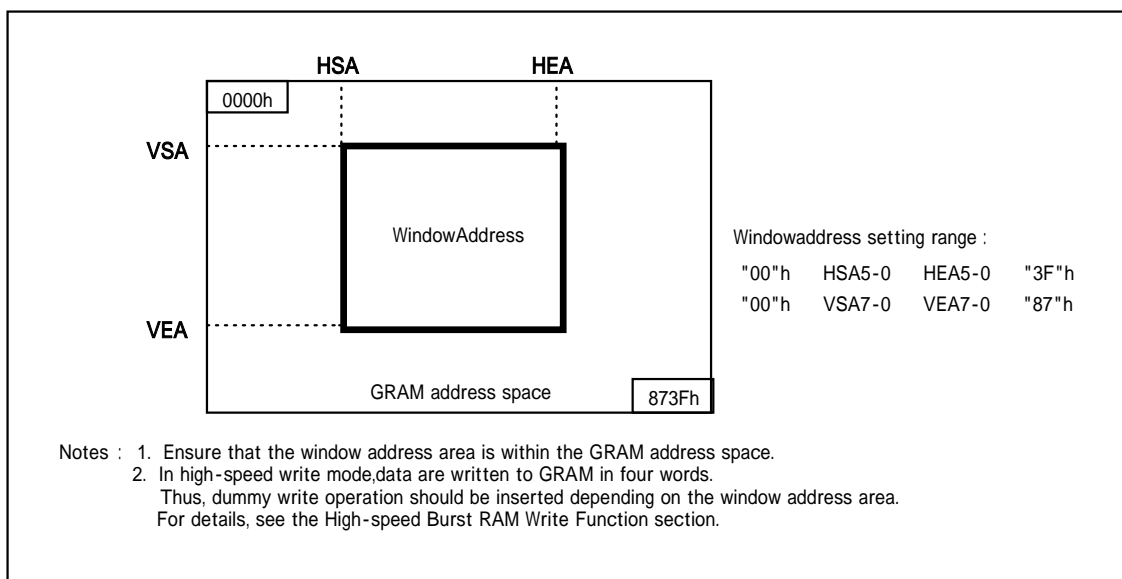
**Vertical RAM Address Position (R17h)**

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	0	0	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

**Figure 15 Horizontal/Vertical RAM Address Position Instruction**

**HSA5-0/HEA5-0:** Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by HEA5-0 from the address specified by HSA5-0. Note that an address must be set before RAM is written to. Ensure "00"h ≤ HSA5-0 ≤ HEA5-0 ≤ "3F"h.

**VSA7-0/VEA7-0:** Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by VEA7-0 from the address specified by VSA7-0. Note that an address must be set before RAM is written to. Ensure "00"h ≤ VSA7-0 ≤ VEA7-0 ≤ "87"h.



**Figure 16 Window Address Setting Range**

RAM Write Data Mask (R20h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WM	WM	WM	WM	WM	WM	WM	WM	WM	WM	WM	WM	WM	WM	WM	WM
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 17 RAM Write Data Mask Instruction

**WM15–0:** In writing to the GRAM, these bits mask writing in a bit unit. When WM15 = 1, this bit masks the write data of DB15 and does not write to the GRAM. Similarly, the WM14–0 bits mask the write data of DB14–0 in a bit unit. When SWP = 1, the upper and lower bytes in the write data mask are swapped. For details, see the Graphics Operation Function section.

RAM Address Set (R21h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	AD	AD	AD	AD	AD	AD	AD9	AD8	0	0	AD5	AD4	AD3	AD2	AD1	AD0
		15	14	13	12	11	10										

Figure 18 RAM Address Set Instruction

**AD15–0:** Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting addresses. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address.

Table 20 GRAM Address Range in Eight-grayscale Mode

AD14–AD0	GRAM Setting
"0000"H–"003F"H	Bitmap data for COM1
"0100"H–"013F"H	Bitmap data for COM2
"0200"H–"023F"H	Bitmap data for COM3
"0300"H–"033F"H	Bitmap data for COM4
:	:
"8400"H–"843F"H	Bitmap data for COM133
"8500"H–"853F"H	Bitmap data for COM134
"8600"H–"863F"H	Bitmap data for COM135
"8700"H–"873F"H	Bitmap data for COM136

Write Data to GRAM (R22h)

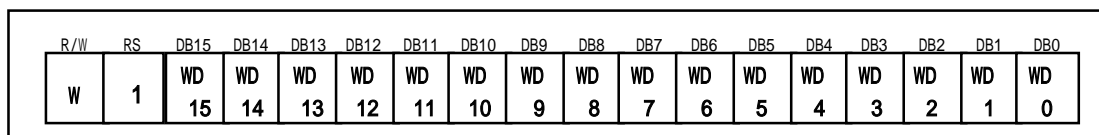


Figure 19 Write Data to GRAM Instruction

**WD15-0** : Write 16-bit data to the GRAM. This data calls each grayscale palette. After a write, the address is automatically updated according to the AM and I/D bit settings. During the standby mode, the GRAM cannot be accessed.

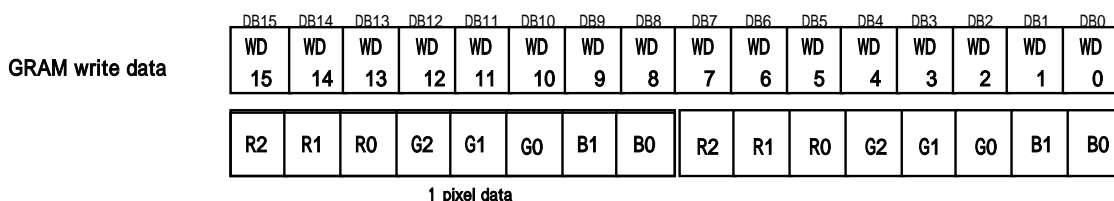


Figure 20 GRAM Write Data Instruction

Table 21 GRAM Data in the Eight-grayscale Mode (R Grayscale Palette)

GRAM Data Setting			
R2	R1	R0	<R> Grayscale Palette
0	0	0	RK03                      RK02                      RK01                      RK00
0	0	1	RK13                      RK12                      RK11                      RK10
0	1	0	RK23                      RK22                      RK21                      RK20
0	1	1	RK33                      RK32                      RK31                      RK30
1	0	0	RK43                      RK42                      RK41                      RK40
1	0	1	RK53                      RK52                      RK51                      RK50
1	1	0	RK63                      RK62                      RK61                      RK60
1	1	1	RK73                      RK72                      RK71                      RK70

Table 22 GRAM Data in the Eight-grayscale Mode (G Grayscale Palette)

GRAM Data Setting						
G2	G1	G0	<G> Grayscale Palette			
0	0	0	GK03	GK02	GK01	GK00
0	0	1	GK13	GK12	GK11	GK10
0	1	0	GK23	GK22	GK21	GK20
0	1	1	GK33	GK32	GK31	GK30
1	0	0	GK43	GK42	GK41	GK40
1	0	1	GK53	GK52	GK51	GK50
1	1	0	GK63	GK62	GK61	GK60
1	1	1	GK73	GK72	GK71	GK70

Table 23 GRAM Data in the Eight-grayscale Mode (B Grayscale Palette)

GRAM Data Setting					
B1	B0	<B> Grayscale Palette			
0	0	BK03	BK02	BK01	BK00
0	1	BK13	BK12	BK11	BK10
1	0	BK23	BK22	BK21	BK20
1	1	BK33	BK32	BK31	BK30

Read Data from GRAM (R22h)

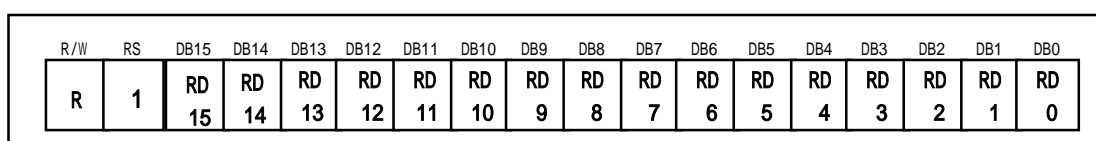


Figure 21 Read Data from GRAM Instruction

**RD15–0:** Read 16-bit data from the GRAM. When the data is read to the microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB15–0) becomes invalid and the second-word read is normal. When bit processing, such as a logical operation, is performed within the HD66762, only one read can be processed since the latched data in the first word is used.



Grayscale Palette Control (R30h to R39h)

	R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R30	W	1	0	0	0	0	RK 13	RK 12	RK 11	RK 10	0	0	0	0	RK 03	RK 02	RK 01	RK 00
R31	W	1	0	0	0	0	RK 33	RK 32	RK 31	RK 30	0	0	0	0	RK 23	RK 22	RK 21	RK 20
R32	W	1	0	0	0	0	RK 53	RK 52	RK 51	RK 50	0	0	0	0	RK 43	RK 42	RK 41	RK 40
R33	W	1	0	0	0	0	RK 73	RK 72	RK 71	RK 70	0	0	0	0	RK 63	RK 62	RK 61	RK 60
R34	W	1	0	0	0	0	GK 13	GK 12	GK 11	GK 10	0	0	0	0	GK 03	GK 02	GK 01	GK 00
R35	W	1	0	0	0	0	GK 33	GK 32	GK 31	GK 30	0	0	0	0	GK 23	GK 22	GK 21	GK 20
R36	W	1	0	0	0	0	GK 53	GK 52	GK 51	GK 50	0	0	0	0	GK 43	GK 42	GK 41	GK 40
R37	W	1	0	0	0	0	GK 73	GK 72	GK 71	GK 70	0	0	0	0	GK 63	GK 62	GK 61	GK 60
R38	W	1	0	0	0	0	BK 13	BK 12	BK 11	BK 10	0	0	0	0	BK 03	BK 02	BK 01	BK 00
R39	W	1	0	0	0	0	BK 33	BK 32	BK 31	BK 30	0	0	0	0	BK 23	BK 22	BK 21	BK 20

Figure 23 Grayscale Palette Control Instruction

**RK73-00:** Specify the R-grayscale level for eight palettes from the 16-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

**GK73-00:** Specify the G-grayscale level for eight palettes from the 16-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

**BK33-00:** Specify the B-grayscale level for four palettes from the 16-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

Instruction List

Reg. No.	Register Name	R/W	RS	Upper Code																Description	Execution Cycle			
				DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0					
IR	Index	0	0	*	*	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	Sets the index register value.	0	
SR	Status read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0	Reads the driving raster-row position (L7-0) and contrast setting (C6-0).	0			
R00h	Start oscillation	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	Starts the oscillation mode.	10 ms
	Device code read	1	1	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	0	Reads 0762H.	0		
R01h	Driver output control	0	1	0	0	0	0	0	0	CMS	SGS	0	0	0	NL4	NL3	NL2	NL1	NL0	Sets the common driver shift direction (CMS), segment driver shift direction (SGS) and driving duty ratio (NL4-0).	0			
R02h	LCD-driving-waveform control	0	1	0	0	0	0	0	RST	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0	Sets the software reset (RST), LCD drive AC waveform (B/C), and EOR output (EOR) or the number of n-raster-rows (NW5-0) at C-pattern AC drive.	0			
R03h	Power control 1	0	1	BS3	BS2	BS1	BS0	BT3	BT2	BT1	BT0	0	DC2	DC1	DC0	AP1	AP0	SLP	STB	Sets the sleep mode (SLP), standby mode (STB), LCD power on (AP1-0), boosting cycle (DC2-0), control polarity inversion circuit (BT3), boosting output multiplying factor (BT2-0), and LCD drive bias value (BS3-0).	0			
R04h	Contrast control	0	1	0	0	0	0	0	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0	Sets the regulator adjustment (VR2-0) and contrast adjustment (CT6-0).	0			
R05h	Entry mode	0	1	0	0	0	0	0	0	HW	SWP	M	0	0	I/D1	I/D0	AM	LG2	LG1	LG0	Specifies the logical operation (LG2-0), AC counter mode (AM), increment/decrement mode (I/D1-0), swap (SWP) and high speed write mode (HWM).	0		
R06h	Compare	0	1	0	0	0	0	0	0	0	0	0	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	Specifies the compare register (CP7-0).	0		
R07h	Display control	0	1	0	0	0	0	0	0	VLE2	VLE1	SPT	0	0	0	0	B/W	REV	D1	D0	Specifies display on (D1-0), black-and-white reversed display (REV), pixel on/off mode (B/W), screen division driving (SPT) and vertical scroll (VLE2-1)	0		
R0Bh	Frame frequency control	0	1	0	0	0	0	0	0	0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0	Specifies the line retrace period (RTN3-0) and operating clock frequency division ratio (DIV1-0).	0		
R0Ch	Power control 2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0	Sets an adjustment factor for the Vci voltage (VC2-0).	0		
R11h	Vertical scroll control	0	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10	Sets the 1 <sup>st</sup> screen display start raster row (VL17-10) and 2 <sup>nd</sup> screen display start raster row (VL27-20)	0			
R14h	1 <sup>st</sup> screen driving position	0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	Sets 1 <sup>st</sup> screen driving start position (SS17-10) and 1 <sup>st</sup> screen driving end position (SE17-10).	0			
R15h	2 <sup>nd</sup> screen driving position	0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	Sets 2 <sup>nd</sup> screen driving start position (SS27-20) and 2 <sup>nd</sup> screen driving end position (SE27-20).	0			
R16h	Horizontal RAM address position	0	1	0	0	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	0	0	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	Sets start (HSA5-0) and end (HEA5-0) of the horizontal RAM address range.	0			
R17h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	Sets start (VSA7-0) and end (VEA7-0) of the vertical RAM address range.	0			
R20h	RAM write data mask	0	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	Specifies write data mask (WM15-0) at RAM write.	0			

Instruction List (cont.)

Reg. No.	Register Name	R/W	RS	Upper Code								Lower Code								Description	Execution Cycle														
				DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0																
R21h	RAM address set	0	1																	AD15-8 (upper)	0	0											AD5-0 (lower)	Initially set the RAM address to the counter (AC).	0
R22	RAM data write	0	1																	Write data (upper)			Write data (lower)									Writes data to the RAM.	0		
	RAM data read	1	1																	Read data (upper)			Read data (lower)									Reads data to the RAM.	0		
R30h	R grayscale palette control (1)	0	1	0	0	0	0	RK 13	RK 12	RK 11	RK 10	0	0	0	0	RK 03	RK 02	RK 01	RK 00													Specifies the R grayscale palette.	0		
R31h	R grayscale palette control (2)	0	1	0	0	0	0	RK 33	RK 32	RK 31	RK 30	0	0	0	0	RK 23	RK 22	RK 21	RK 20													Specifies the R grayscale palette.	0		
R32h	R grayscale palette control (3)	0	1	0	0	0	0	RK 53	RK 52	RK 51	RK 50	0	0	0	0	RK 43	RK 42	RK 41	RK 40													Specifies the R grayscale palette.	0		
R33h	R grayscale palette control (4)	0	1	0	0	0	0	RK 73	RK 72	RK 71	RK 70	0	0	0	0	RK 63	RK 62	RK 61	RK 60													Specifies the R grayscale palette.	0		
R34h	G grayscale palette control (1)	0	1	0	0	0	0	GK 13	GK 12	GK 11	GK 10	0	0	0	0	GK 03	GK 02	GK 01	GK 00													Specifies the G grayscale palette.	0		
R35h	G grayscale palette control (2)	0	1	0	0	0	0	GK 33	GK 32	GK 31	GK 30	0	0	0	0	GK 23	GK 22	GK 21	GK 20													Specifies the G grayscale palette.	0		
R36h	G grayscale palette control (3)	0	1	0	0	0	0	GK 53	GK 52	GK 51	GK 50	0	0	0	0	GK 43	GK 42	GK 41	GK 40													Specifies the G grayscale palette.	0		
R37h	G grayscale palette control (4)	0	1	0	0	0	0	GK 73	GK 72	GK 71	GK 70	0	0	0	0	GK 63	GK 62	GK 61	GK 60													Specifies the G grayscale palette.	0		
R38h	B grayscale palette control (1)	0	1	0	0	0	0	BK 13	BK 12	BK 11	BK 10	0	0	0	0	BK 03	BK 02	BK 01	BK 00													Specifies the B grayscale palette.	0		
R39h	B grayscale palette control (2)	0	1	0	0	0	0	BK 33	BK 32	BK 31	BK 30	0	0	0	0	BK 23	BK 22	BK 21	BK 20													Specifies the B grayscale palette.	0		

Note: 1. “\*” means doesn’t matter.

2. High-speed write mode is available only for the RAM writing.

**Reset Function**

The HD66762 is internally initialized by RESET input. Reset the common driver as its settings are not automatically reinitialized when the HD66762 is reset. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

**Instruction Set Initialization:**

1. Start oscillation executed
2. Driver output control (NL4-0 = 10000, SGS = 0, CMS = 0)
3. B-pattern waveform AC drive (B/C = 0, ECR = 0, NW5-0 = 00000)
4. Power control 1 (DC2-0 = 000, AP1-0 = 00: LCD power off, STB = 0: Standby mode off, SLP = 0, BS3-0 = 0000, BT3-0 = 0000)
5. Contrast control (Weak contrast VR2-0 = 000, CT6-0 = 0000000)
6. Entry mode set (HWM = 0, SWP = 0, I/D1-0 = 11: Increment by 1, AM = 0: Horizontal move, LG2-0 = 000: Replace mode)
7. Compare register (CP7-0: 00000000)
8. Display control (VLE2-1 = 00: No vertical scroll, SPT = 0, REV = 0, D1-0 = 00: Display off)
9. Frame cycle control (DIV1-0 = 00: 1-divided clock, RTN3-0: No retrace line period)
10. Power control 2 (VC2-0 = 000)
11. Vertical scroll (VL27-20 = 00000000, VL17-10 = 00000000)
12. 1st screen division (SE17-10 = 11111111, SS17-10 = 00000000)
13. 2nd screen division (SE27-20 = 11111111, SS27-20 = 00000000)
14. Horizontal RAM address position (HEA5-0 = 111111, HSA5-0 = 000000)
15. Vertical RAM address position (VEA7-0 = 10000111, VSA7-0 = 00000000)
16. RAM write data mask (WM15-0 = 0000H: No mask)
17. RAM address set (AD15-0 = 0000H)
18.  
(RK03-00 = 0000, RK13-10 = 0011, RK23-20 = 0101, RK33-30 = 0111,  
RK43-40 = 1001, RK53-50 = 1011, RK63-60 = 1101, RK73-70 = 1111,  
GK03-00 = 0000, GK13-10 = 0011, GK23-20 = 0101, GK33-30 = 0111,  
GK43-40 = 1001, GK53-50 = 1011, GK63-60 = 1101, GK73-70 = 1111,  
BK03-00 = 0000, BK23-20 = 0101, BK43-40 = 1001, BK63-60 = 1111)

**GRAM Data Initialization:**

This is not automatically initialized by reset input but must be initialized by software while display is off (D1-0 = 00).

**Output Pin Initialization:**

1. LCD driver output pins (SEG/COM): Output GND level
2. Oscillator output pin (OSC2): Outputs oscillation signal

## Parallel Data Transfer

### 16-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/GND/GND level allows 68-system E-clock-synchronized 16-bit parallel data transfer. Setting the IM2/1/0 to the GND/Vcc/GND level allows 80-system 16-bit parallel data transfer. When the number of buses or the mounting area is limited, use an 8-bit bus interface.

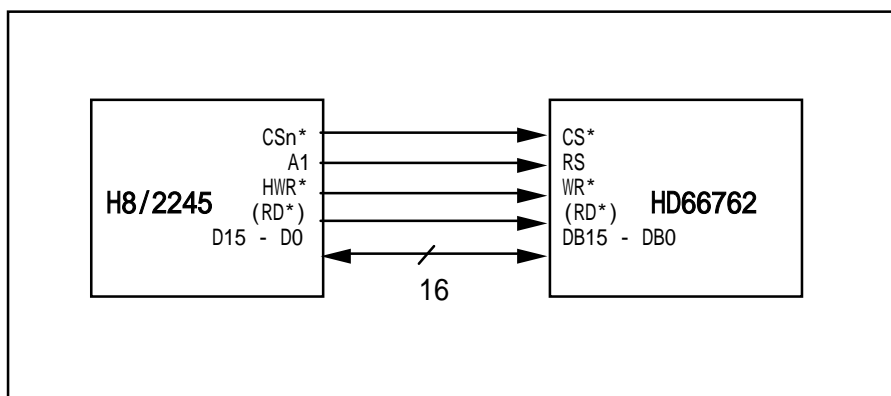
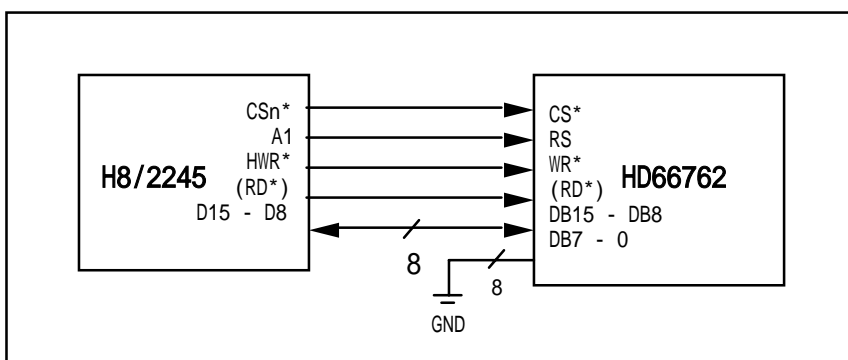


Figure 24 Interface to 16-bit Microcomputer

### 8-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/GND/Vcc level allows 68-system E-clock-synchronized 8-bit parallel data transfer using pins DB15-DB8. Setting the IM1/0 to the Vcc/Vcc level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB7-DB0 to the Vcc or GND level. Note that the upper bytes must also be written when the index register



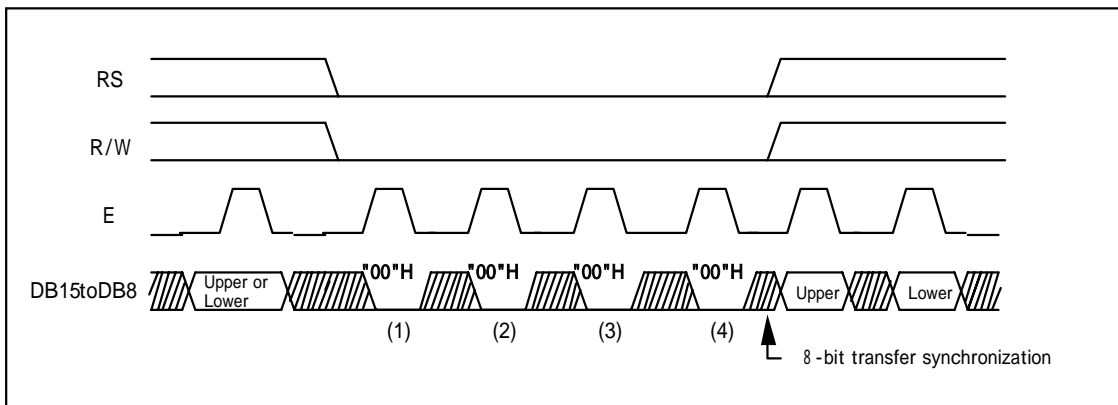
is written to.

Figure 25 Interface to 8-bit Microcomputer

Note: Transfer synchronization function for an 8-bit bus interface

The HD66762 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface.

Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a "00"H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.



**Figure 26 8-bit Transfer Synchronization**

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## HD66762

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### Serial Data Transfer

Setting the IM1 pin to the GND level and the IM2 pin to the Vcc level allows standard clock-synchronized serial data transfer, using the chip select line (CS\*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB15-2 and RS pins, which are not used, must be fixed at Vcc or GND.

The HD66762 initiates serial data transfer by transferring the start byte at the falling edge of CS\* input. It ends serial data transfer at the rising edge of CS\* input.

The HD66762 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66762. The HD66762, when selected, receives the subsequent data string. The ID pin can determine the least significant bit of the identification code. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66762 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.

After receiving the start byte, the HD66762 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All HD66762 instructions are 16 bits. Two bytes are received with the MSB first (DB15 to 0), then the instructions are internally executed. After the start byte has been received, the first byte is fetched internally as the upper eight bits of the instruction and the second byte is fetched internally as the lower eight bits of the instruction.

Fifth bytes of RAM read data after the start byte are invalid. The HD66762 starts to read correct RAM data from the sixth byte.

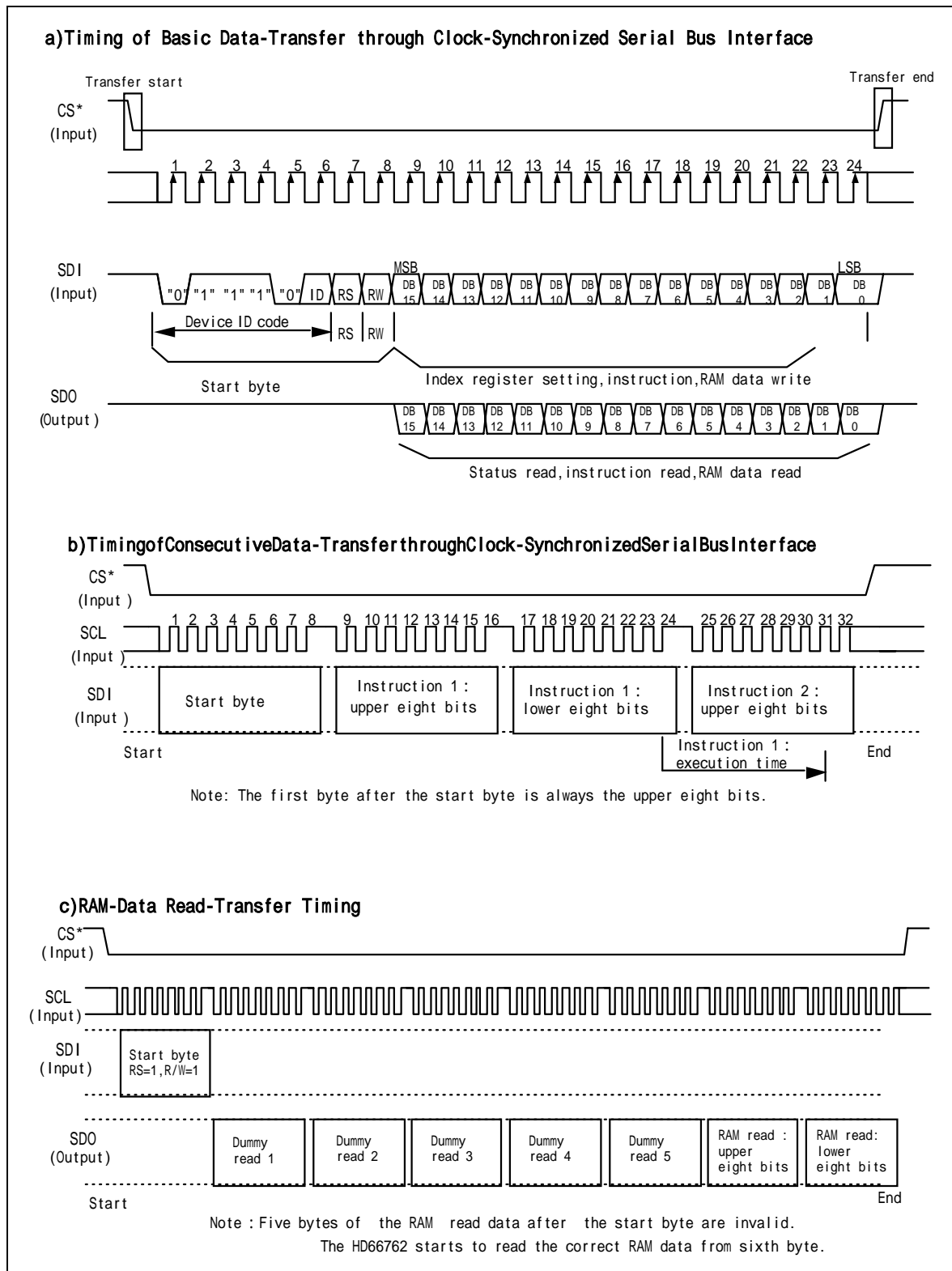
**Table 24 Start Byte Format**

Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: The IM0/ID pin selects ID bit.

**Table 25 RS and R/W Bit Function**

RS	R/W	Function
0	0	Sets index register
0	1	Reads status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data



**Figure 27 Procedure for transfer through the clock synchronized serial interface**



### High-Speed Burst RAM Write Function

The HD66762 has a high-speed burst RAM-write function that can be used to write data to RAM in one-fourth the access time required for an equivalent standard RAM-write operation. This function is especially suitable for applications, which require the high-speed rewriting of the display data, for example, display of color animations, etc.

When the high-speed RAM-write mode (HWM) is selected, data for writing to RAM is once stored to the HD66762 internal register. When data is selected four times per word, all data is written to the on-chip RAM. While this is taking place, the next data can be written to an internal register so that high-speed and consecutive RAM writing can be executed for animated displays, etc.

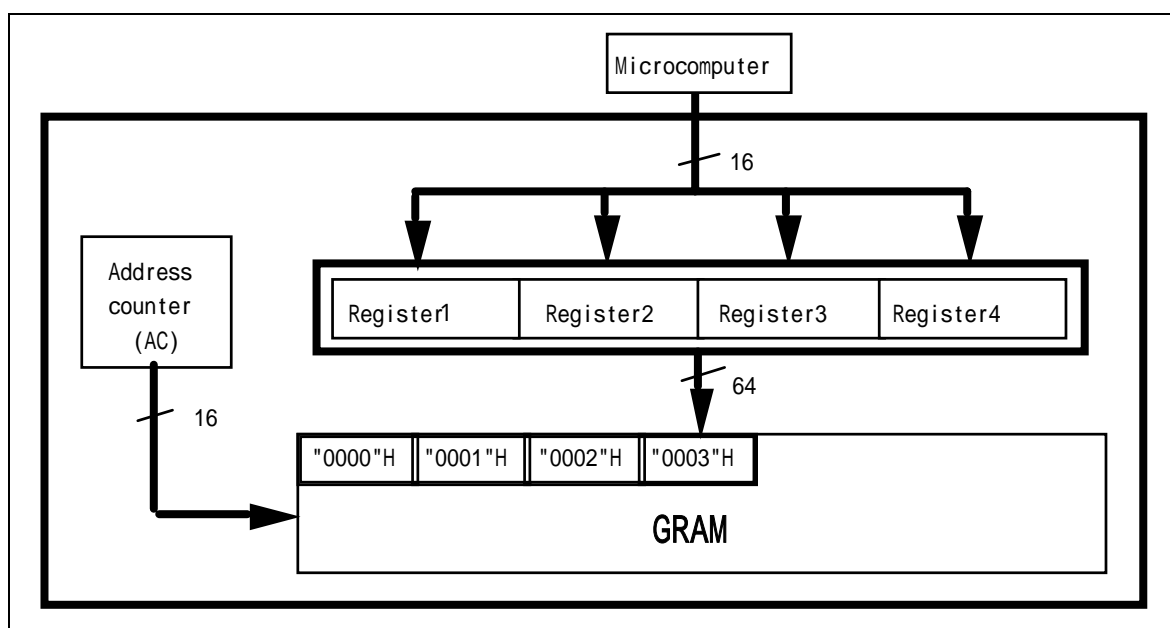
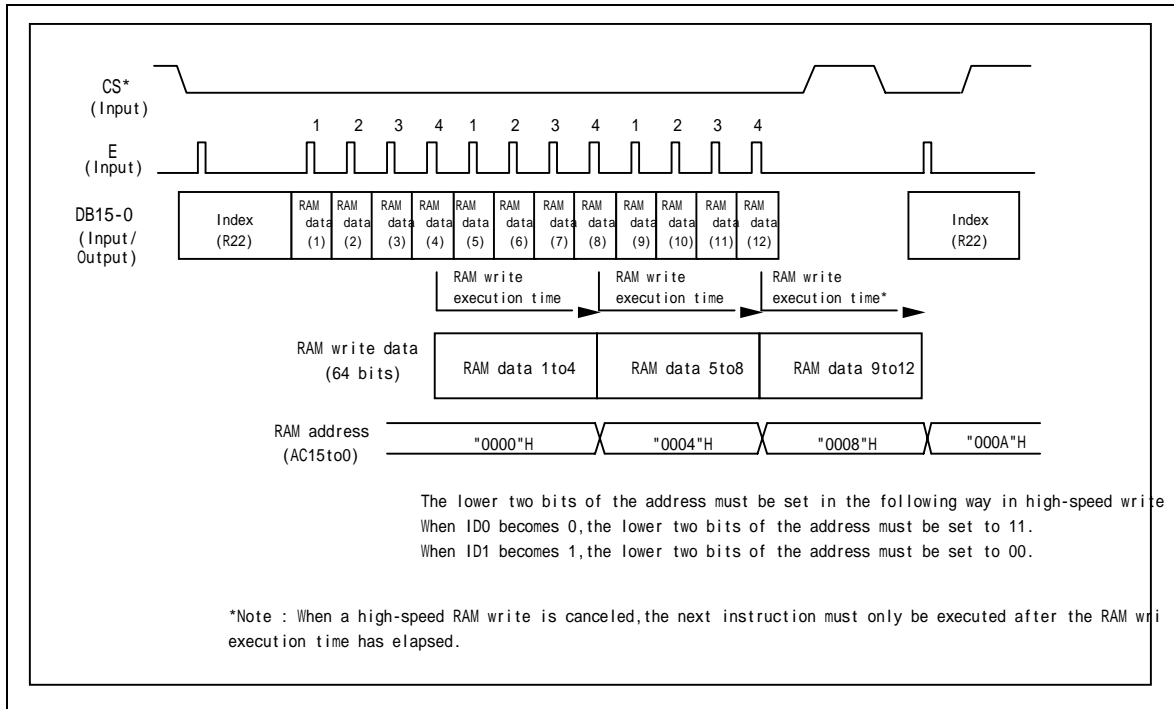


Figure 28 Flow of Operation in High-Speed Consecutive Writing to RAM



**Figure 29 Example of the Operation of High-Speed Consecutive Writing to RAM**

When high-speed RAM write mode is used, note the following.

- Notes:
1. The logical and compare operations cannot be used.
  2. Data is written to RAM each four words. When an address is set, the lower two bits in address must be set to the following values.
    - \*When I/D0=0, the lower two bits in the address must be set to 11 and be written to RAM.
    - \*When I/D0=1, the lower two bits in the address must be set to 00 and be written to RAM.
  3. Data is written to RAM each four words. If less than four words of data is written to RAM, the last data will not be written to RAM.
  4. When the index register and RAM data write (“22”H) have been selected, the data is always written first. RAM cannot be written to and read from at the same time. HWM must be set to 0 while RAM is being read.
  5. High-speed and normal RAM write-operations cannot be executed at the same time. The mode must be switched and the address must then be set.
  6. When high-speed RAM write is used with a window address-range specified, dummy write operation may be required to suit the window address range specification. Refer to the High-speed RAM Write in the Window Address section.

**Table 26 Comparison between Normal and High-Speed RAM Write Operations**

	<b>Normal RAM Write (HWM=0)</b>	<b>High-Speed RAM Write (HWM=1)</b>
Logical operation function	Can be used	Cannot be used
Compare operation function	Can be used	Cannot be used
Swap function	Can be used	Can be used
Write mask function	Can be used	Can be used
RAM address set	Can be specified by word	ID0 bit=0: Set the lower two bits to 11 ID0 bit=1: Set the lower two bits to 00
RAM read	Can be read by word	Cannot be used
RAM write	Can be written by word	Dummy write operations may have to be inserted according to a window address-range specification
Window address	Can be set by word	Can be set by word

**High-Speed RAM Write in the Window Address**

When a window address range is specified, RAM data which is in an optional window area can be rewritten consecutively and quickly by inserting dummy write operations so that RAM access counts become  $4N$  as shown in the tables below.

Dummy write operations may have to be inserted as the first or last operations for a row of data, depending on the horizontal window-address range specification bits (HSA1 to 0, HEA1 to 0). Numbers of dummy write operations of a row must be  $4N$ .

**Table 27 Numbers of Dummy Write Operations in High-Speed RAM Write (HSA Bits)**

HSA1	HSA0	Numbers of Dummy Write Operations to be Inserted at the Start of a Row
0	0	0
0	1	1
1	0	2
1	1	3

**Table 28 Numbers of Dummy Write Operations in High-Speed RAM Write (HEA Bits)**

HEA1	HEA0	Numbers of Dummy Write Operations to be Inserted at the End of a Row
0	0	3
0	1	2
1	0	1
1	1	0

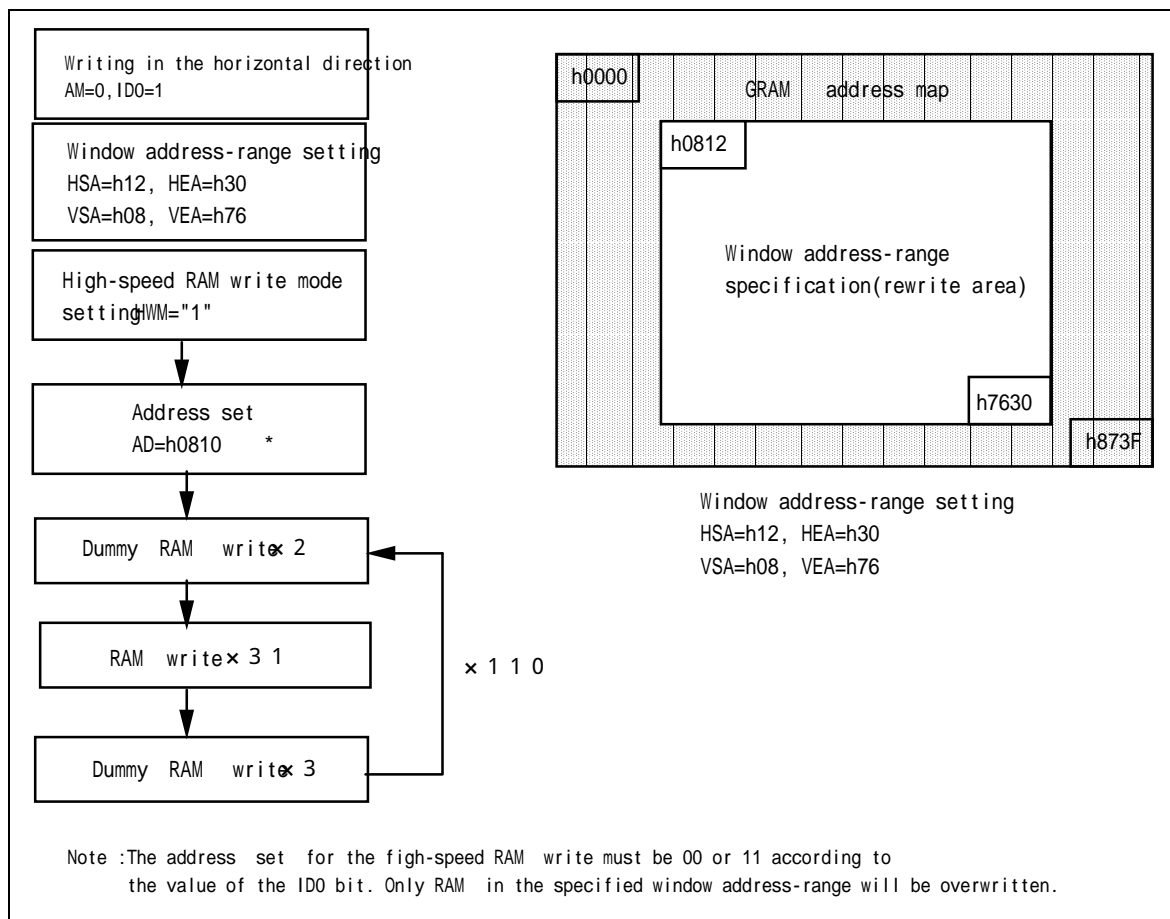
Each row of access must consist of  $4 \times N$  operations, including the dummy writes.

Horizontal access count = first dummies write count + write data count + last dummy write count =  $4 \times N$

An example of high-speed RAM write with a window address-range specified is shown below.

The window address-range can be rewritten to consecutively and quickly by inserting two dummies writes

at the start of a row and three dummy writes at the end of a row, as determined by window address-range specification bits (HSA1 to 0=10, HEA1 to 0=00).



**Figure 30** Example of the High-Speed RAM write with a window address-range specification

### Window Address Function

When data is written to the on-chip GRAM, a window address-range which is specified by the horizontal address register (start: HSA5-0, end: HEA5-0) or the vertical address register (start: VSA7-0, end: VEA7-0) can be written to consecutively.

Data is written to addresses in the direction specified by the AM bit (increment/decrement). When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.

The window must be specified to be within the GRAM address area described below. Addresses must be set within the window address.

[Restriction on window address-range settings]

(Horizontal direction)  $"00"H \leq HSA5-0 \leq HEA5-0 \leq "3F"H$

(Vertical direction)  $"00"H \leq VSA7-0 \leq VEA7-0 \leq "87"H$

[Restriction on address settings during the window address]

(RAM address)  $HSA5-0 \leq AD5-0 \leq HEA5-0$

$VSA7-0 \leq AD15-8 \leq VEA7-0$

Note: In high-speed RAM-write mode, the lower two bits of the address must be set as shown below according to the value of the ID0 bit.

ID0=0: The lower two bits of the address must be set to 11.

ID0=1: The lower two bits of the address must be set to 00.

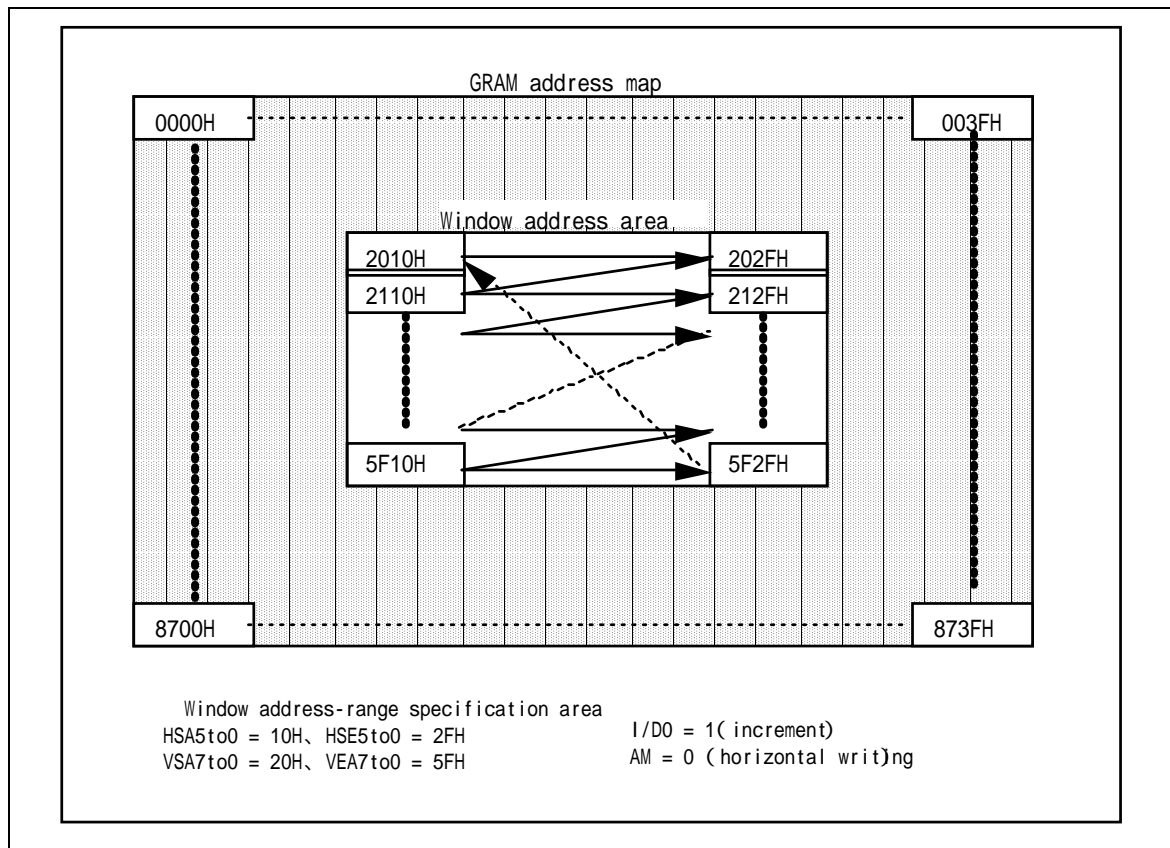


Figure 31 Example of Address Operation in the Window Address Specification

## Graphics Operation Function

The HD66762 can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and internal graphics-bit operation function.

This function supports the following:

1. A swap function that exchanges the upper and lower bytes in the 16-bit data sent the microcomputer.
2. A write data mask function that selectively rewrites some of the bits in the 16-bit write data.
3. Logical operations write function that writes the data sent from the microcomputer and the original RAM data by a logical operation.
4. A conditional write function that compares the original RAM data or write data and the compare-bit data and writes the data sent from the microcomputer only when the conditions match.

Even if the display size is large, the display data in the graphics RAM (GRAM) can be quickly rewritten. The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the read/write from the microcomputer.

**Table 29 Graphics Operation**

Operation Mode	Bit Setting			Operation and Usage
	I/D	AM	LG2-0	
Write mode 1	0/1	0	000	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	1	000	Vertical data replacement, vertical-border drawing
Write mode 3	0/1	0	110, 111	Conditional horizontal data replacement, horizontal-border drawing
Write mode 4	0/1	1	110, 111	Conditional vertical data replacement, vertical-border drawing
Read/write mode 1	0/1	0	001, 010, 011	Horizontal data write with logical operation, horizontal-border drawing
Read/write mode 2	0/1	1	001, 010, 011	Vertical data write with logical operation, vertical-border drawing
Read/write mode 3	0/1	0	100, 101	Conditional horizontal data replacement, horizontal-border drawing
Read/write mode 4	0/1	1	100, 101	Conditional vertical data replacement, vertical-border drawing

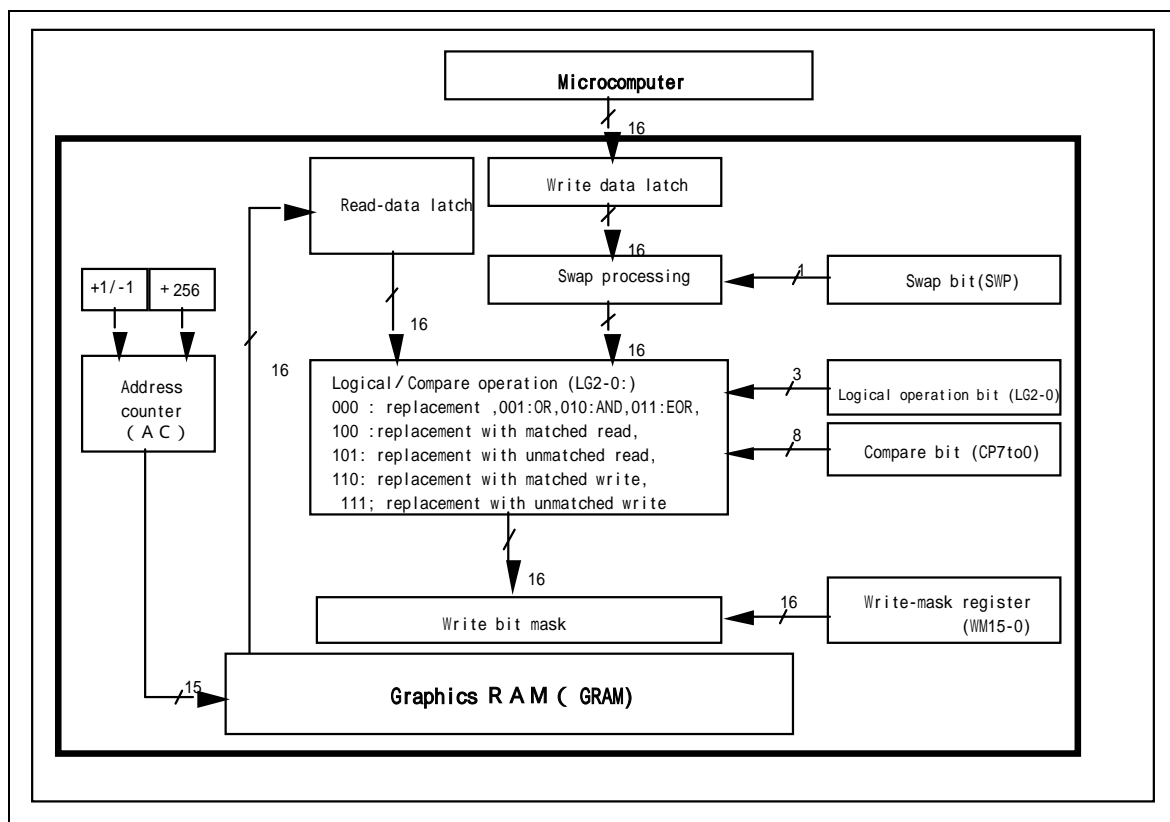
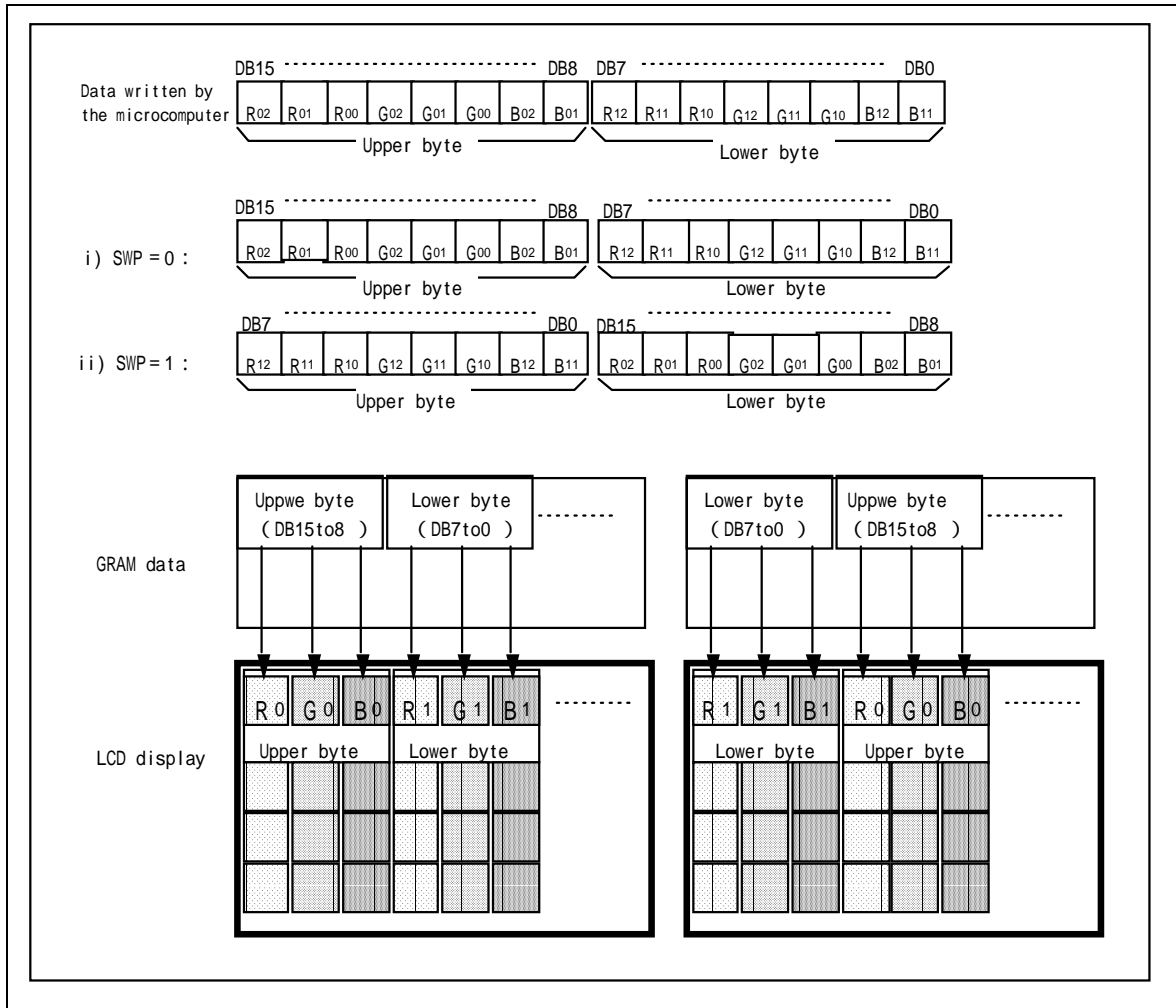


Figure 32 Data Processing Flow of the Graphics Operation

**Swap Function**

The HD66762 has a byte-wise swap function that exchanges the upper and lower bytes in the two-byte data sent from the microcomputer. When SWP = 0, the data written by the microcomputer is directly transferred to the inside. When SWP = 1, the data written by the microcomputer is internally transferred by exchanging the upper and lower bytes.



**Figure 33 Example of Swap Function Operation**

### Write-data Mask Function

The HD66762 has a bit-wise write-data mask function that controls writing the two-byte data from the microcomputer to the GRAM. Bits that are 0 in the write-data mask register (WM15-0) cause the corresponding DB bit to be written to the GRAM. Bits that are 1 prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is retained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.

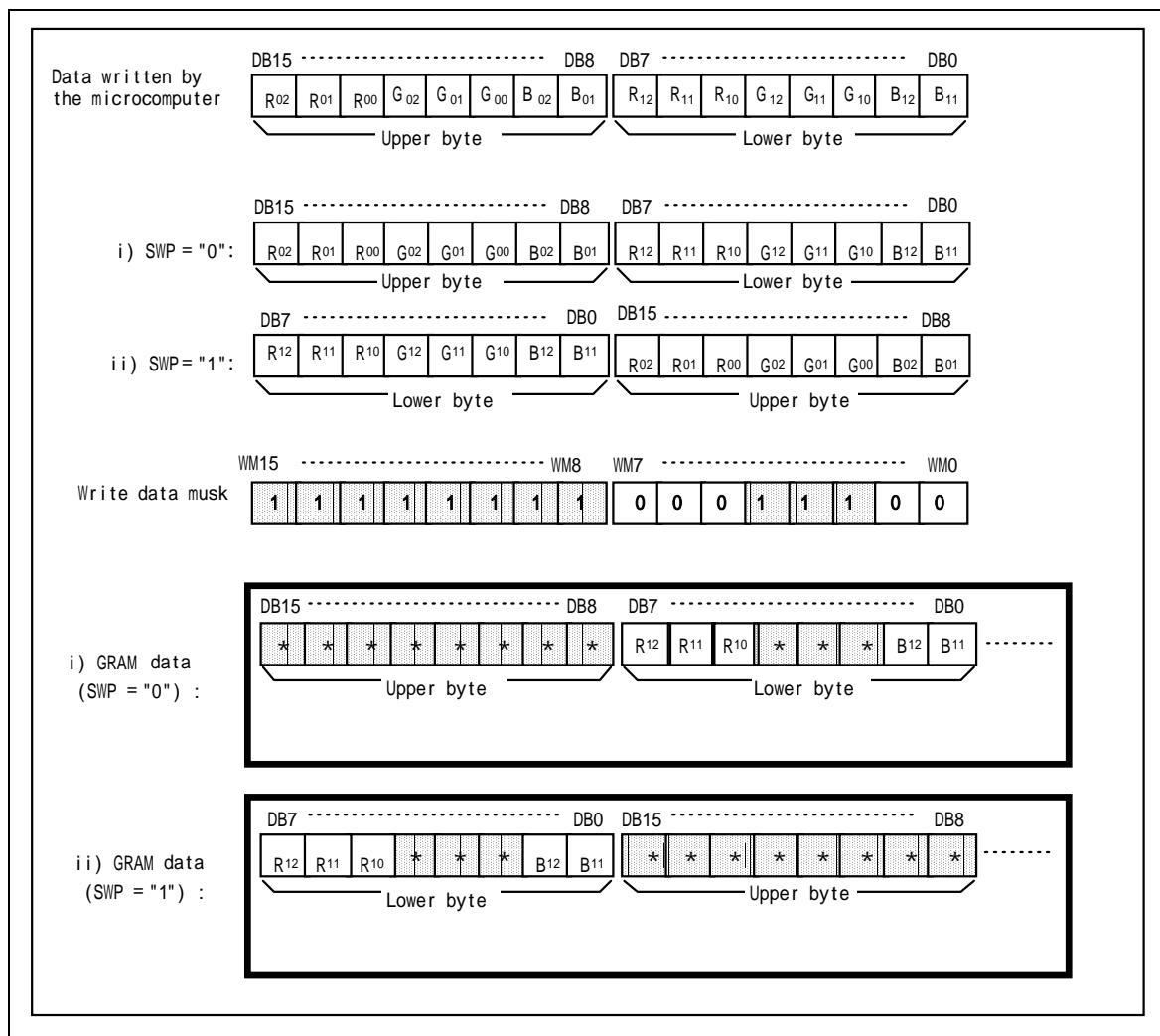


Figure 34 Example of Write-data Mask Function Operation

### Logical/Compare Operation Function

The HD66762 performs a logical operation or conditional replacement between the two-byte write data sent from the microcomputer and the read data from the GRAM.

The logical operation function has four types: replacement, OR, AND, and EOR.

The conditional replacement performs a compare operation for the set value of the compare register (CP7-0) and the read data value from the GRAM, and rewrites only the pixel data in the GRAM that satisfies the conditions (in a byte unit). This function can be used when a particular color is selectively rewritten. The swap function or write-data mask function can be effectively used.

**Table 30 Logical/Compare Operation**

Bit Setting			Description of Logical/Compare Operation Function
LG2	LG1	LG0	
0	0	0	Writes the data written from the microcomputer directly to the GRAM. Only write processing is performed since the data in the read-data latch is not used.
0	0	1	ORs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM. Read, modify, or write processing is performed.
0	1	0	ANDs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM.
0	1	1	EORs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM.
1	0	0	Compares the data in the read-data latch and the set value of the compare register (CP7-0). When the read data matches CP7-0, the data from the microcomputer is written to the GRAM. Only the particular color specified in the compare register can be rewritten. Read, modify, or write processing is performed.
1	0	1	Compares the data in the read-data latch and the set value of the compare register (CP7-0). When the read data does not match CP7-0, the data from the microcomputer is written to the GRAM. Colors other than the particular one specified in the compare register can be rewritten. Read, modify, or write processing is performed.
1	1	0	Compares the data written to the GRAM by the microcomputer and the set value of the compare register (CP7-0). When the write data matches CP7-0, the data from the microcomputer is written to the GRAM. Only write processing is performed.
1	1	1	Compares the data written to the GRAM by the microcomputer and the set value of the compare register (CP7-0). When the write data does not match CP7-0, the data from the microcomputer is written to the GRAM. Only write processing is performed.

### Graphics Operation Processing

1. Write mode 1: AM = 0, LG2-0 = 000

This mode is used when the data is horizontally written at high speed. It can also be used to initialize

the graphics RAM (GRAM) or to draw borders. The swap function (SWP) and write-data mask function (WM15-0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

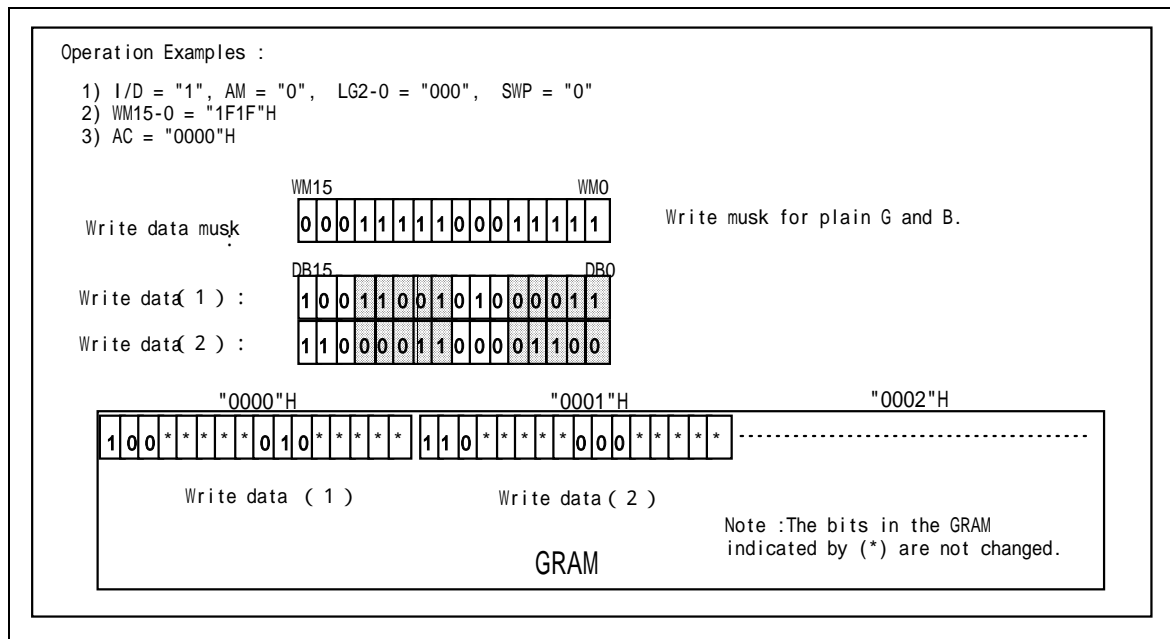
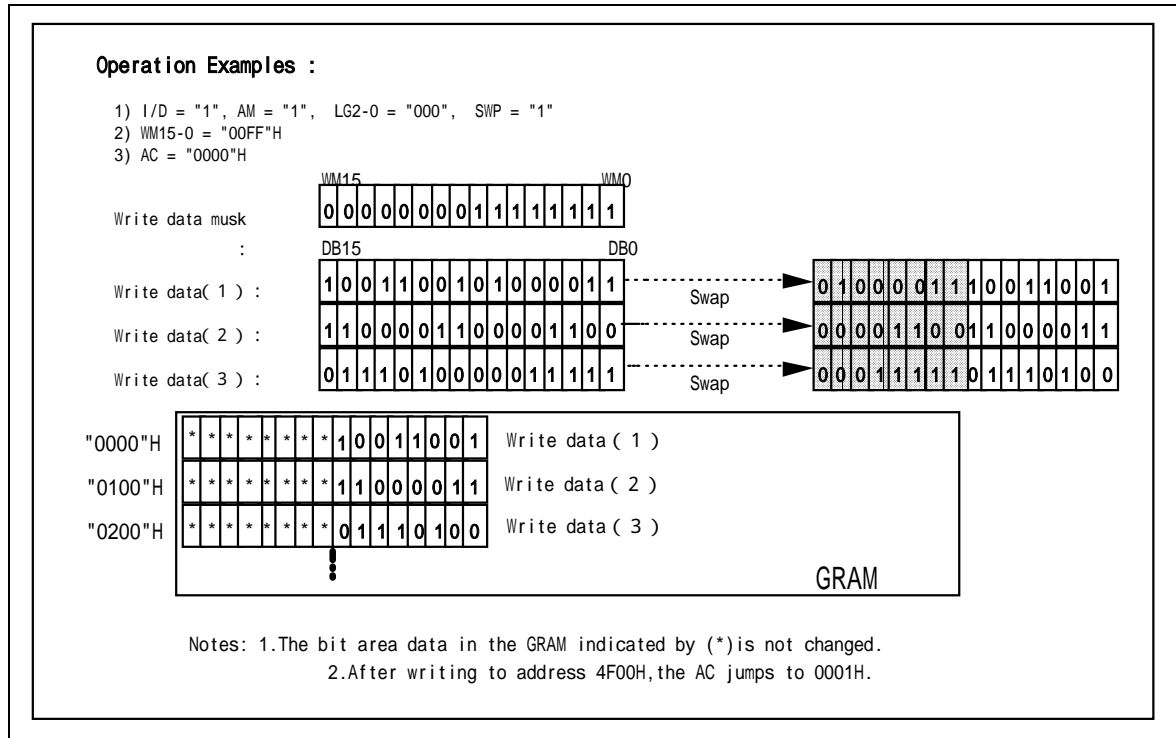


Figure 35 Writing Operation of Write Mode 1

# HD66762

## 2. Write mode 2: AM = 1, LG2-0 = 000

This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The swap function (SWP) and write-data mask function (WM15-0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.



**Figure 36 Writing Operation of Write Mode 2**

3. Write mode 3: AM = 0, LG2-0 = 110/111

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP7-0). When the result of the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the swap function (SWP) and write-data mask function (WM15-0) are also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

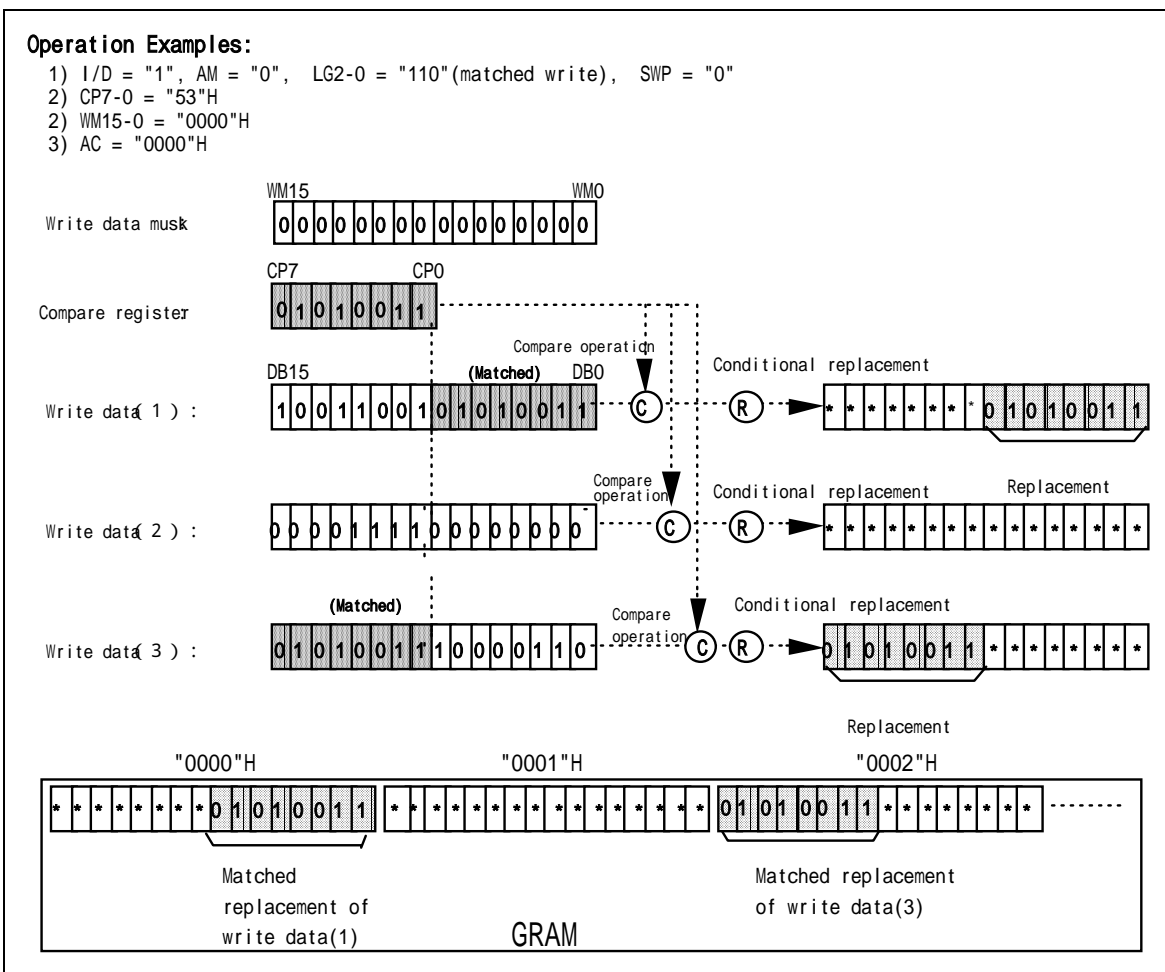


Figure 37 Writing Operation of Write Mode 3

4. Write mode 4: AM = 1, LG2-0 = 110/111

This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP7-0) to write the data. When the result by the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the swap function (SWP) and write-data mask function (WM15-0) are also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

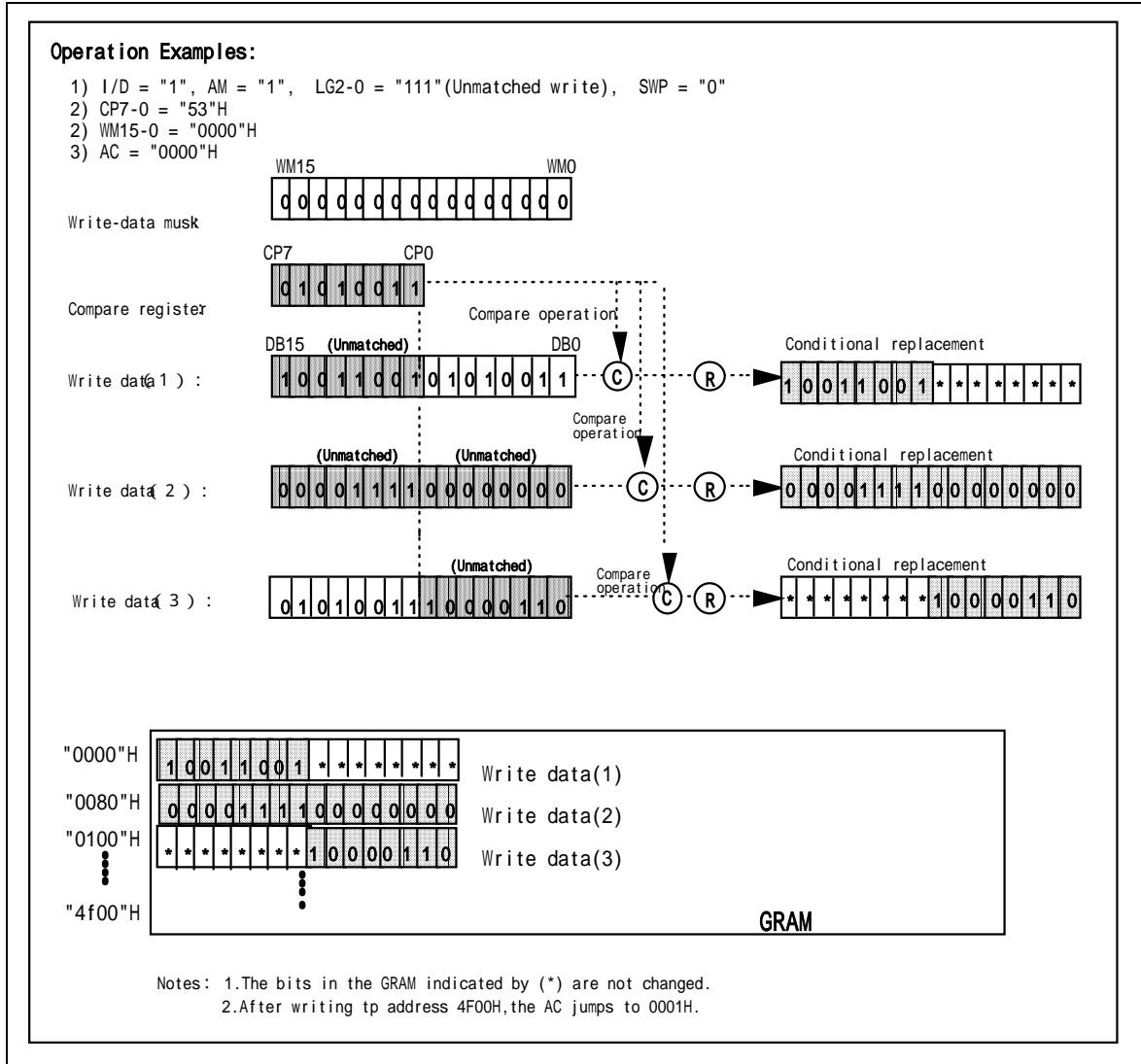


Figure 38 Writing Operation of Write Mode 4

5. Read/Write mode 1: AM = 0, LG2-0 = 001/010/011

This mode is used when the data is horizontally written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD\* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch.

However, the bus cycle requires the same time as the read operation. The swap function (SWP) or write-data mask function (WM15-0) are also enabled in these operations. After writing,

counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

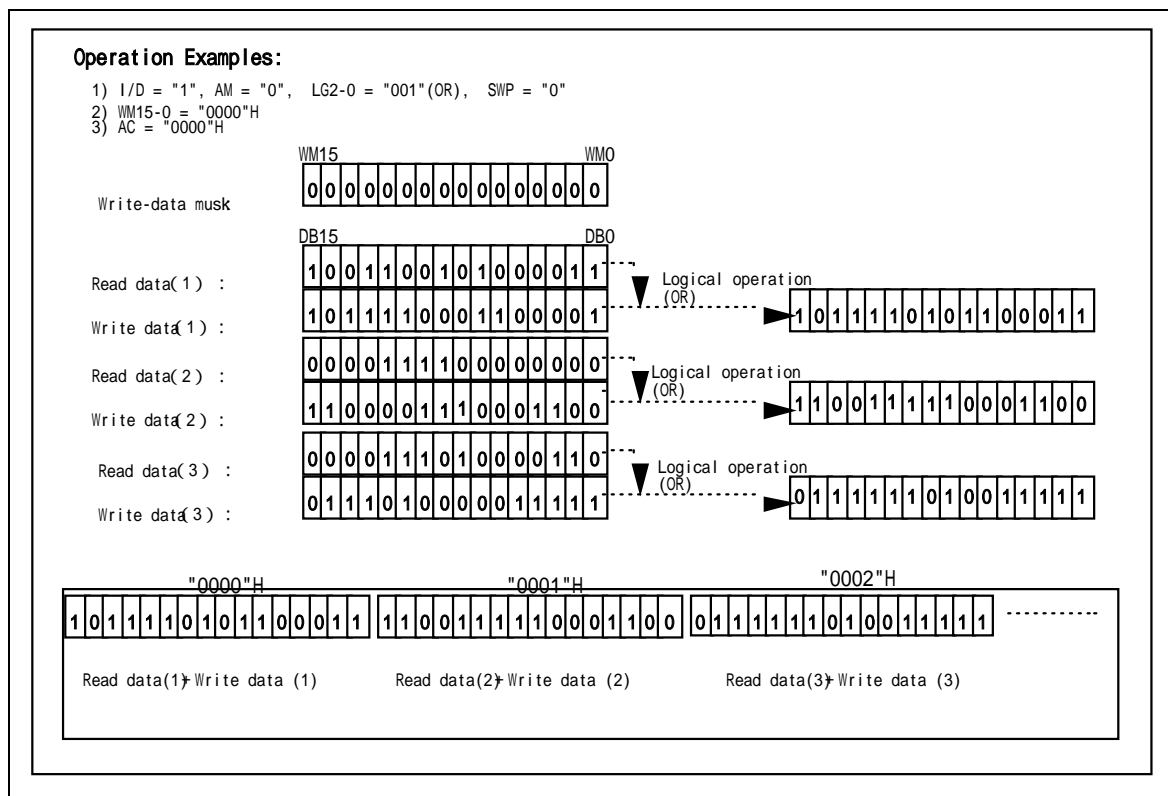


Figure 39 Writing Operation of Read/Write Mode 1

6. Read/Write mode 2: AM = 1, LG1-0 = 001/010/011

This mode is used when the data is vertically written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode can read the data during the same access-pulse width (68-system: enabled high level, 80-system: RD\* low level) as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) or write-data mask function (WM15-0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

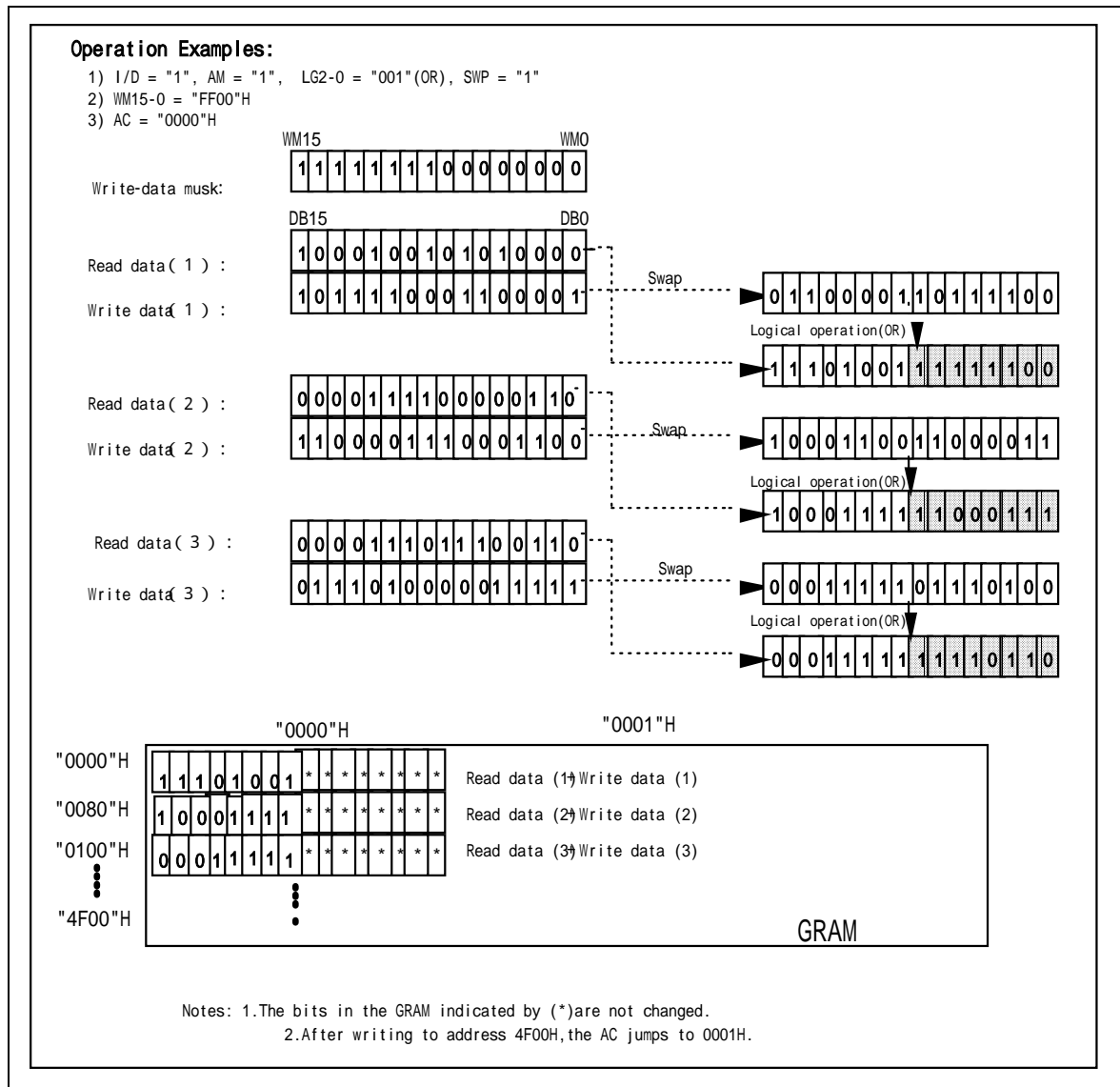


Figure 40 Writing Operation of Read/Write Mode 2

7. Read/Write mode 3: AM = 0, LG2-0 = 100/101

This mode is used when the data is horizontally written by comparing the original data and the set value of compare register (CP7-0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the comparison satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD\* low level) as write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) and write-data mask function (WM15-0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

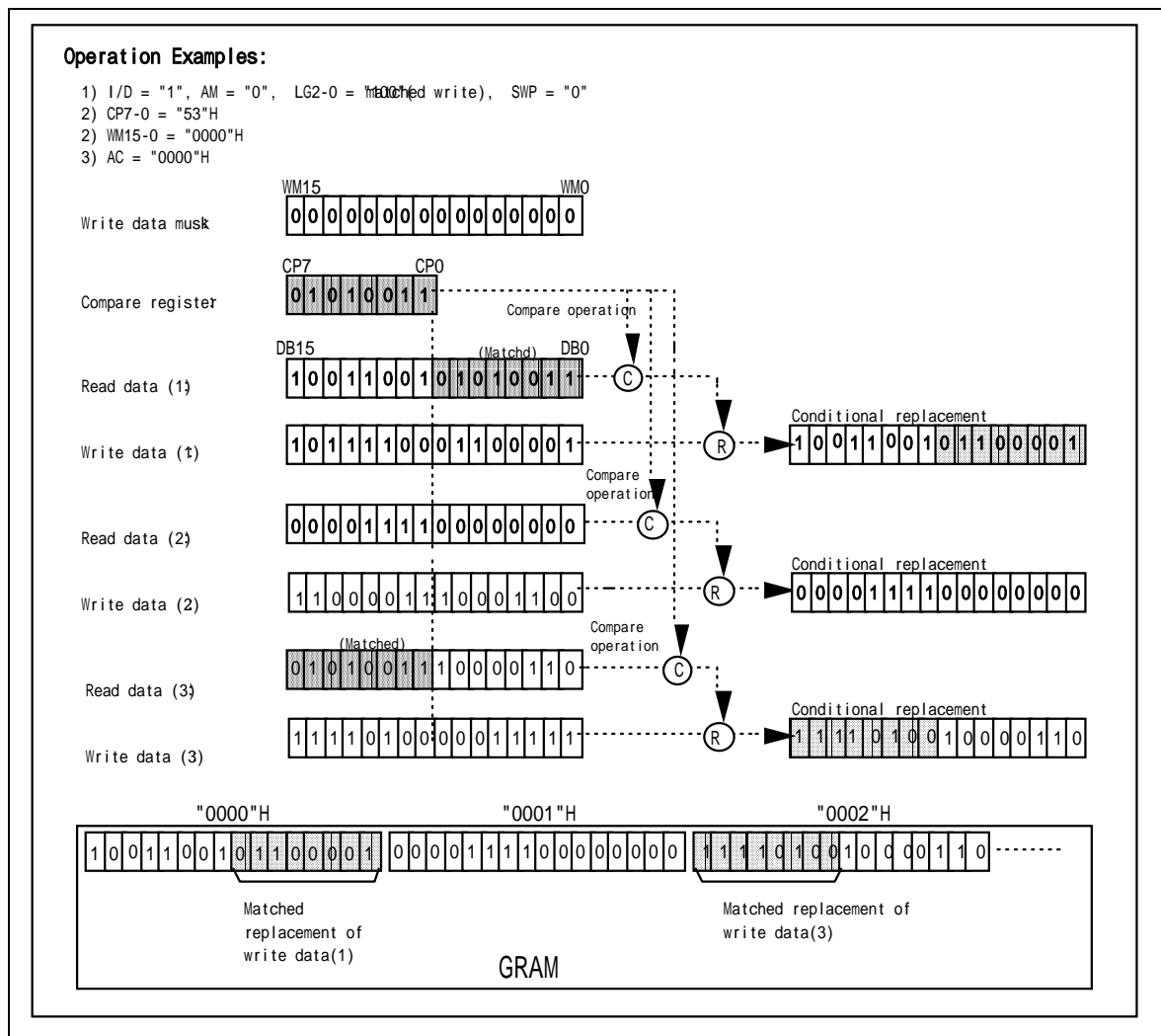


Figure 41 Writing Operation of Read/Write Mode 3

8. Read/Write mode 4: AM = 1, LG2-0 = 110/111

This mode is used when the data is vertically written by comparing the original data and the set value of compare register (CP7-0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the comparison satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD\* low level) as write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) and write-data mask function (WM15-0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256 and automatically jumps to the upper right (I/D=1) or left (I/D=0) counter edge by I/D bits after it has reached the bottom edges of the GRAM.

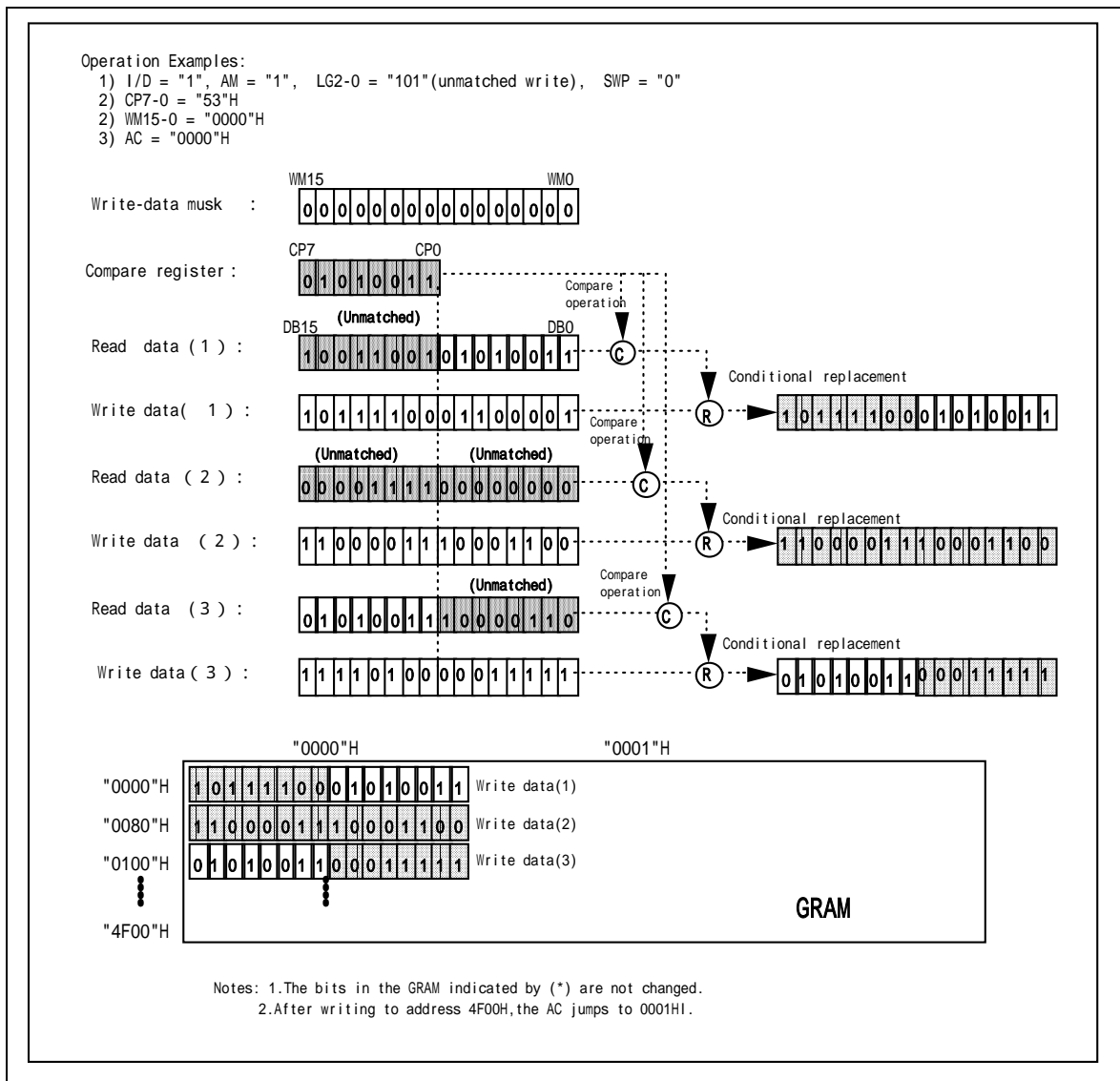


Figure 42 Writing Operation of Read/Write Mode 4

### Grayscale Palette

The HD66762 incorporates a grayscale palette to simultaneously display 256 of the 4,096 possible colors.

The R and G grayscales consist of eight four-bit palettes, and the B grayscale consists of four four-bit palettes. The 16-stage grayscale levels can be selected from the four-bit palette data.

For the display data of R and G, the three-bit data in the GRAM written from the microcomputer is used. For the display data of B, the two-bit data in the GRAM is used.

In this palette, a pulse-width control system (PWM) is used to eliminate flicker in the LCD display. The time over which the LCDs are switched on is adjusted according to the level and grayscales are displayed so that flicker is reduced and grayscales are clearly displayed.

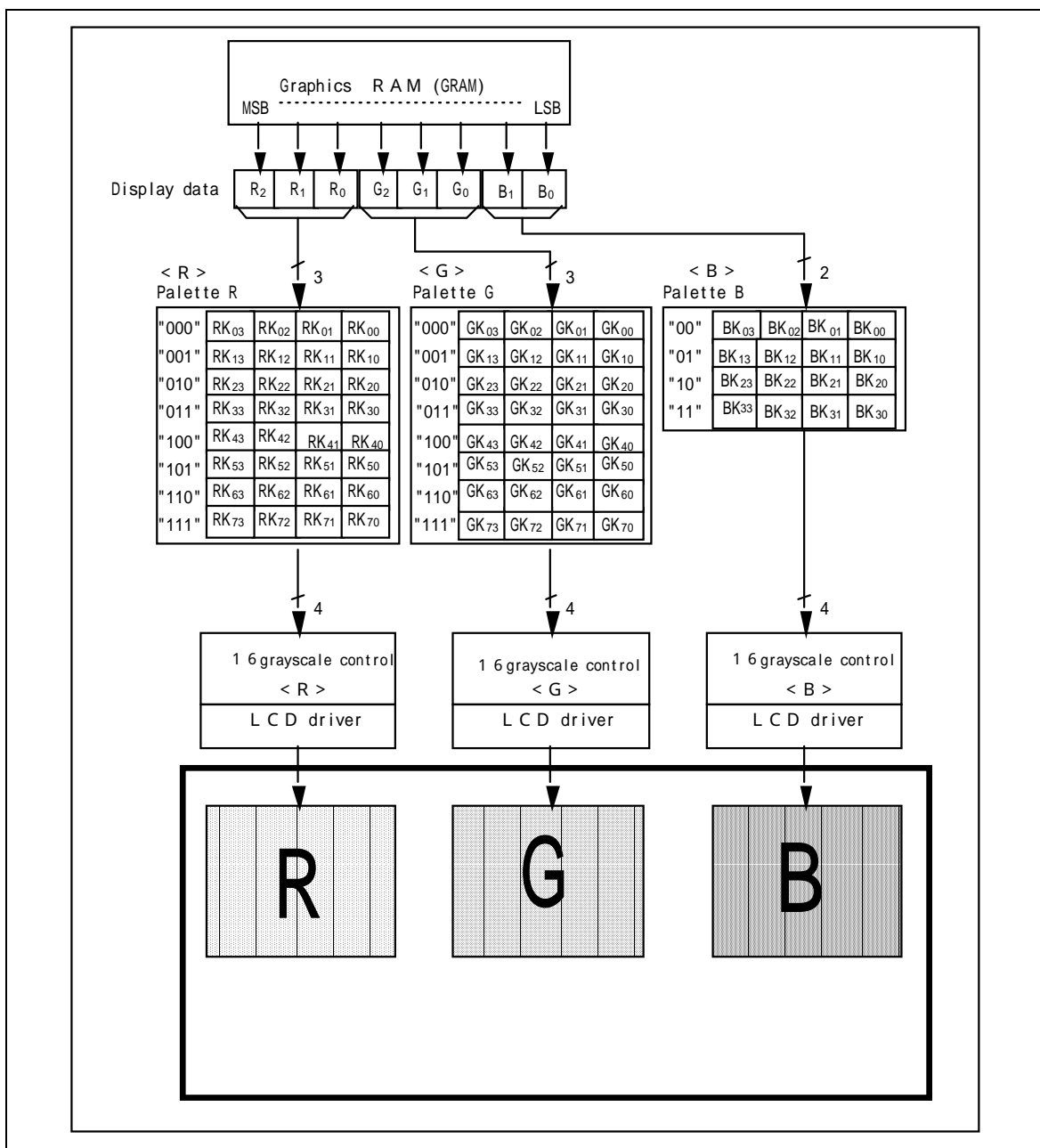


Figure 43 Grayscale Palette Control

### Grayscale Palette Table

The grayscale register that is set for each palette register (RK, GK, or BK) can be set to any level. 16-grayscale lighting levels can be set according to palette values (0000 to 1111).

**Table 31 Grayscale Control Level**

Palette Register Value (RK, GK, or BK)				Grayscale Control Level
0	0	0	0	Unlit level <sup>*1</sup>
0	0	0	1	2/16 level
0	0	1	0	3/16 level
0	0	1	1	4/16 level
0	1	0	0	5/16 level
0	1	0	1	6/16 level
0	1	1	0	7/16 level
0	1	1	1	8/16 level
1	0	0	0	9/16 level
1	0	0	1	10/16 level
1	0	1	0	11/16 level
1	0	1	1	12/16 level
1	1	0	0	13/16 level
1	1	0	1	14/16 level
1	1	1	0	15/16 level
1	1	1	1	All-lit level <sup>*2</sup>

Notes: 1. The unlit level corresponds to a black display when a normally-black color-LCD panel is used, and a white display when a normally-white color-LCD panel is used.

2. The all-lit level corresponds to a white display when a normally-black color-LCD panel is used, and a black display when a normally-white color-LCD panel is used.

## Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66762 in the sleep mode, where the device stops all internal display operations, thus reducing current consumption. Specifically, LCD operation is completely halted. Here, all the SEG (SEG1 to SEG384) and COM (COM1 to COM136) pins output the GND level, resulting in no display. If the AP1-0 bits in the power control register are set to 00 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

**Table 32 Comparison of Sleep Mode and Standby Mode**

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)
LCD control	Turned off	Turned off
R-C oscillation circuit	Operates normally	Operation stopped

## Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66762 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, all the SEG (SEG1 to SEG384) and COM (COM1 to COM136) pins for the time-sharing drive output the GND level, resulting in no display. If the AP1-0 bits are set to 00 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than the start-oscillation instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to 0.

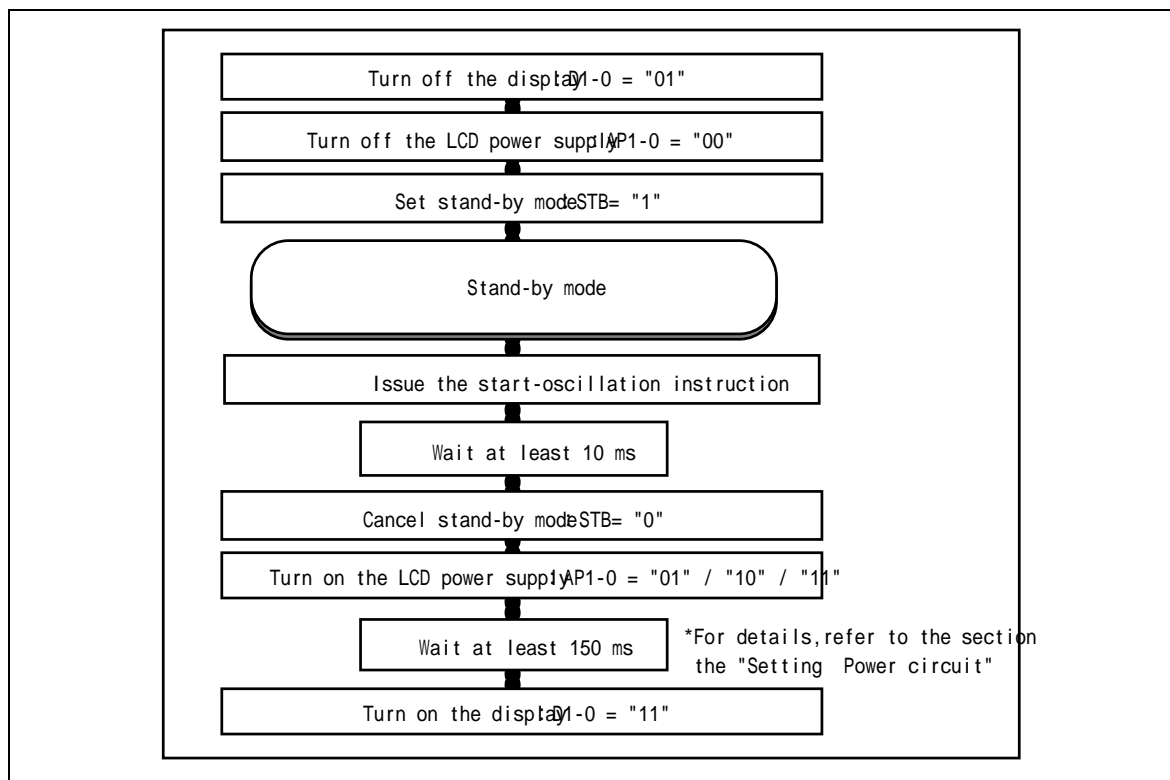


Figure 44 Procedure for Setting and Canceling Standby Mode

### Power-on/off Sequence

To prevent pulse lighting of LCD screens at power-on/off, the power-on/off sequence is activated as shown below. However, since the sequence depends on LCD materials to be used, confirm the conditions by using your own system.

#### Power-on Sequence

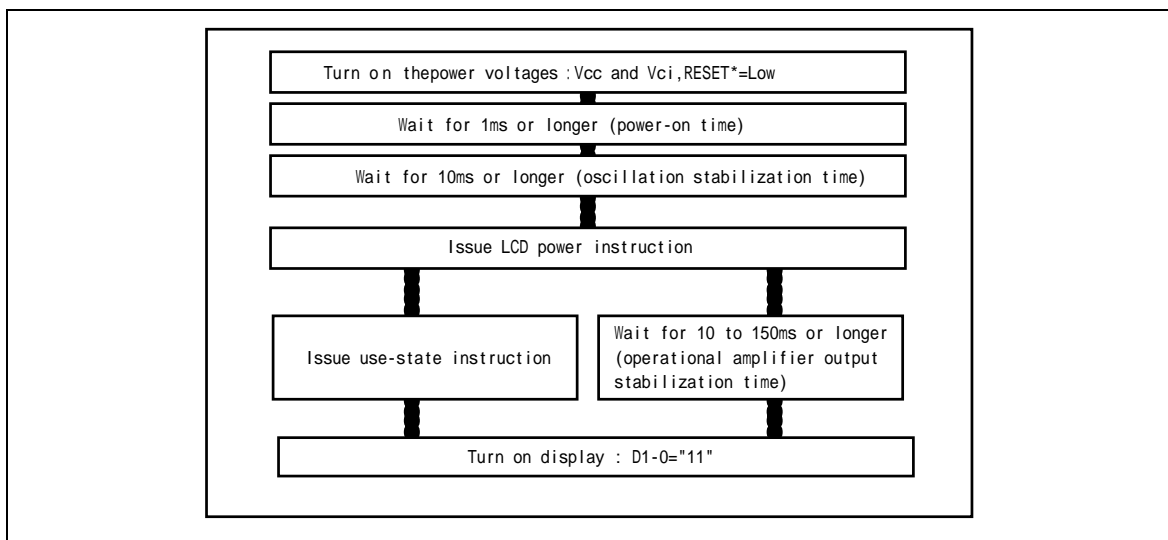


Figure 45 Power-on Sequence

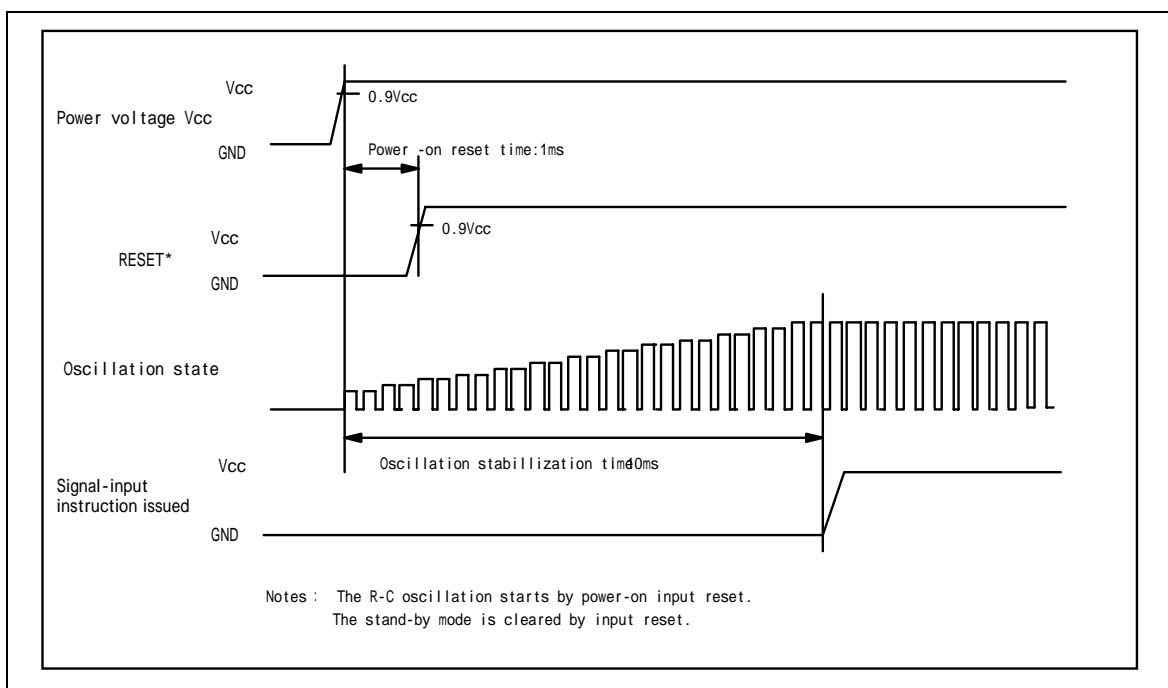
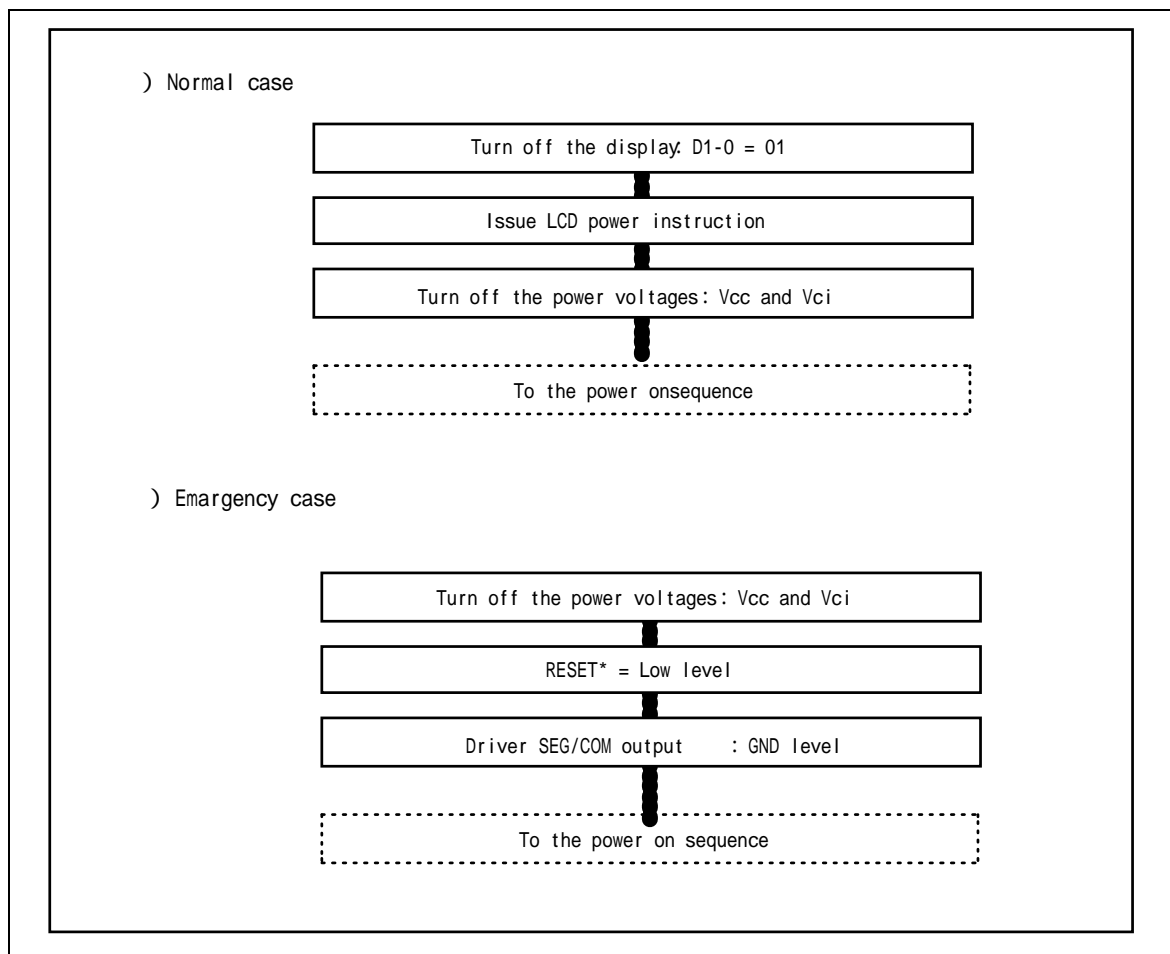


Figure 46 Power-on Timing

**Power-off Sequence****Figure 47 Power-off Sequence**

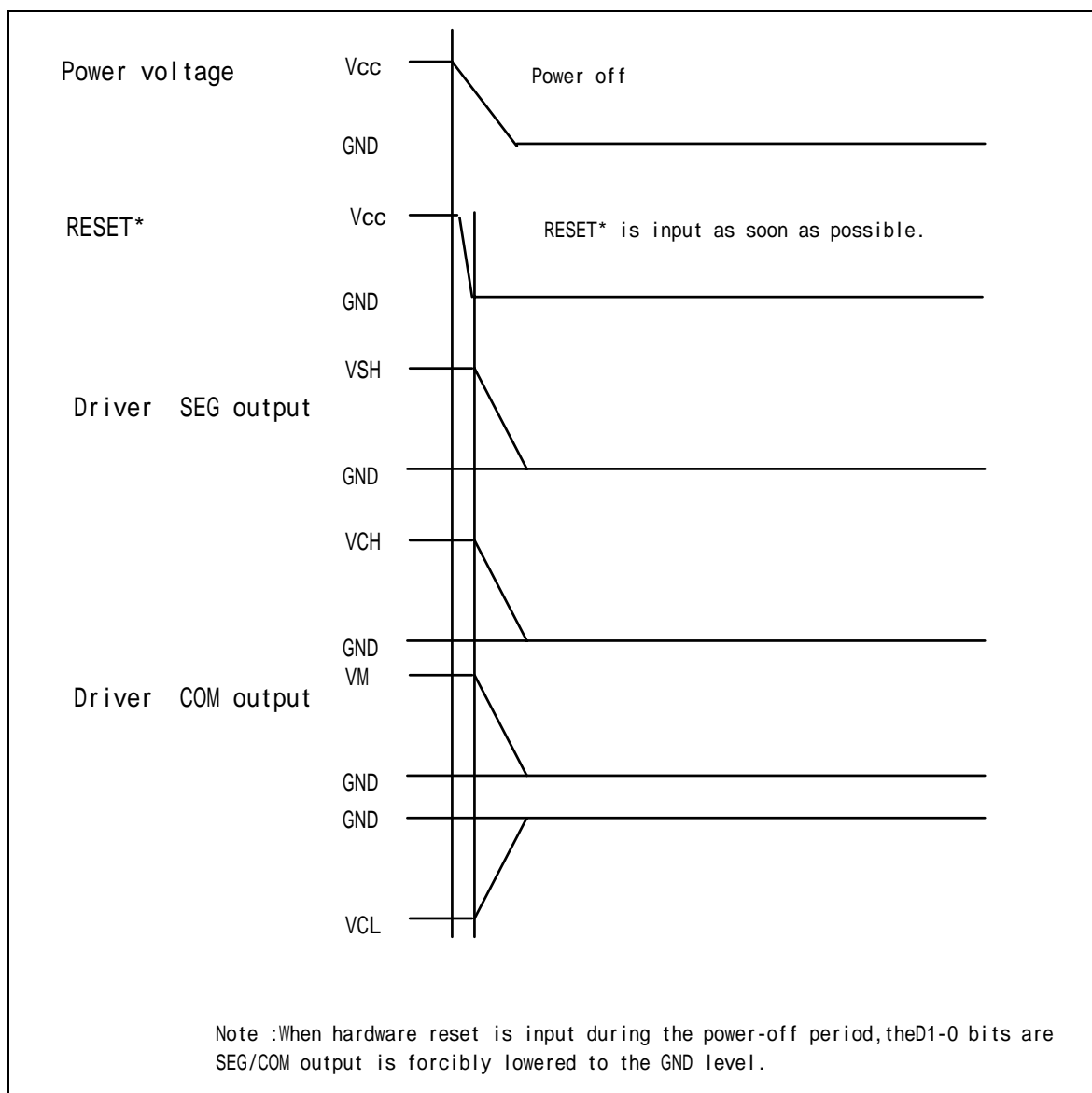


Figure 48 Power-off Timing

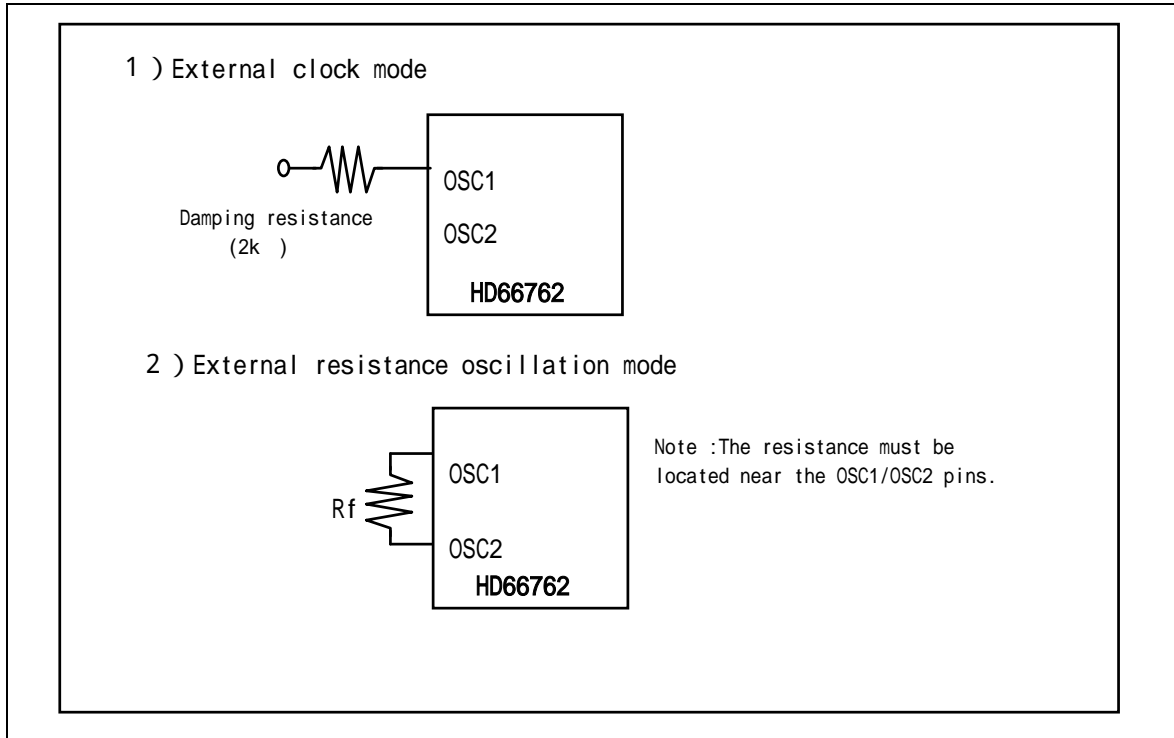
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# HD66762

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## Oscillation Circuit

The HD66762 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If  $R_f$  is increased or power supply voltage is decrease, the oscillation frequency decreases. For the relationship between  $R_f$  resistor value and oscillation frequency, see the Electric Characteristics Notes section.



**Figure 49 Oscillation Circuits**

The relationship between the SEG and COM output levels is as shown in the following figure. While the display is off, SEG and COM outputs go to GND level.

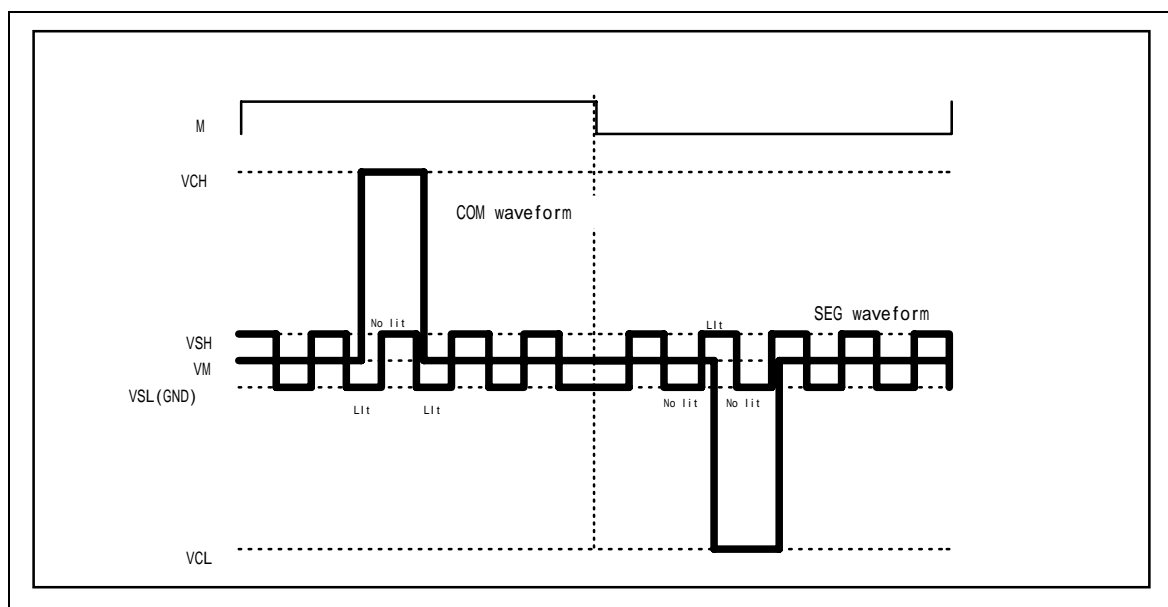


Figure 50 Relationship with SEG/COM Output Level

### Frame-Frequency Adjustment Function

The HD66762 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD drive as the oscillation frequency is always same. When the display duty is changed, the frame frequency can be adjusted to be the same.

If the oscillation frequency is set to high, an animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching, for an animated display, etc. is required, the frame frequency can be set high.

### Relationship between LCD Drive Duty and Frame Frequency

The relationship between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the retrace-line period bit (RTN) and in the operation clock division bit (DIV) by the instruction.

(Formula for the frame frequency)

$$\text{Frame frequency} = \frac{f_{osc}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times 1/\text{duty cycle}} \quad [\text{Hz}]$$

f<sub>osc</sub>: R-C oscillation frequency  
 Duty: drive duty (NL bit)  
 Division ratio: DIV bit  
 Clock cycles per raster-row: (RTN + 17) clock cycles

**Example Calculation 1 To set the maximum frame frequency to 60 Hz**

Display duty: 1/136

Retrace-line period: 0 clock (RTN3-0 = "0000")

Operation clock division ratio: 1 division

$$f_{osc} = 60 \text{ Hz} \times (0 + 17) \text{ clock} \times 1 \text{ division} \times 136 \text{ lines} = 139 \text{ (kHz)}$$

In this case, the CR oscillation frequency becomes 139 kHz. The external resistance value of the CR oscillator must be adjusted to be 139 kHz. The display duty can be changed by the partial display, etc. and the frame frequency can be the same by setting the RNT bit and DIV bit to achieve the following.

Partial

Display duty: 1/40

Retrace-line period: 1 clock (RTN3-0 = "0010")

Operation clock division ratio: 3 division

$$\text{Frame frequency} = 139 \text{ kHz} / ((2 + 17) \text{ clock} \times 3 \text{ division} \times 40 \text{ lines}) = 61.0 \text{ (Hz)}$$

**Example Calculation 2 Switching the frame frequency to suit animation/static image display**

(Animation display)

Frame frequency: 90 Hz

Display duty: 1/136

Retrace-line period: 0 clock (RTN3-0 = "0000")

Operation clock division ratio: 1 division

$$f_{osc} = 90 \text{ Hz} \times (0 + 17) \text{ clock} \times 1 \text{ division} \times 136 \text{ lines} = 208 \text{ (kHz)}$$

(Static image display)

Frame frequency: 60 Hz

Display duty: 1/136

Retrace-line period: 0 clock (RTN3-0 = "1000")

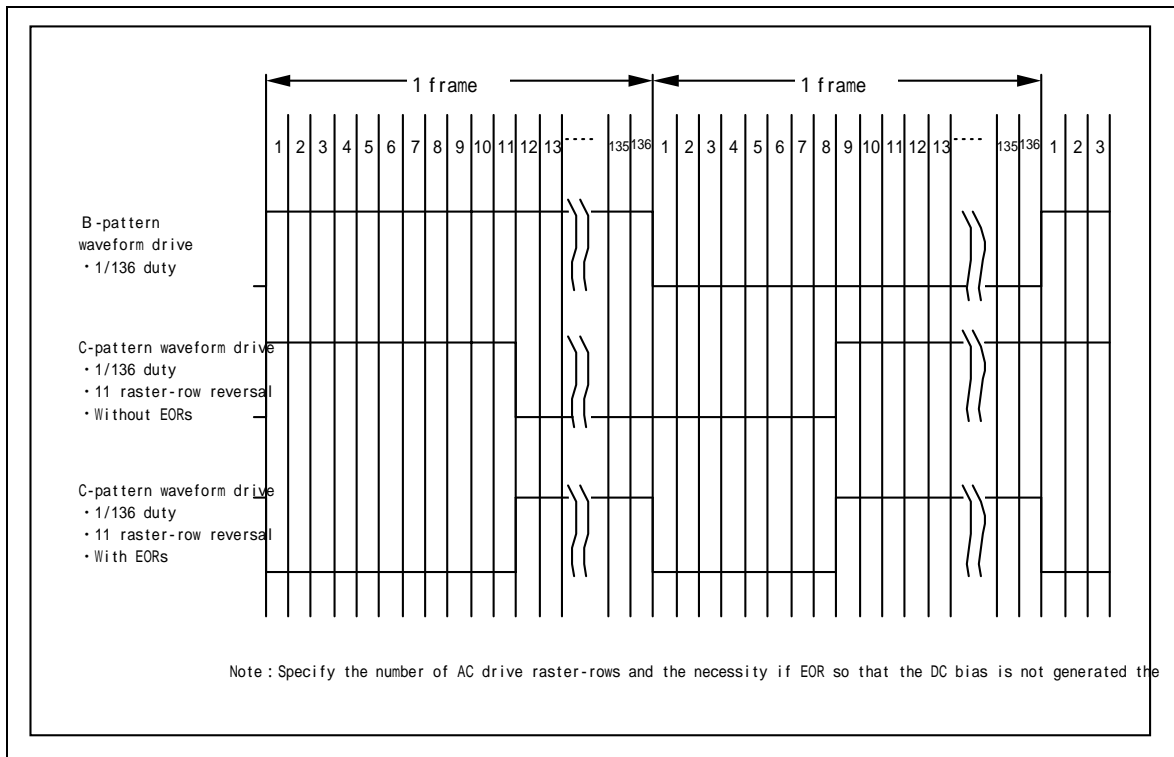
Operation clock division ratio: 1 division

$$\text{Frame frequency} = 208 \text{ kHz} / ((8 + 17) \text{ clock} \times 1 \text{ division} \times 136 \text{ lines}) = 61.2 \text{ (Hz)}$$

**n-raster-row Reversed AC Drive**

The HD66762 supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 64 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as cross-talk at high-duty driving of more than 1/64 duty, the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality.

Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.

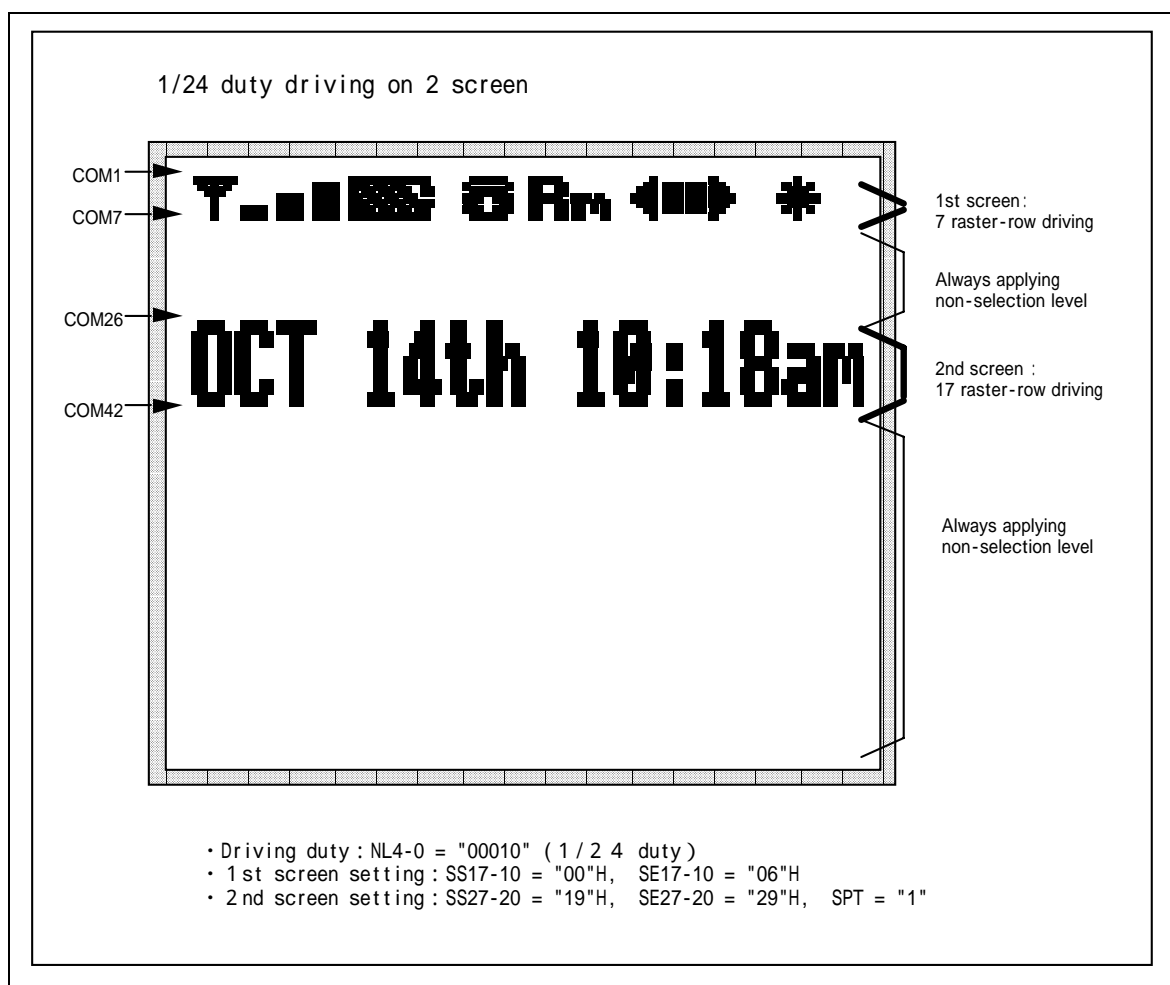


**Figure 51 Example of an AC Signal under n-raster-row Reversed AC Drive**

### Screen-division Driving Function

The HD66762 can select and drive two screens at any position with the screen-driving position registers (R14h and R15h). Any two screens required for display are selectively driven and a duty ratio is lowered by LCD-driving duty setting (NL4-0), thus reducing LCD-driving voltage and power consumption.

For the 1st division screen, start line (SS17-10) and end line (SE17-10) are specified by the 1st screen-driving position register (R14h). For the 2nd division screen, start line (SS27-20) and end line (SE27-20) are specified by the 2nd screen-driving position register (R15h). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.



**Figure 52** Display example in 2-screen division driving

**Restrictions on the 1st/2nd Screen Driving Position Register Settings**

The following restrictions must be satisfied when setting the start line (SS17-10) and end line (SE17-10) of the 1st screen driving position register (R14h) and the start line (SS27-20) and end line (SE27-20) of the 2nd screen driving position register (R15h) for the HD66762. Note that incorrect display may occur if the restrictions are not satisfied.

**Table 33 Restrictions on the 1st/2nd Screen Driving Position Register Settings**

	<b>1st Screen Driving (SPT = 0)</b>	<b>2nd Screen Driving (SPT = 1)</b>
Register setting	SS17-10 = SE17-0 = "87"H	SS17-10 = SE17-10 < SS27-20 = SE27-20 = "87"H
Display operation	ï Time-sharing driving for COM pins (SS1+1) to (SE1+1) ï Non-selection level driving for others	ï Time-sharing driving for COM pins (SS1+1) to (SE1+1) and (SS2+1) to (SE2+1) ï Non-selection level driving for others

- Notes:
1. When the total line count in screen division driving settings is less than the duty setting, non-selection level driving is performed without the screen division driving setting range.
  2. When the total line count in screen division driving settings is larger than the duty setting, the start line, the duty-setting line, and the lines between them are displayed and non-selection level driving is performed for other lines.
  3. For the 1st screen driving, the SS27-20 and SE27-20 settings are ignored.



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## HD66762

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- Notes:
1. Generate an output voltage (VOUT) from step-up circuit 1 within the range from 4.5 to 6.0 V.
  2. Do not allow the output voltage (VCH) from step-up circuit 2 to exceed 22 V.
  3. Do not allow the output voltage (Vci2) to exceed VOUT level.
  4. When a capacitor with polarity is used, be sure that an inverted voltage is not applied to it in any state of the system.
  5. Vci1 is used as both the reference voltage input and power supply in the step-up circuit. Keep sufficient LCD drive current.
  6. Following condensers can be used;
    - 6.3V : VREFM, VciOUT, C11, C12, VOUT, BIASC, Vci2, C21, C22, C23, VSH, VM
    - 25V : VCH, VCL, CE

### LCD Drive Voltage

The required voltage can be calculated by applying the following expressions.

Drive voltages are standard; generate a voltage to suit the panel to be used .

$$VSH-VM, VM-VSL = \frac{1}{2} \sqrt{\frac{2\sqrt{N}}{\sqrt{N}}} \times V_{th}$$

Vth: slethord

$$VCH-VM, VM-VCL = \frac{1}{2} \sqrt{\frac{2N\sqrt{N}}{\sqrt{N}-1}} \times V_{th}$$

N : display duty

### LCD Drive Bias

An optimal bias can be calculated by applying the following expression. The value that has been calculated is theoretically optimal. If a lower bias value than the optimal value is used to drive the LCD, contrast may be reduced depending on lighting conditions. However, the power consumption can be reduced by lowering the drive voltage. Adjust the value according to the system to be used.

$$\text{Bias value} = \frac{1}{\sqrt{N}}$$

### How to determine the VCH voltage

$$VCH = N_B \times N_{D2} \times VSH$$

$N_B$  : Bias ratio

$N_{D2}$  : Step-up factor of the step-up circuit 2

**Contrast adjustment**

$R_B$  : Contrast resistance (0.004R to 0.512R)

$$V_{SH} = V_{REFM} \times 2R / (R_b + 2R)$$

**Table 34 Contrast control**

CT6	CT5	CT4	CT3	CT2	CT1	CT0	Resistance of Rb
0	0	0	0	0	0	0	1.016R
0	0	0	0	0	0	1	1.008R
0	0	0	0	0	1	0	1.000R
0	0	0	0	0	1	1	0.992R
0	0	0	0	1	0	0	0.984R
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	0.008R
1	1	1	1	1	1	1	0.000R

## How to determine the power setting value

### 1. Determine LCD drive bias

Determine LCD drive bias first. LCD drive bias is theoretically (1/SQRT (display duty)) optimal; however, the total drive voltage can be reduced by lowering bias ratio. Consider the display quality, the drive voltage and the current consumption.

### 2. Determine VOUT voltage

Determine factor of Vci1 regulator and step-up factor so as to set output voltage, VOUT of step-up circuit 1 4.5 to 6.0V, setting input voltage Vci2 of step-up circuit 2 more than +0.5V. Since the entire electric power for driving LCD is supplied from step-up circuit, subsequent voltage fall need to be considered.

### 3. Segment drive voltage calculation

Segment output drive voltage is calculated by the following expression.

$$V_{seg} = \sqrt{\frac{2 \times B}{(B - 1)}} \times V_{th}$$

B : LCDdrive bias ratio  
Vth : LCD threshold voltage

### 4. Common drive voltage calculation

Common output drive voltage is calculated by the following expression.

$$V_{com} = \frac{V_{seg}}{2} \times (B + 1)$$

B : LCD drive bias ratio

### 5. Determine input voltage of step-up circuit 2

Determine input voltage of step-up circuit 2. This voltage is determined by dividing Vcom voltage by step-up factor ; lower factors are used for low current consumption. Vci2 voltage need to be less than VOUT voltage (4.5 to 6.0 V).

**Example of register setting on power supply**

Examples of register setting values on power supply are described below.

**Example 1** : 1/136 duty ratio,  $V_{cc} = V_{REFL} = 3.0V$ , 1/10 bias

BS3-0 = H'8 : bias adjustment 1.375 times  
 BT2-0 = H'4 : set-up circuit 1 2 times set-up circuit 2 4 times  
 BT3 = H'1 : operate voltage inverting circuit  
 DC2-0 = H'6 : set-up circuit 1 frequency 15 clocks set-up circuit 2 frequency 60 clocks TBD  
 AP1-0 = H'1 : low fixed current in the amplifier  
  
 VC2-0 = H'0 :  $V_{ci1} = 0.92 \times V_{cc} = 2.75V$   
 VR2-0 = H'0 :  $V_{REFM} = 1.1 \times V_{REFL}$   
 CT6-0 : appropriate contrast setting values

**Example 2** : 1/136 duty ratio,  $V_{cc} = V_{REFL} = 2.4V$ ,  $V_{ci} = 2.8V$ , 1/10 bias

BS2-0 = H'8 : bias adjustment 1.375 times  
 BT2-0 = H'4 : set-up circuit 1 2 times set-up circuit 2 4 times  
 BT3 = H'1 : operate voltage inverting circuit  
 DC2-0 = H'6 : set-up circuit 1 frequency 15 clocks set-up circuit 2 frequency 60 locks TBD  
 AP1-0 = H'1 : low fixed current in the amplifier  
 VC2-0 = H'4 : internal  $V_{ci1}$  regulator off 2.8V directly supplied to  $V_{ci1}$   
 VR3-0 = H'2 :  $V_{REFM} = 1.4 \times V_{REFL}$   
 CT6-0 : appropriate contrast setting values

**Example 3** : Partial display, 1/24 duty ratio,  $V_{cc} = 2.4V$ ,  $V_{ci} = 2.8V$ , 1/4 bias

BS2-0 = H'0 : bias adjustment 1.25 times  
 BT2-0 = H'0 : set-up circuit 1 2 times set-up circuit 2 2 times  
 BT3 = H'1 : operate voltage inverting circuit  
 DC2-0 = H'6 : set-up circuit 1 frequency 30 clocks set-up circuit 2 frequency 60 clocks TBD  
 AP1-0 = H'1 : low fixed current in the amplifier  
 VC2-0 = H'4 : internal  $V_{ci1}$  regulator off  
 VR3-0 = H'2 :  $V_{REG1} = 1.4 \times V_{REFL}$   
 CT6-0 : appropriate contrast setting values

**HD66762 Power Supply Level Correlation**

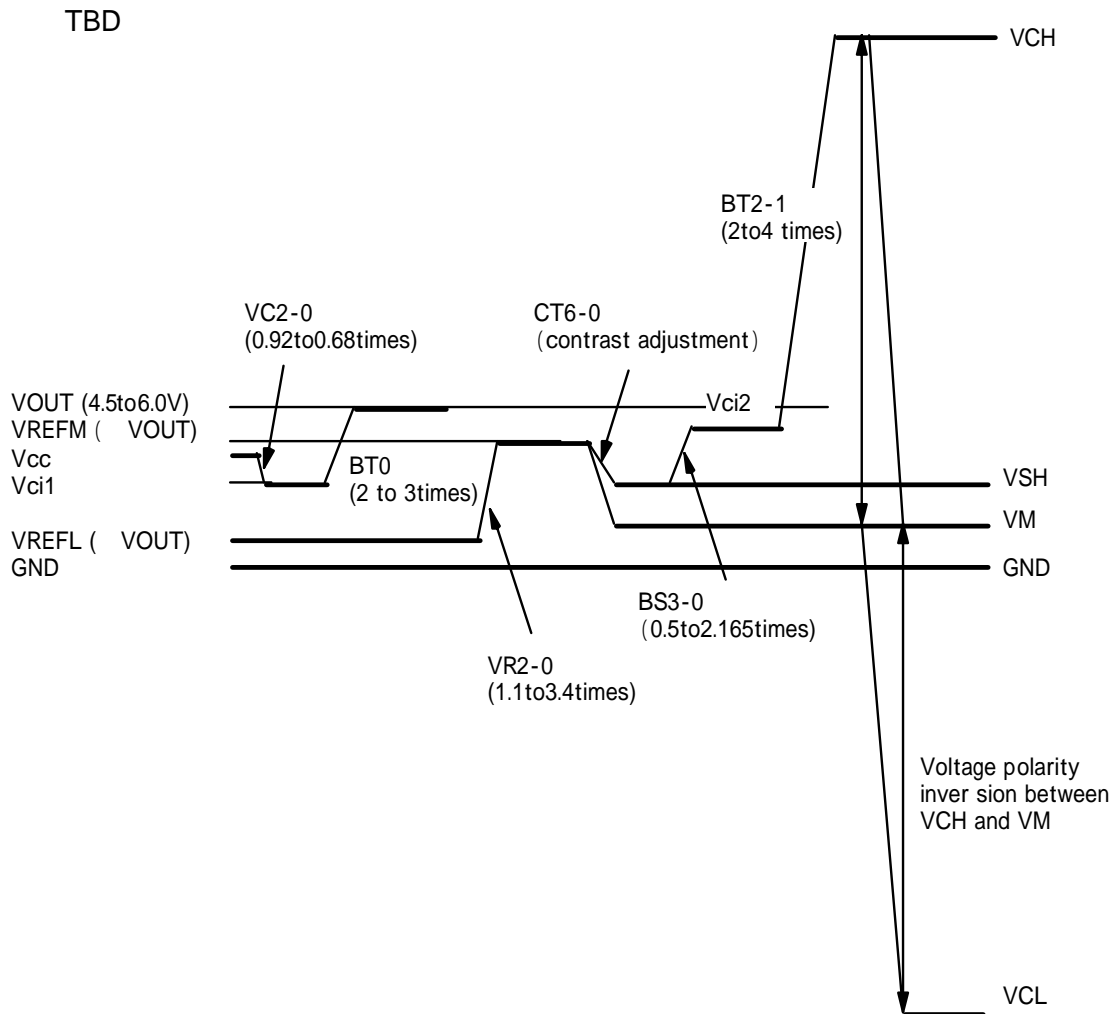
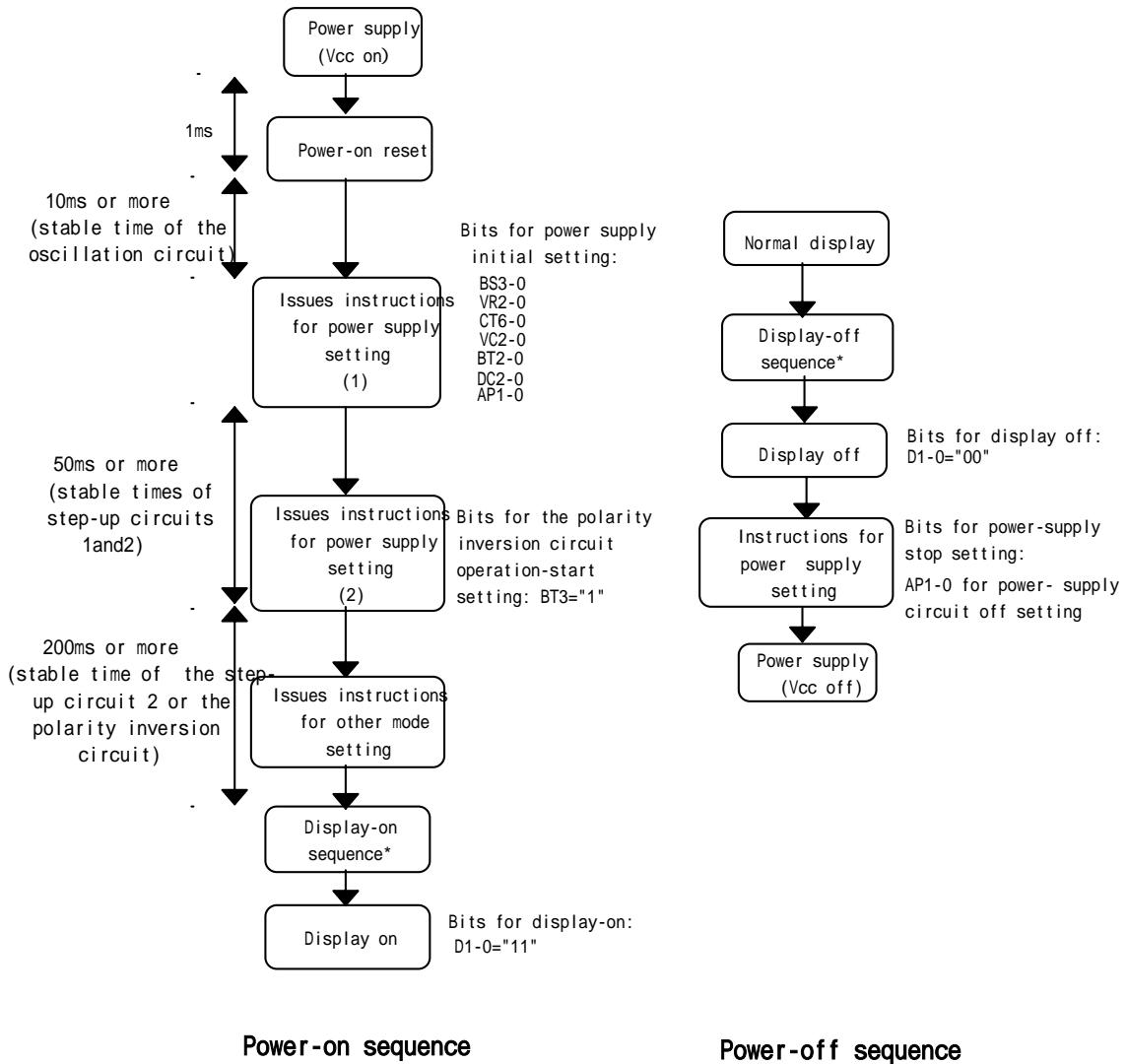


Figure HD66762 Power supply level correlation

### Flow of Power-Supply Setting

Apply the power in a sequence as shown in figure.

The stable times of the oscillation circuit, step-up circuit, and operational amplifier depend on the external resistor or capacitance.



\*Notes: For the display-on/off sequence, refer to the section on Instruction Setting Flow.

### Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	$V_{CC}$	V	-0.3 to +4.6	1, 2
Power supply voltage (2)	$V_{ci1}$	V	-0.3 to +4.6	1, 3
Power supply voltage (3)	$V_{CH} - V_{CL}$	V	-0.3 to +4.4	1, 4
Input voltage	$V_t$	V	-0.3 to $V_{CC} + 0.3$	1
Operating temperature	$T_{opr}$		-40 to +85	1, 5
Storage temperature	$T_{stg}$		-55 to +110	1, 6

- Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.
2.  $V_{CC} > GND$  must be maintained.
  3.  $V_{ci1} > GND$  must be maintained.
  4.  $V_{CH} > GND$  and  $GND > V_{CL}$  must be maintained.
  5. For die and wafer products, specified up to 85 .
  6. This temperature specification applies to the TCP package.

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### DC Characteristics ( $V_{CC} = 1.8$ to $3.6$ V, $V_{CH} - V_{CL} = 10$ to $38$ V, $T_a = -40$ to $+85$ \*<sup>1</sup>)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high	$V_{IH}$	$0.7 V_{CC}$	-	$V_{CC}$	V	$V_{CC} = 1.8$ to $3.6$ V	2, 3
Input low voltage	$V_{IL}$	-0.3	-	$0.15 V_{CC}$	V	$V_{CC} = 1.8$ to $3.6$ V	2, 3
Output high voltage (1) (DB0-15 pins)	$V_{OH1}$	$0.75 V_{CC}$	-	-	V	$I_{OH} = -0.1$ mA	2
Output low voltage (1) (DB0-15 pins)	$V_{OL1}$	-	-	$0.2 V_{CC}$	V	$V_{CC} = 1.8$ to $2.4$ V, $I_{OL} = 0.1$ mA	2
				$0.15 V_{CC}$	V	$V_{CC} = 2.4$ to $3.6$ V, $I_{OL} = 0.1$ mA	2
Driver ON resistance (SEG pins)	$R_{SEG}$	-	0.35	3	k	$\pm I_d = 0.05$ mA, $V_{SH} = 3$ V	4
Driver ON resistance (COM pins)	$R_{COM}$	-	0.90	3	k	$\pm I_d = 0.05$ mA, $V_{CH} - V_{CL} = 40$ V	4
I/O leakage current	$I_{Li}$	-1	-	1	$\mu$ A	$V_{in} = 0$ to $V_{CC}$	5
Current consumption during normal operation ( $V_{CC} - GND$ )	$I_{OP}$	-	370	500	$\mu$ A	R-C oscillation, $V_{CC} = 3.0$ V, $T_a = 25$ , $f_{OSC} = 180$ kHz (1/176 duty) Writing to RAM: All "1"	6, 7
Current consumption during standby mode ( $V_{CC} - GND$ )	$I_{ST}$	-	0.1	5	$\mu$ A	$V_{CC} = 3.0$ V, $T_a = 25$	6, 7

Note: For the numbered notes, refer to the Electrical Characteristics Notes section tables.

### AC Characteristics ( $V_{CC} = 1.8$ to $3.6$ V, $T_a = -40$ to $+85$ \*<sup>1</sup>)

#### Clock Characteristics ( $V_{CC} = 1.8$ to $3.6$ V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	fcp	140	210	315	kHz	$V_{CC} = 1.8$ to $3.6$ V	8
External clock duty ratio	Duty	45	50	55	%	$V_{CC} = 1.8$ to $3.6$ V	8
External clock rise time	trcp	-	-	0.2	$\mu$ s	$V_{CC} = 1.8$ to $3.6$ V	8
External clock fall time	tfcp	-	-	0.2	$\mu$ s	$V_{CC} = 1.8$ to $3.6$ V	8
R-C oscillation clock	$f_{OSC}$	168	210	252	kHz	$R_f = 220$ k $V_{CC} = 3$ V	9

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

**68-system Bus Interface Timing Characteristics**
**<Normal write mode (HWM = 0), Vcc = 1.8 to 2.4 V>**

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	$t_{CYCE}$	600	-	-	ns	Figure 58
	Read	$t_{CYCE}$	800	-	-		
Enable high-level pulse width	Write	$PW_{EH}$	90	-	-	ns	Figure 58
	Read	$PW_{EH}$	350	-	-		
Enable low-level pulse width	Write	$PW_{EL}$	300	-	-	ns	Figure 58
	Read	$PW_{EL}$	400	-	-		
Enable rise/fall time		$t_{Er}, t_{Ef}$	-	-	25	ns	Figure 58
Setup time (RS, R/W to E, CS*)		$t_{ASE}$	10	-	-	ns	Figure 58
Address hold time		$t_{AHE}$	5	-	-	ns	Figure 58
Write data setup time		$t_{DSWE}$	60	-	-	ns	Figure 58
Write data hold time		$t_{HE}$	15	-	-	ns	Figure 58
Read data delay time		$t_{DDRE}$	-	-	200	ns	Figure 58
Read data hold time		$t_{DHRE}$	5	-	-	ns	Figure 58

**<High-speed write mode (HWM = 1), Vcc = 1.8 to 2.4 V>**

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	$t_{CYCE}$	200	-	-	ns	Figure 58
	Read	$t_{CYCE}$	800	-	-		
Enable high-level pulse width	Write	$PW_{EH}$	90	-	-	ns	Figure 58
	Read	$PW_{EH}$	350	-	-		
Enable low-level pulse width	Write	$PW_{EL}$	90	-	-	ns	Figure 58
	Read	$PW_{EL}$	400	-	-		
Enable rise/fall time		$t_{Er}, t_{Ef}$	-	-	25	ns	Figure 58
Setup time (RS, R/W to E, CS*)		$t_{ASE}$	10	-	-	ns	Figure 58
Address hold time		$t_{AHE}$	5	-	-	ns	Figure 58
Write data setup time		$t_{DSWE}$	60	-	-	ns	Figure 58
Write data hold time		$t_{HE}$	15	-	-	ns	Figure 58
Read data delay time		$t_{DDRE}$	-	-	200	ns	Figure 58
Read data hold time		$t_{DHRE}$	5	-	-	ns	Figure 58

## HD66762

<Normal write mode (HWM = 0), Vcc = 2.4 to 3.6 V>

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t <sub>CYCE</sub>	250	-	-	ns	Figure 58
	Read	t <sub>CYCE</sub>	500	-	-		
Enable high-level pulse width	Write	PW <sub>EH</sub>	40	-	-	ns	Figure 58
	Read	PW <sub>EH</sub>	250	-	-		
Enable low-level pulse width	Write	PW <sub>EL</sub>	100	-	-	ns	Figure 58
	Read	PW <sub>EL</sub>	200	-	-		
Enable rise/fall time		t <sub>Er</sub> , t <sub>Ef</sub>	-	-	25	ns	Figure 58
Setup time (RS, R/W to E, CS*)		t <sub>ASE</sub>	10	-	-	ns	Figure 58
Address hold time		t <sub>AHE</sub>	5	-	-	ns	Figure 58
Write data setup time		t <sub>DSWE</sub>	60	-	-	ns	Figure 58
Write data hold time		t <sub>HE</sub>	15	-	-	ns	Figure 58
Read data delay time		t <sub>DDRE</sub>	-	-	200	ns	Figure 58
Read data hold time		t <sub>DHRE</sub>	5	-	-	ns	Figure 58

<High-speed write mode (HWM = 1), Vcc = 2.4 to 3.6 V>

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t <sub>CYCE</sub>	100	-	-	ns	Figure 58
	Read	t <sub>CYCE</sub>	500	-	-		
Enable high-level pulse width	Write	PW <sub>EH</sub>	40	-	-	ns	Figure 58
	Read	PW <sub>EH</sub>	250	-	-		
Enable low-level pulse width	Write	PW <sub>EL</sub>	50	-	-	ns	Figure 58
	Read	PW <sub>EL</sub>	200	-	-		
Enable rise/fall time		t <sub>Er</sub> , t <sub>Ef</sub>	-	-	25	ns	Figure 58
Setup time (RS, R/W to E, CS*)		t <sub>ASE</sub>	10	-	-	ns	Figure 58
Address hold time		t <sub>AHE</sub>	5	-	-	ns	Figure 58
Write data setup time		t <sub>DSWE</sub>	60	-	-	ns	Figure 58
Write data hold time		t <sub>HE</sub>	15	-	-	ns	Figure 58
Read data delay time		t <sub>DDRE</sub>	-	-	200	ns	Figure 58
Read data hold time		t <sub>DHRE</sub>	5	-	-	ns	Figure 58

**80-system Bus Interface Timing Characteristics**
**<Normal write mode (HWM = 0), V<sub>CC</sub> = 1.8 to 2.4 V>**

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write $t_{CYCW}$	600	-	-	ns	Figure 59
	Read $t_{CYCR}$	800	-	-	ns	Figure 59
Write low-level pulse width	$PW_{LW}$	90	-	-	ns	Figure 59
Read low-level pulse width	$PW_{LR}$	350	-	-	ns	Figure 59
Write high-level pulse width	$PW_{HW}$	300	-	-	ns	Figure 59
Read high-level pulse width	$PW_{HR}$	400	-	-	ns	Figure 59
Write/Read rise/fall time	$t_{WRr},$ $t_{WRf}$	-	-	25	ns	Figure 59
Setup time (RS to CS*, WR*, RD*)	$t_{AS}$	10	-	-	ns	Figure 59
Address hold time	$t_{AH}$	5	-	-	ns	Figure 59
Write data setup time	$t_{DSW}$	60	-	-	ns	Figure 59
Write data hold time	$t_H$	15	-	-	ns	Figure 59
Read data delay time	$t_{DDR}$	-	-	200	ns	Figure 59
Read data hold time	$t_{DHR}$	5	-	-	ns	Figure 59

**<High-speed write mode (HWM = 0), V<sub>CC</sub> = 1.8 to 2.4 V>**

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write $t_{CYCW}$	200	-	-	ns	Figure 59
	Read $t_{CYCR}$	800	-	-	ns	Figure 59
Write low-level pulse width	$PW_{LW}$	90	-	-	ns	Figure 59
Read low-level pulse width	$PW_{LR}$	350	-	-	ns	Figure 59
Write high-level pulse width	$PW_{HW}$	90	-	-	ns	Figure 59
Read high-level pulse width	$PW_{HR}$	400	-	-	ns	Figure 59
Write/Read rise/fall time	$t_{WRr},$ $t_{WRf}$	-	-	25	ns	Figure 59
Setup time (RS to CS*, WR*, RD*)	$t_{AS}$	10	-	-	ns	Figure 59
Address hold time	$t_{AH}$	5	-	-	ns	Figure 59
Write data setup time	$t_{DSW}$	60	-	-	ns	Figure 59
Write data hold time	$t_H$	15	-	-	ns	Figure 59
Read data delay time	$t_{DDR}$	-	-	200	ns	Figure 59
Read data hold time	$t_{DHR}$	5	-	-	ns	Figure 59

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<Normal write mode (HWM = 0), Vcc = 2.4 to 3.6 V>

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write $t_{CYCW}$	300	-	-	ns	Figure 59
	Read $t_{CYCR}$	500	-	-	ns	Figure 59
Write low-level pulse width	$PW_{LW}$	40	-	-	ns	Figure 59
Read low-level pulse width	$PW_{LR}$	250	-	-	ns	Figure 59
Write high-level pulse width	$PW_{HW}$	100	-	-	ns	Figure 59
Read high-level pulse width	$PW_{HR}$	200	-	-	ns	Figure 59
Write/Read rise/fall time	$t_{WRr, WRf}$	-	-	25	ns	Figure 59
Setup time (RS to CS*, WR*, RD*)	$t_{AS}$	10	-	-	ns	Figure 59
Address hold time	$t_{AH}$	5	-	-	ns	Figure 59
Write data setup time	$t_{DSW}$	60	-	-	ns	Figure 59
Write data hold time	$t_H$	15	-	-	ns	Figure 59
Read data delay time	$t_{DDR}$	-	-	200	ns	Figure 59
Read data hold time	$t_{DHR}$	5	-	-	ns	Figure 59

<High-speed write mode (HWM = 1), Vcc = 2.4 to 3.6 V>

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write $t_{CYCW}$	100	-	-	ns	Figure 59
	Read $t_{CYCR}$	500	-	-	ns	Figure 59
Write low-level pulse width	$PW_{LW}$	40	-	-	ns	Figure 59
Read low-level pulse width	$PW_{LR}$	250	-	-	ns	Figure 59
Write high-level pulse width	$PW_{HW}$	40	-	-	ns	Figure 59
Read high-level pulse width	$PW_{HR}$	200	-	-	ns	Figure 59
Write/Read rise/fall time	$t_{WRr, WRf}$	-	-	25	ns	Figure 59
Setup time (RS to CS*, WR*, RD*)	$t_{AS}$	10	-	-	ns	Figure 59
Address hold time	$t_{AH}$	5	-	-	ns	Figure 59
Write data setup time	$t_{DSW}$	60	-	-	ns	Figure 59
Write data hold time	$t_H$	15	-	-	ns	Figure 59
Read data delay time	$t_{DDR}$	-	-	200	ns	Figure 59
Read data hold time	$t_{DHR}$	5	-	-	ns	Figure 59

**Clock Synchronized Serial Interface Timing Characteristics**
**(V<sub>CC</sub> = 1.8 to 2.4 V)**

<b>Item</b>		<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>	<b>Test Condition</b>
Serial clock cycle time	At write (receive)	t <sub>SCYC</sub>	0.125	-	20	us	Figure 60
	At read (send)	t <sub>SCYC</sub>	0.55	-	20	us	Figure 60
Serial clock high-level pulse width	At write (receive)	t <sub>SCH</sub>	50	-	-	ns	Figure 60
	At read (send)	t <sub>SCH</sub>	250	-	-	ns	Figure 60
Serial clock low-level pulse width	At write (receive)	t <sub>SCL</sub>	50	-	-	ns	Figure 60
	At read (send)	t <sub>SCL</sub>	250	-	-	ns	Figure 60
Serial clock rise/fall time		t <sub>SCr</sub> , t <sub>SCf</sub>	-	-	20	ns	Figure 60
CS* Setup time		t <sub>CSU</sub>	20	-	-	ns	Figure 60
CS* hold time		t <sub>CH</sub>	260	-	-	ns	Figure 60
Serial input data setup time		t <sub>SISU</sub>	30	-	-	ns	Figure 60
Serial input data hold time		t <sub>SIH</sub>	30	-	-	ns	Figure 60
Serial output data delay time		t <sub>SOD</sub>	-	-	230	ns	Figure 60
Serial output data hold time		t <sub>SOH</sub>	5	-	-	ns	Figure 60

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(V<sub>CC</sub> = 2.4 to 3.6 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	At write (receive)	t <sub>SCYC</sub>	0.1	-	20	us	Figure 60
	At read (send)	t <sub>SCYC</sub>	0.35	-	20	us	Figure 60
Serial clock high-level pulse width	At write (receive)	t <sub>SCH</sub>	40	-	-	ns	Figure 60
	At read (send)	t <sub>SCH</sub>	170	-	-	ns	Figure 60
Serial clock low-level pulse width	At write (receive)	t <sub>SCL</sub>	40	-	-	ns	Figure 60
	At read (send)	t <sub>SCL</sub>	170	-	-	ns	Figure 60
Serial clock rise/fall time		t <sub>SCr</sub> , t <sub>SCf</sub>	-	-	20	ns	Figure 60
CS* Setup time		t <sub>CSU</sub>	20	-	-	ns	Figure 60
CS* hold time		t <sub>CH</sub>	160	-	-	ns	Figure 60
Serial input data setup time		t <sub>SISU</sub>	30	-	-	ns	Figure 60
Serial input data hold time		t <sub>SIH</sub>	30	-	-	ns	Figure 60
Serial output data delay time		t <sub>SOD</sub>	-	-	150	ns	Figure 60
Serial output data hold time		t <sub>SOH</sub>	5	-	-	ns	Figure 60

### Reset Timing Characteristics (V<sub>CC</sub> = 1.8 to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t <sub>RES</sub>	1	-	-	ms	Figure 61
Reset rise time	t <sub>rRES</sub>	-	-	10	us	Figure 61

Electrical Characteristics Notes

1. For bare die and wafer products, specified up to 85 .
2. The following three circuits are I/O pin configurations.

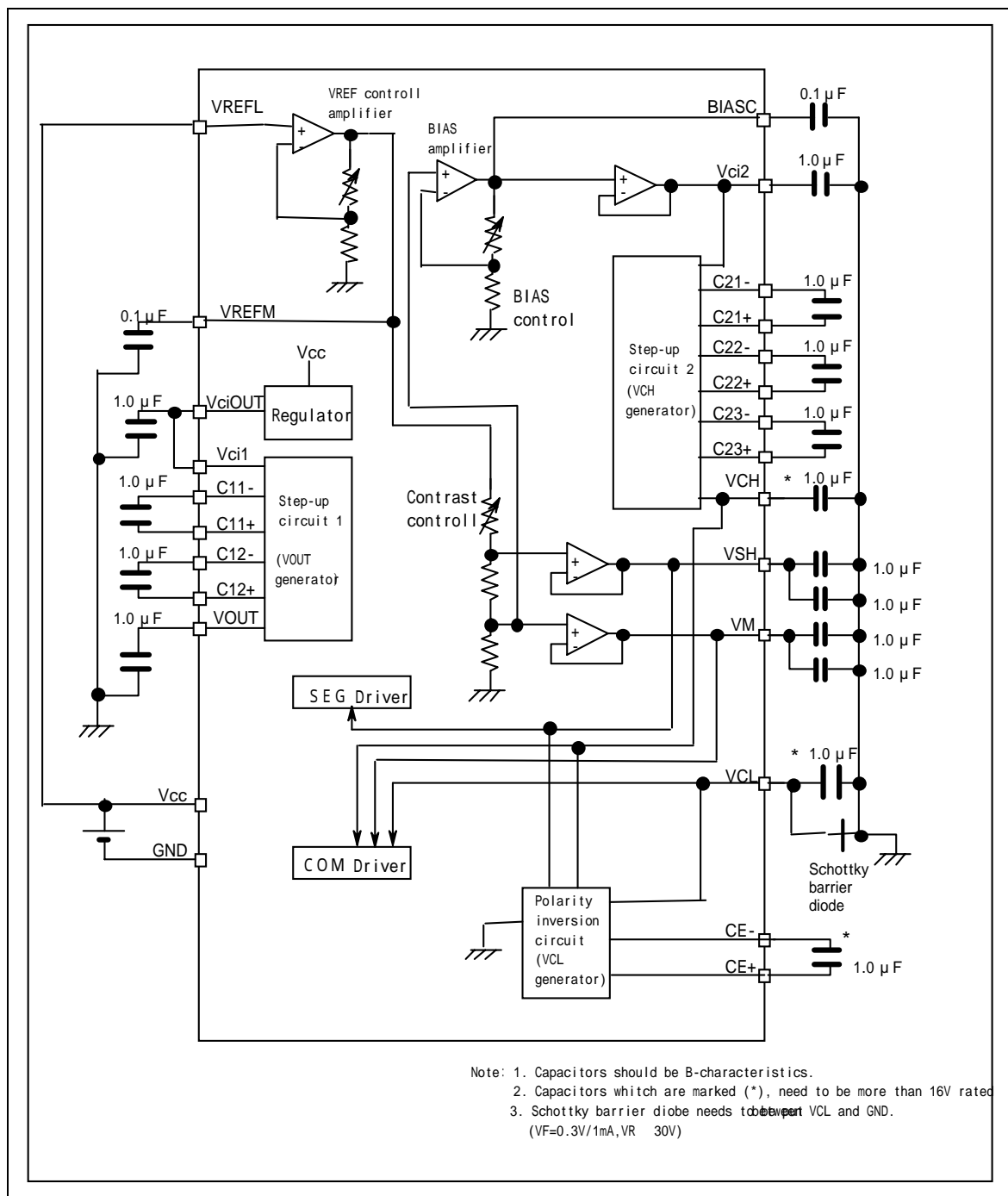
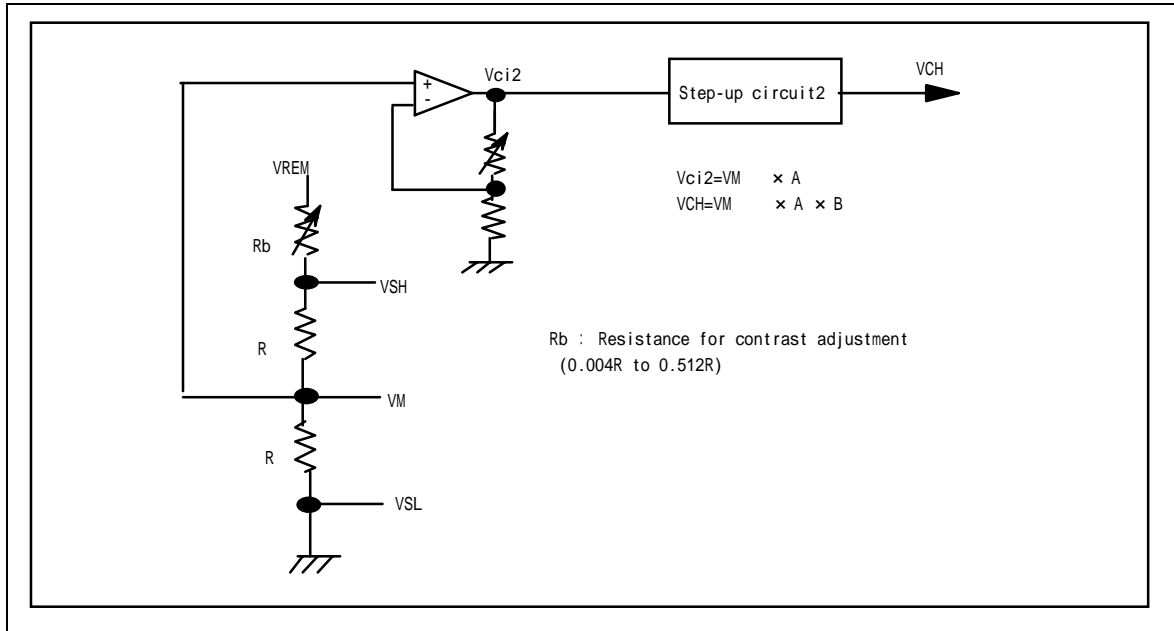


Figure 53 I/O Pin Configuration

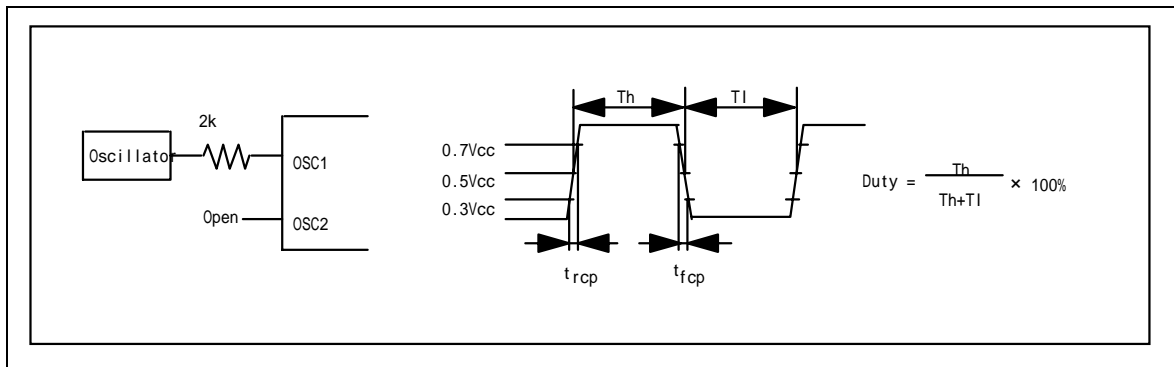
## HD66762

3. The TEST pin must be grounded and the IM2/IM1/0 pins must be grounded or connected to Vcc.
4. Applies to the resistor value (RSEG) between power supply pins VSH, GND and segment signal pins.
5. This excludes the current flowing through output drive MOSs.
6. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating.
7. The following shows the relationship between the operation frequency and current consumption.



**Figure 54 Relationship between the Operation Frequency and Current Consumption**

8. Applies to the external clock input.



**Figure 55 External Clock Supply**

9. Applies to the internal oscillator operations using external oscillation resistor Rf.

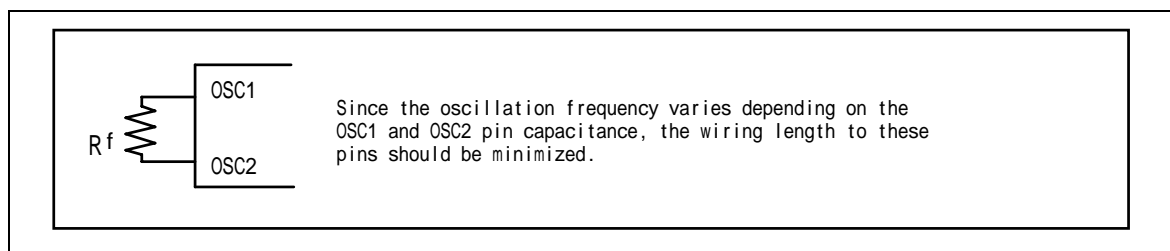


Figure 56 Internal Oscillation

Table 30 External Resistance Value and R-C Oscillation Frequency (Referential Data)

External Resistance (Rf)	R-C Oscillation Frequency: fosc				
	Vcc = 1.8 V	Vcc = 2.2 V	Vcc = 2.4 V	Vcc = 3.0 V	Vcc = 3.6 V
91K	242.5	325.6	356.4	418.3	457.4
150 K	171.9	299.1	248.2	285.3	307.8
219 K	130.9	172.6	185.3	209.4	223.8
242 K	123.0	160.3	173.2	195.0	208.0
270K	113.1	147.0	158.6	177.9	189.2
362 K	90.7	115.8	124.2	137.5	145.1
434 K	79.0	100.1	107.2	118.0	124.2
583 K	63.3	78.8	83.5	90.7	95.1
682 K	55.8	68.8	72.6	78.5	81.9
2125 K	21.6	24.9	25.7	26.9	27.6

Load Circuits

AC Characteristics Test Load Circuits

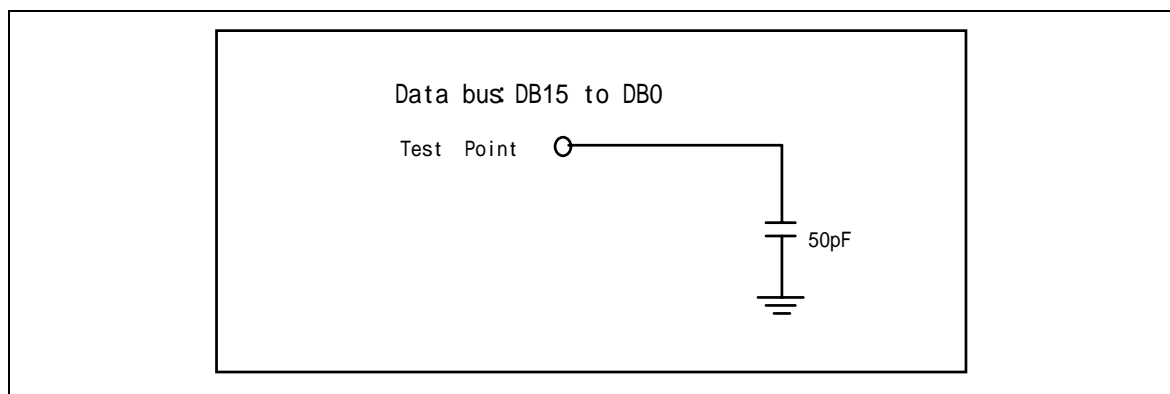


Figure 57 Load Circuit

Timing Characteristics

68-system Bus Operation

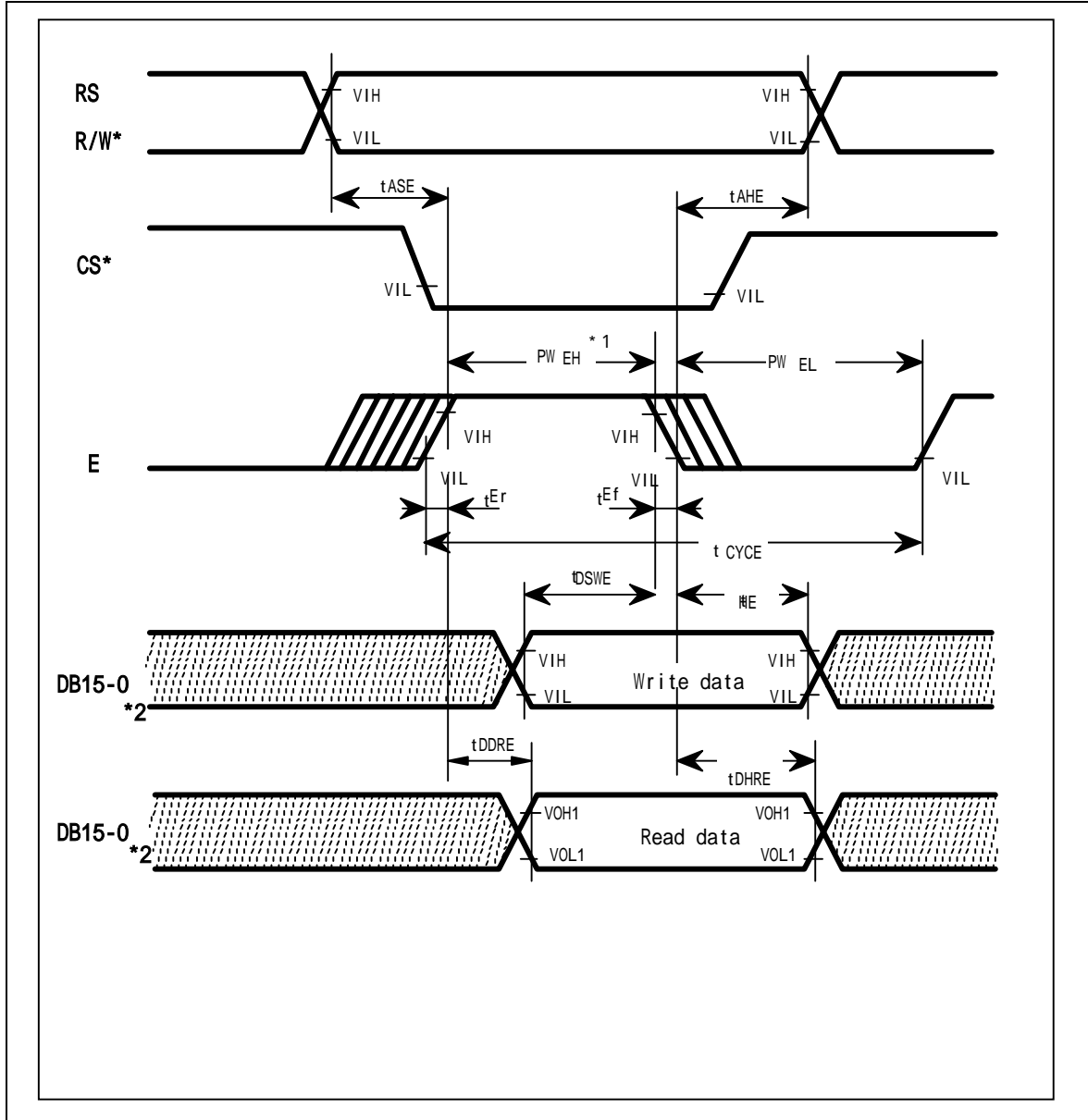


Figure 58 68-system Bus Timing

80-system Bus Operation

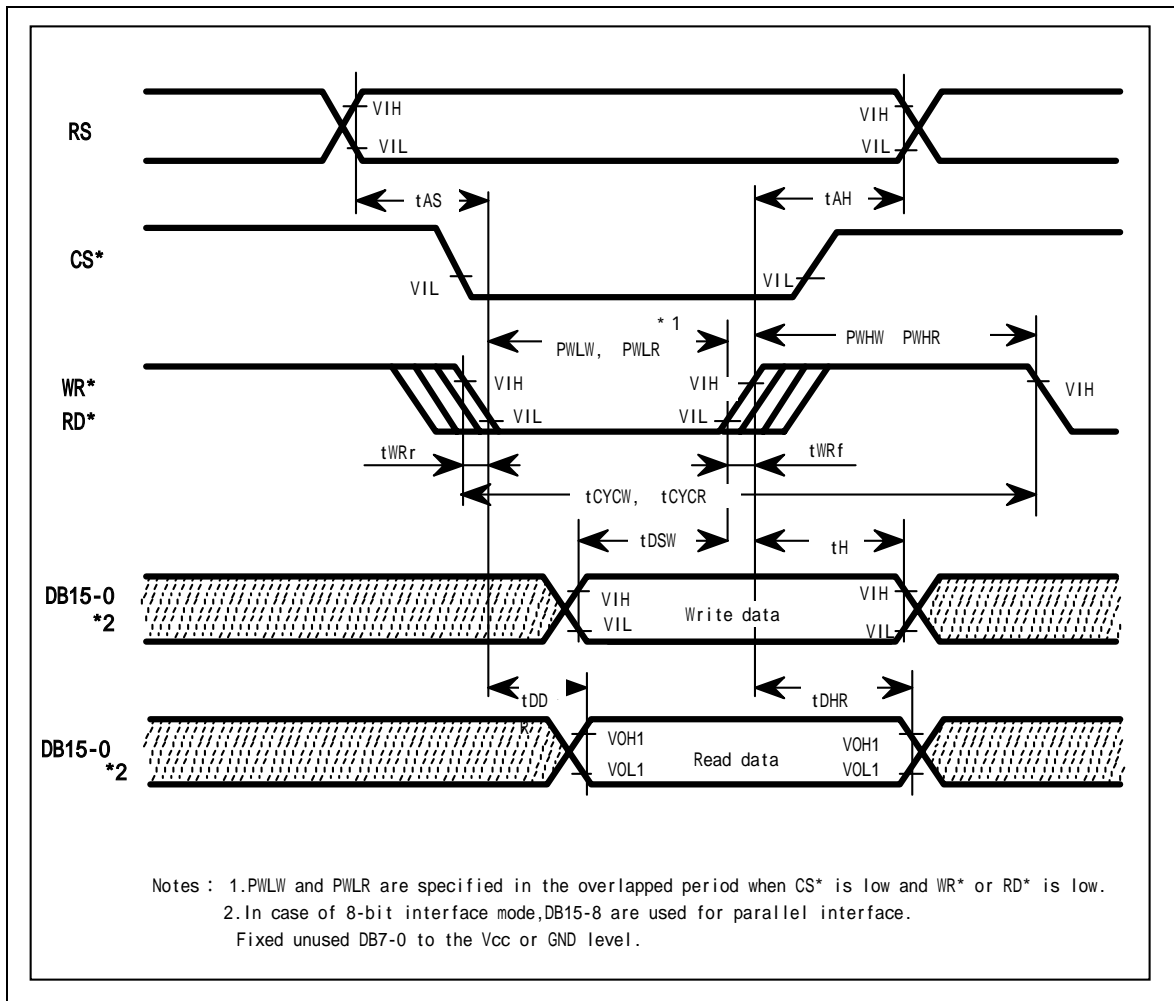


Figure 59 80-system Bus Timing

Clock Synchronized Serial Interface Operation

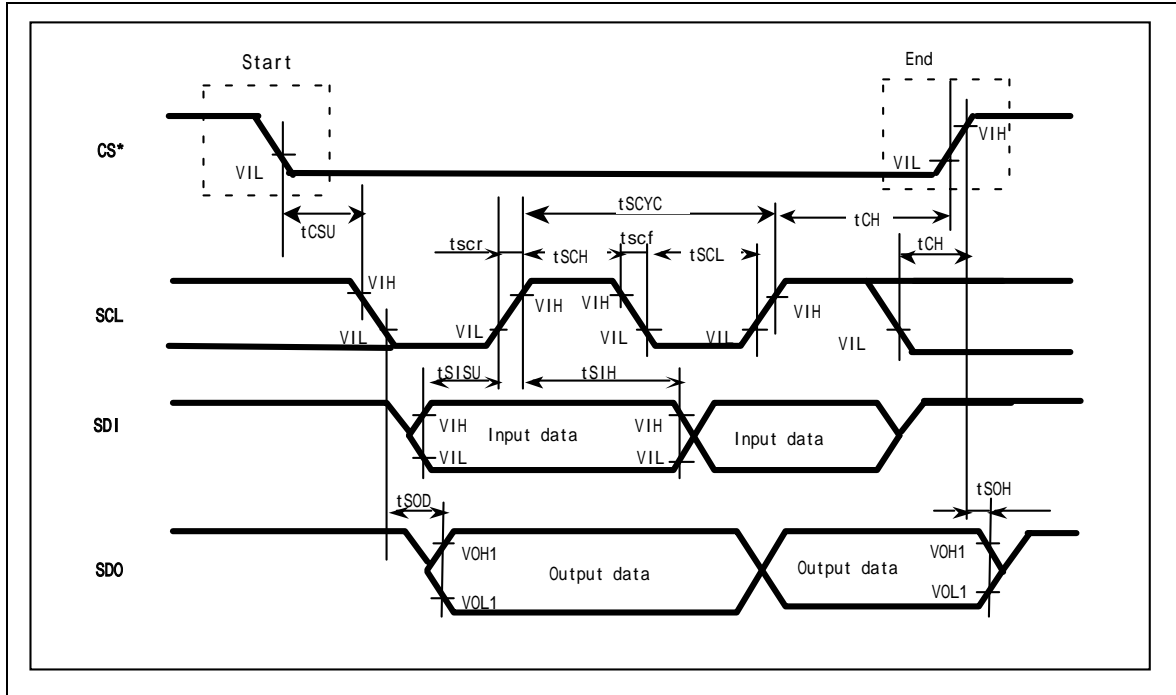


Figure 60 Clock Synchronized Serial Interface Input Timing

Reset Operation

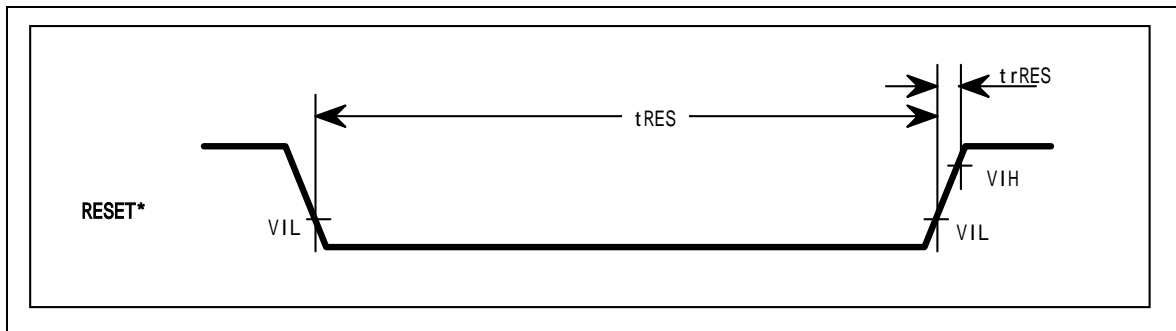


Figure 61 Reset