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Renesas Technology Corp.  
April 1, 2003

# HD66768

(104 x 84-dot Graphics LCD Controller/Driver for 65K Colors)

# HITACHI

Rev. 0.31  
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## 1. Description

The HD66768, color-graphics LCD controller and driver LSI, displays 104-by-84-dot graphics. HD66768 can simultaneously display 65,000 colors at maximum. A high-speed bus interface and high-speed RAM write function enable efficient data transfer and high-speed rewriting of data to the graphics RAM.

The HD66768 has various functions for reducing the power consumption of a LCD system. Such as low-voltage operation of 1.7 V/min., a step-up circuit to generate a maximum of 12-times the LCD drive voltage from the supplied voltage, and voltage-followers to decrease the direct current flow in the LCD drive bleeder-resistors. Combining these hardware functions with software functions, such as a partial display with low-duty drive and standby and sleep modes, allows precise power control. The HD66768 is suitable for any mid-sized or small portable battery-driven product requiring long-term driving capabilities, such as digital cellular phones supporting a WWW browser, bi-directional pagers, and small PDAs.

## 2. Features

- Color display: 104RGB x 84-dot graphics display LCD controller/driver  
Display color: 65,000 colors by dithering (16-bit/pixel)  
4,096 colors (12-bit/pixel)  
256 colors (8-bit/pixel)
- low voltage drive and flickerless PWM grayscale drive
- 8-bit high-speed bus interface and Three or Four-lines Serial Interface
- High-speed burst-RAM write function

- Writing to a window-RAM address area by using a window-address function
- Bit-operation functions for graphics processing:
  - Write-data mask function in bit units.
  - Logical operation in pixel unit and conditional write function.
- Various color-display control functions
  - Built-in grayscale palette
  - Vertical scroll display function in raster-row units
  - Partial LCD drive of two screens in any position
- Low-power operation supports:
  - Vcc = 1.7 to 3.6 V (low-voltage)
  - VLPS = 5 to 17V (Low-voltage LCD drive)
  - Equipped with power saving functions such as stand by mode
  - Built-in power supply circuit
  - Programmable drive duty ratio (1/8 to 1/84) and bias value (1/4 to 1/11) displayed on LCD
  - Maximum 6-times step-up circuit for liquid crystal drives voltage
  - 128-step contrast adjuster and voltage followers to decrease direct current flow in the LCD drive bleeder-resistors
- Internal RAM capacity: 17,472 bytes
- 312-segment × 84-common liquid crystal display driver
- n-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Internal oscillation and hardware reset
- COM positioned on both sides in one chip for COG
- Built-in E<sup>2</sup>PROM interface

#### Notes

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3. HD66768 Pad Arrangement

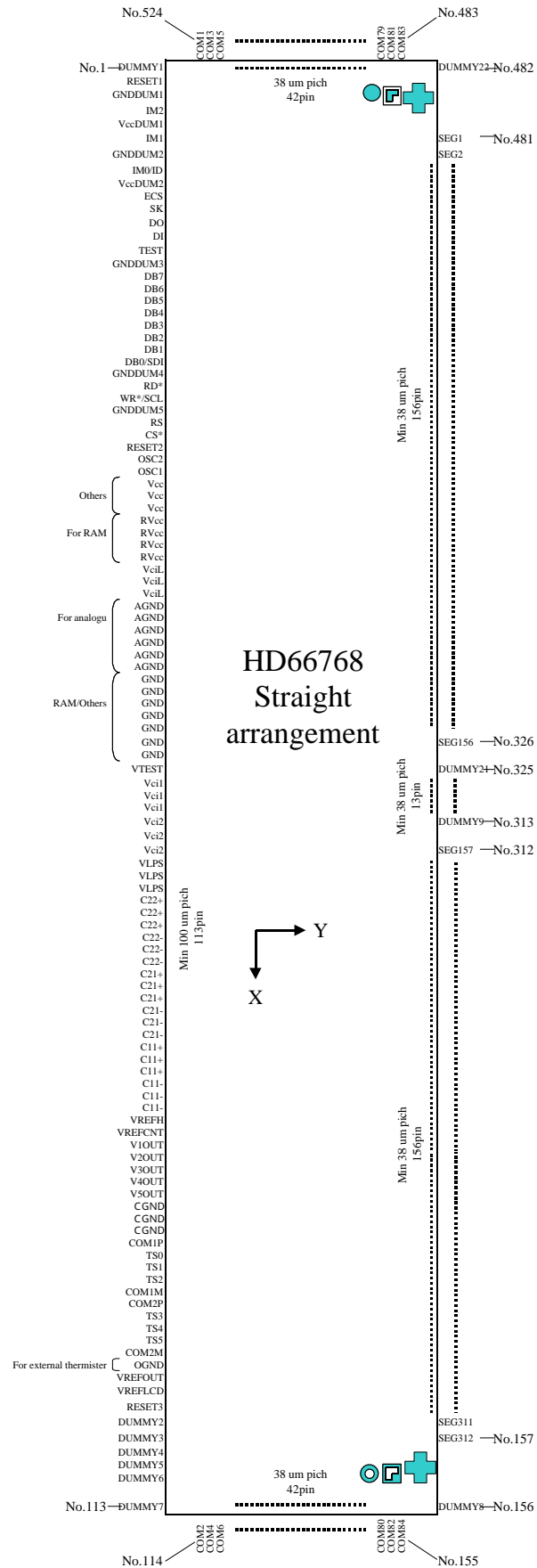
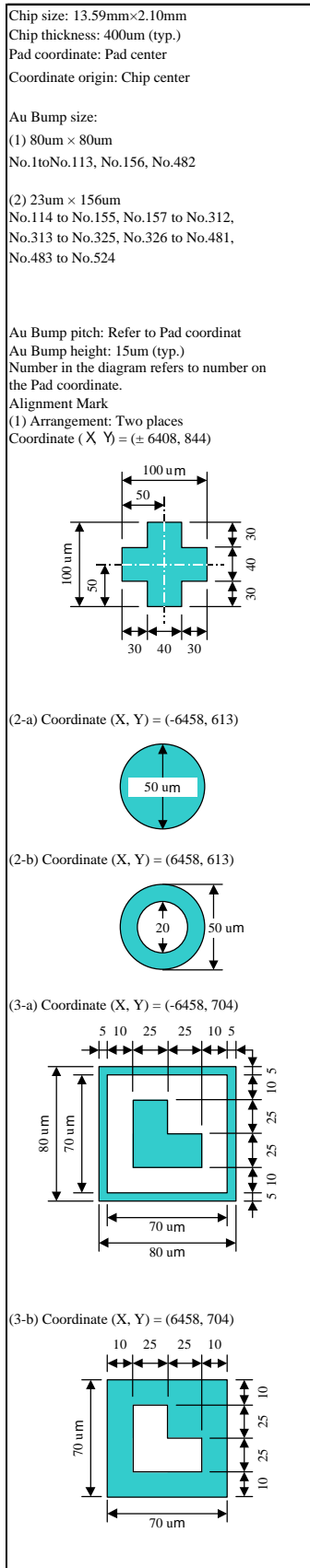


Figure 1 PAD arrangement

Table 1

4. HD66768PAD Coordinate (Straight) (No.1)

ver 0.2 2002.07.15

(Unit: um)

No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y
1	DUMMY1	-6665	-912	91	CGND	4093	-912	181	SEG288	5303	882	271	SEG198	1869	882
2	RESET1	-6519	-912	92	CGND	4193	-912	182	SEG287	5265	882	272	SEG197	1831	882
3	GNDDUM1	-6394	-912	93	CGND	4293	-912	183	SEG286	5227	882	273	SEG196	1793	882
4	IM2	-6270	-912	94	COM1P	4393	-912	184	SEG285	5188	882	274	SEG195	1755	882
5	VccDUM1	-6169	-912	95	TS0	4493	-912	185	SEG284	5150	882	275	SEG194	1717	882
6	IM1	-6069	-912	96	TS1	4593	-912	186	SEG283	5112	882	276	SEG193	1679	882
7	GNDDUM2	-5945	-912	97	TS2	4693	-912	187	SEG282	5074	882	277	SEG192	1640	882
8	IM0/ID	-5820	-912	98	COM1M	4793	-912	188	SEG281	5036	882	278	SEG191	1602	882
9	VccDUM2	-5720	-912	99	COM2P	4893	-912	189	SEG280	4998	882	279	SEG190	1564	882
10	ECS	-5620	-912	100	TS3	4993	-912	190	SEG279	4960	882	280	SEG189	1526	882
11	SK	-5467	-912	101	TS4	5094	-912	191	SEG278	4921	882	281	SEG188	1488	882
12	DO	-5314	-912	102	TS5	5194	-912	192	SEG277	4883	882	282	SEG187	1450	882
13	DI	-5161	-912	103	COM2M	5294	-912	193	SEG276	4845	882	283	SEG186	1412	882
14	TEST	-5007	-912	104	OGND	5394	-912	194	SEG275	4807	882	284	SEG185	1373	882
15	GNDDUM3	-4883	-912	105	VREFOUT	5536	-912	195	SEG274	4769	882	285	SEG184	1335	882
16	DB7	-4758	-912	106	VREFLCD	5687	-912	196	SEG273	4731	882	286	SEG183	1297	882
17	DB6	-4605	-912	107	RESET3	5864	-912	197	SEG272	4692	882	287	SEG182	1259	882
18	DB5	-4452	-912	108	DUMMY2	6084	-912	198	SEG271	4654	882	288	SEG181	1221	882
19	DB4	-4299	-912	109	DUMMY3	6184	-912	199	SEG270	4616	882	289	SEG180	1183	882
20	DB3	-4146	-912	110	DUMMY4	6284	-912	200	SEG269	4578	882	290	SEG179	1145	882
21	DB2	-3993	-912	111	DUMMY5	6384	-912	201	SEG268	4540	882	291	SEG178	1106	882
22	DB1	-3840	-912	112	DUMMY6	6484	-912	202	SEG267	4502	882	292	SEG177	1068	882
23	DB0/SD1	-3686	-912	113	DUMMY7	6665	-912	203	SEG266	4464	882	293	SEG176	1030	882
24	GNDDUM4	-3562	-912	114	COM2	6627	-744	204	SEG265	4425	882	294	SEG175	992	882
25	RD*	-3437	-912	115	COM4	6627	-706	205	SEG264	4387	882	295	SEG174	954	882
26	WR*/SCL	-3286	-912	116	COM6	6627	-668	206	SEG263	4349	882	296	SEG173	916	882
27	GNDDUM5	-3161	-912	117	COM8	6627	-629	207	SEG262	4311	882	297	SEG172	877	882
28	RS	-3037	-912	118	COM10	6627	-591	208	SEG261	4273	882	298	SEG171	839	882
29	CS*	-2883	-912	119	COM12	6627	-553	209	SEG260	4235	882	299	SEG170	801	882
30	RESET2	-2730	-912	120	COM14	6627	-515	210	SEG259	4197	882	300	SEG169	763	882
31	OSC2	-2577	-912	121	COM16	6627	-477	211	SEG258	4158	882	301	SEG168	725	882
32	OSC1	-2424	-912	122	COM18	6627	-439	212	SEG257	4120	882	302	SEG167	687	882
33	Vcc	-2248	-912	123	COM20	6627	-401	213	SEG256	4082	882	303	SEG166	649	882
34	Vcc	-2148	-912	124	COM22	6627	-362	214	SEG255	4044	882	304	SEG165	610	882
35	Vcc	-2048	-912	125	COM24	6627	-324	215	SEG254	4006	882	305	SEG164	572	882
36	RVcc	-1948	-912	126	COM26	6627	-286	216	SEG253	3968	882	306	SEG163	534	882
37	RVcc	-1848	-912	127	COM28	6627	-248	217	SEG252	3929	882	307	SEG162	496	882
38	RVcc	-1748	-912	128	COM30	6627	-210	218	SEG251	3891	882	308	SEG161	458	882
39	RVcc	-1648	-912	129	COM32	6627	-172	219	SEG250	3853	882	309	SEG160	420	882
40	VciL	-1509	-912	130	COM34	6627	-134	220	SEG249	3815	882	310	SEG159	382	882
41	VciL	-1409	-912	131	COM36	6627	-95	221	SEG248	3777	882	311	SEG158	343	882
42	VciL	-1309	-912	132	COM38	6627	-57	222	SEG247	3739	882	312	SEG157	305	882
43	AGND	-1170	-912	133	COM40	6627	-19	223	SEG246	3701	882	313	DUMMY9	229	882
44	AGND	-1070	-912	134	COM42	6627	19	224	SEG245	3662	882	314	DUMMY10	191	882
45	AGND	-970	-912	135	COM44	6627	57	225	SEG244	3624	882	315	DUMMY11	153	882
46	AGND	-870	-912	136	COM46	6627	95	226	SEG243	3586	882	316	DUMMY12	114	882
47	AGND	-770	-912	137	COM48	6627	134	227	SEG242	3548	882	317	DUMMY13	76	882
48	AGND	-670	-912	138	COM50	6627	172	228	SEG241	3510	882	318	DUMMY14	38	882
49	GND	-521	-912	139	COM52	6627	210	229	SEG240	3472	882	319	DUMMY15	0	882
50	GND	-421	-912	140	COM54	6627	248	230	SEG239	3434	882	320	DUMMY16	-38	882
51	GND	-321	-912	141	COM56	6627	286	231	SEG238	3395	882	321	DUMMY17	-76	882
52	GND	-221	-912	142	COM58	6627	324	232	SEG237	3357	882	322	DUMMY18	-114	882
53	GND	-120	-912	143	COM60	6627	362	233	SEG236	3319	882	323	DUMMY19	-153	882
54	GND	-20	-912	144	COM62	6627	401	234	SEG235	3281	882	324	DUMMY20	-191	882
55	GND	80	-912	145	COM64	6627	439	235	SEG234	3243	882	325	DUMMY21	-229	882
56	VTEST	229	-912	146	COM66	6627	477	236	SEG233	3205	882	326	SEG156	-305	882
57	Vci1	329	-912	147	COM68	6627	515	237	SEG232	3166	882	327	SEG155	-343	882
58	Vci1	429	-912	148	COM70	6627	553	238	SEG231	3128	882	328	SEG154	-382	882
59	Vci1	529	-912	149	COM72	6627	591	239	SEG230	3090	882	329	SEG153	-420	882
60	Vci2	708	-912	150	COM74	6627	629	240	SEG229	3052	882	330	SEG152	-458	882
61	Vci2	808	-912	151	COM76	6627	668	241	SEG228	3014	882	331	SEG151	-496	882
62	Vci2	908	-912	152	COM78	6627	706	242	SEG227	2976	882	332	SEG150	-534	882
63	VLPS	1057	-912	153	COM80	6627	744	243	SEG226	2938	882	333	SEG149	-572	882
64	VLPS	1157	-912	154	COM82	6627	782	244	SEG225	2899	882	334	SEG148	-610	882
65	VLPS	1257	-912	155	COM84	6627	820	245	SEG224	2861	882	335	SEG147	-649	882
66	C22+	1406	-912	156	DUMMY8	6665	918	246	SEG223	2823	882	336	SEG146	-687	882
67	C22+	1506	-912	157	SEG312	6218	882	247	SEG222	2785	882	337	SEG145	-725	882
68	C22+	1606	-912	158	SEG311	6180	882	248	SEG221	2747	882	338	SEG144	-763	882
69	C22-	1707	-912	159	SEG310	6142	882	249	SEG220	2709	882	339	SEG143	-801	882
70	C22-	1807	-912	160	SEG309	6104	882	250	SEG219	2671	882	340	SEG142	-839	882
71	C22-	1907	-912	161	SEG308	6066	882	251	SEG218	2632	882	341	SEG141	-877	882
72	C21+	2007	-912	162	SEG307	6028	882	252	SEG217	2594	882	342	SEG140	-916	882
73	C21+	2107	-912	163	SEG306	5990	882	253	SEG216	2556	882	343	SEG139	-954	882
74	C21+	2207	-912	164	SEG305	5951	882	254	SEG215	2518	882	344	SEG138	-992	882
75	C21-	2307	-912	165	SEG304	5913	882	255	SEG214	2480	882	345	SEG137	-1030	882
76	C21-	2407	-912	166	SEG303	5875	882	256	SEG213	2442	882	346	SEG136	-1068	882
77	C21-	2507	-912	167	SEG302	5837	882	257	SEG212	2403	882	347	SEG135	-1106	882
78	C11+	2658	-912	168	SEG301	5799	882	258	SEG211	2365	882	348	SEG134	-1145	882
79	C11+	2758	-912	169	SEG300	5761	882	259	SEG210	2327	882	349	SEG133	-1183	882
80	C11+	2858	-912	170	SEG299	5723	882	260	SEG209	2289	882	350	SEG132	-1221	882
81	C11-	2958	-912	171	SEG298	5684	882	261	SEG208	2251	882	351	SEG131	-1259	882
82	C11-	3058	-912	172	SEG297	5646	882	262	SEG207	2213	882	352	SEG130	-1297	882
83	C11-	3158	-912	173	SEG296	5608	882	263	SEG206	2175	882	353	SEG129	-1335	882
84	VREFH	3309	-912	174	SEG295	5570	882	264	SEG205	2136	882	354	SEG128	-1373	882
85	VREFCNT	3409	-912	175	SEG294	5532	882	265	SEG204	2098	882	355	SEG127	-1412	882
86	VIOU	3509	-912	176	SEG293	5494	882	266	SEG203	2060	882	356	SEG126	-1450	882
87	V2OUT	3609	-912	177	SEG292	5455	882	267	SEG202	2022	882	357	SEG125	-1488	882
88	V3OUT	3710	-912	178	SEG291	5417	882	268	SEG201	1984	8				

Table 1 cont.

HD66768PAD Coordinate (Straight) (No.2)

No.	pad name	X	Y	No.	pad name	X	Y	Alignment Mark	X	Y
361	SEG121	-1640	882	451	SEG31	-5074	882	Cross	-6408	844
362	SEG120	-1679	882	452	SEG30	-5112	882		6408	844
363	SEG119	-1717	882	453	SEG29	-5150	882	Circle (Positive)	-6458	613
364	SEG118	-1755	882	454	SEG28	-5188	882	Circle (Negative)	6458	613
365	SEG117	-1793	882	455	SEG27	-5227	882	L (Positive)	-6458	704
366	SEG116	-1831	882	456	SEG26	-5265	882	L (Negative)	6458	704
367	SEG115	-1869	882	457	SEG25	-5303	882			
368	SEG114	-1908	882	458	SEG24	-5341	882			
369	SEG113	-1946	882	459	SEG23	-5379	882			
370	SEG112	-1984	882	460	SEG22	-5417	882			
371	SEG111	-2022	882	461	SEG21	-5455	882			
372	SEG110	-2060	882	462	SEG20	-5494	882			
373	SEG109	-2098	882	463	SEG19	-5532	882			
374	SEG108	-2136	882	464	SEG18	-5570	882			
375	SEG107	-2175	882	465	SEG17	-5608	882			
376	SEG106	-2213	882	466	SEG16	-5646	882			
377	SEG105	-2251	882	467	SEG15	-5684	882			
378	SEG104	-2289	882	468	SEG14	-5723	882			
379	SEG103	-2327	882	469	SEG13	-5761	882			
380	SEG102	-2365	882	470	SEG12	-5799	882			
381	SEG101	-2403	882	471	SEG11	-5837	882			
382	SEG100	-2442	882	472	SEG10	-5875	882			
383	SEG99	-2480	882	473	SEG9	-5913	882			
384	SEG98	-2518	882	474	SEG8	-5951	882			
385	SEG97	-2556	882	475	SEG7	-5990	882			
386	SEG96	-2594	882	476	SEG6	-6028	882			
387	SEG95	-2632	882	477	SEG5	-6066	882			
388	SEG94	-2671	882	478	SEG4	-6104	882			
389	SEG93	-2709	882	479	SEG3	-6142	882			
390	SEG92	-2747	882	480	SEG2	-6180	882			
391	SEG91	-2785	882	481	SEG1	-6218	882			
392	SEG90	-2823	882	482	DUMMY22	-6665	918			
393	SEG89	-2861	882	483	COM83	-6627	820			
394	SEG88	-2899	882	484	COM81	-6627	782			
395	SEG87	-2938	882	485	COM79	-6627	744			
396	SEG86	-2976	882	486	COM77	-6627	706			
397	SEG85	-3014	882	487	COM75	-6627	668			
398	SEG84	-3052	882	488	COM73	-6627	629			
399	SEG83	-3090	882	489	COM71	-6627	591			
400	SEG82	-3128	882	490	COM69	-6627	553			
401	SEG81	-3166	882	491	COM67	-6627	515			
402	SEG80	-3205	882	492	COM65	-6627	477			
403	SEG79	-3243	882	493	COM63	-6627	439			
404	SEG78	-3281	882	494	COM61	-6627	401			
405	SEG77	-3319	882	495	COM59	-6627	362			
406	SEG76	-3357	882	496	COM57	-6627	324			
407	SEG75	-3395	882	497	COM55	-6627	286			
408	SEG74	-3434	882	498	COM53	-6627	248			
409	SEG73	-3472	882	499	COM51	-6627	210			
410	SEG72	-3510	882	500	COM49	-6627	172			
411	SEG71	-3548	882	501	COM47	-6627	134			
412	SEG70	-3586	882	502	COM45	-6627	95			
413	SEG69	-3624	882	503	COM43	-6627	57			
414	SEG68	-3662	882	504	COM41	-6627	19			
415	SEG67	-3701	882	505	COM39	-6627	-19			
416	SEG66	-3739	882	506	COM37	-6627	-57			
417	SEG65	-3777	882	507	COM35	-6627	-95			
418	SEG64	-3815	882	508	COM33	-6627	-134			
419	SEG63	-3853	882	509	COM31	-6627	-172			
420	SEG62	-3891	882	510	COM29	-6627	-210			
421	SEG61	-3929	882	511	COM27	-6627	-248			
422	SEG60	-3968	882	512	COM25	-6627	-286			
423	SEG59	-4006	882	513	COM23	-6627	-324			
424	SEG58	-4044	882	514	COM21	-6627	-362			
425	SEG57	-4082	882	515	COM19	-6627	-401			
426	SEG56	-4120	882	516	COM17	-6627	-439			
427	SEG55	-4158	882	517	COM15	-6627	-477			
428	SEG54	-4197	882	518	COM13	-6627	-515			
429	SEG53	-4235	882	519	COM11	-6627	-553			
430	SEG52	-4273	882	520	COM9	-6627	-591			
431	SEG51	-4311	882	521	COM7	-6627	-629			
432	SEG50	-4349	882	522	COM5	-6627	-668			
433	SEG49	-4387	882	523	COM3	-6627	-706			
434	SEG48	-4425	882	524	COM1	-6627	-744			
435	SEG47	-4464	882							
436	SEG46	-4502	882							
437	SEG45	-4540	882							
438	SEG44	-4578	882							
439	SEG43	-4616	882							
440	SEG42	-4654	882							
441	SEG41	-4692	882							
442	SEG40	-4731	882							
443	SEG39	-4769	882							
444	SEG38	-4807	882							
445	SEG37	-4845	882							
446	SEG36	-4883	882							
447	SEG35	-4921	882							
448	SEG34	-4960	882							
449	SEG33	-4998	882							
450	SEG32	-5036	882							



## 6. Pin Functions

Table 2 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions
IM2-1, IM0/ID	3	I	GND or V <sub>CC</sub>	Selects the MPU interface mode:
				IM2    IM1    IM0/ID    MPU Interface mode
				GND    Vcc    Vcc    80 system 8-bit bus interface
				Vcc    GND    ID    Clock synchronized serial interface (Three-lines)
Vcc    Vcc    GND    Clock synchronized serial interface (Four-lines)				
				When a serial interface is selected, the IM0 pin is used as the ID setting for a device code.
CS*	1	I	MPU	Selects the HD66768: Low: HD66768 is selected and can be accessed High: HD66768 is not selected and cannot be accessed
RS	1	I	MPU	Selects the register. Low: Index / status register High: Control register
WR*/SCL	1	I	MPU	For a parallel bus interface, serves as a write strobe signal, and writes data at the low level.  For a synchronous clock interface, serves as the synchronous clock signal.
RD*	1	I	MPU	For a parallel bus interface, serves as a read strobe signal, and reads data at the low level.  For a synchronous clock interface, fixed to the Vcc or GND level.
DB0/SDI	1	I/O	MPU	Serves as a 8-bit bi-directional data bus. For a clock-synchronous serial interface, serves as the serial data input pin (SDI). The input level is read on the rising edge of the SCL signal.
DB2-DB7	6	I/O	MPU	Serves as a 8-bit bi-directional data bus.  For a synchronous clock interface or unused pins, fixed to the Vcc or GND level.
DB1	1	I/O	MPU or Open	Serves as a 8-bit bi-directional data bus. For a synchronous clock interface, leave it open.
SEG1– SEG312	312	O	LCD	Output signals for segment drive. During the display-off period (D1–0 = “00”, “01”) standby mode (STB = “1”) or sleep mode (SLP = “1”), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = “0”, RAM address “0000” is output from SEG1. If SGS = “1”, it is output from SEG312. SEG1, SEG4, SEG7, ... display red (R), SEG2, SEG5, SEG8, ... display green (G), and SEG3, SEG6, SEG9, ... display blue (B) (SGS = “0”).

Table 2 cont.

Signals	Number of Pins	I/O	Connected to	Functions
COM1–COM84	84	O	LCD	Output signals for common drive. During the display-off period (D1–0 = “00”, “01”) sleep mode (SLP = “1”) or standby mode (STB = “1”), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = “0”, driver outputs from COM1 to COM84. If CMS = “1”, driver outputs COM84 to COM1. Note that start position of the common driver output is changed by screen diving position function.
TEST	1	I	GND	Test pin. Must be fixed to GND level.
DUMMY1~22	22	-	Open	Dummy pads. Must be disconnected.
VccDUM1~2	2	-	Input pin	Outputs the internal VCC level; short this pin when setting the adjacent input pin to the VCC level.
GNDDUM1~5	5	-	Input pin	Outputs the internal GND level. Short this pin when setting the adjacent input pin to the VCC level.
OGND	1	-	External thermistor circuit	GND pin for an external thermistor circuit. “GND” = 0V
CGND	3	-	Capacitor for stabilization, Step-up capacitance, or Shot key barrier diode	GND pin for external capacitor and shot key barrier diode. “GND” = 0V.
AGND	6	-	-	GND for power supply circuit. “GND” = 0V. Must be connected to system ground.
GND	7	-	-	GND pin for logic circuit. “GND” = 0V. Must be connected to system ground.
RVcc	4	-	-	Power supply pins for display RAM. “Vcc” = +1.7V ~+3.6V. Must be connected to system power supply.
Vcc	3	-	-	Power supply terminal. “Vcc” = 1.7V to +3.6V They must be connected to system power supply.
OSC1, OSC2	2	I/O	Oscillation-resistor	Connect an external resistor for R-C oscillation. When providing clocks from outside, input clock to OCS1 and leave OSC2 open.
RESET1~3	3	I	MPU or external R-C circuit Open unused pins	Reset pin. Initializes the LSI when low. Must be reset after power-on. Since HCD66768 has three RESET* pins, use one pin and open unused two pins.
VciL	3	I	Power supply	Power supply for an internal power suppl circuit. Connect a 2.5 to 3.6 V external power supply.
Vci1	3	I/O	Capacitor for stabilization or External power supply	Outputs internal reference voltage generated between VciL and GND. This operates as the reference voltage of step up circuit 1. When not using the internal reference voltage, connect external power supply 2.5 to 2.75V.
Vci2	3	I/O	Capacitor for stabilization or External power supply	Reference voltage of step up circuit 2. When not using the internal power supply circuit, connect an external power supply 5.0 to 5.5V.

Table 2 cont.

Signals	Number of Pins	I/O	Connected to	Functions
VLPS	3	—	Capacitor for stabilization or external power supply	A power supply for LCD drive. VLPS = 17.0V max. When using internal power supply circuit, it is output from the internal power supply circuit. Connect a capacitor for stabilization. When not using an internal power supply circuit, apply voltage from an external power supply.
C11+, C11-	6	—	Step-up capacitance	When using step-up circuit, connect an external capacitor.
C21+, C21-	6	—	Step-up capacitance	When using step-up circuit, connect an external capacitor.
C22+, C22-	6	—	Step-up capacitance	When using step-up circuit, connect an external capacitor.
VREFOUT	1	O	External thermistor circuit or open	Outputs internal reference power supply voltage. When compensating temperature, connect an external thermistor circuit. When not using internal reference power supply voltage, leave it open.
VREFLCD	1	I	External thermistor circuit or external power supply or open	Inputs reference voltage of LCD drive power supply. Use internal reference power supply voltage and connect an external thermistor circuit when compensating temperature. Since input current does not run, level input, which is divided by resistors, is also possible.
VREFH	1	O	Input pin	Output terminal for LCD driving voltage regulator circuit. Leave it open when not using.
TS0 to TS5	6	—	—	Test pin. Must be disconnected.
COM1P, COM1M, COM2P, COM2M	4	—	—	Test pin. Must be disconnected.
VREFCNT	1	—	Open	Test pin. Must be disconnected.
V1OUT to V5OUT	5	O/I	Open or Capacitor for stabilization or external breeder register	They are output from an internal operation amplifier when using an internal operation amplifier. Connect V1OUT and V5OUT to a capacitor for stabilization. When not using in internal operation amplifier, V1 to V5 level can be externally supplied.
VTEST	1	—	Open	Test pin. Must be disconnected.
ECS	1	O	Serial E2PROM	Selects HD66768 when using a serial E2PROM interface.
SK	1	O	Serial E2PROM	Serial clock when using serial E2PROM interface.
DO	1	O	Serial E2PROM	Serial output data when using serial E2PROM interface
DI	1	I	Serial E2PROM	Serial input data when using serial E2PROM interface.

## 7. Block Function Description

### (1) System Interface

The HD66768 has three high-speed system interfaces: an 80-series 8-bit bus, a Clock synchronized three lines serial interface, and a Clock synchronized four lines serial interface. The IM2-0 pins select the interface mode.

The HD66768 has three 16-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information from the control registers and the GRAM. The WDR temporarily stores data to be written into control registers and the GRAM, and the RDR temporarily stores data read from the GRAM. Data written into the GRAM from the MPU is first written into the WDR and then is automatically written into the GRAM by internal operation. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are normal.

Execution time for instruction excluding oscillation start is 0-clock cycle and instructions can be written continuously.

**Table 3 Register Selection (8-bit Parallel Interface)**

80-series Bus		RS	Operations
WR*	RD*		
0	1	0	Writes indexes into IR
1	0	0	Reads internal status
0	1	1	Writes into control registers and GRAM through WDR
1	0	1	Reads from GRAM through RDR

**Table 4 Register Selection (Clock synchronized Serial Interface)**

Three line serial	Four lines serial	RS*	Operations
Start bytes RS Bit			
0		0	Writes indexes into IR
1		1	Writes into control registers and GRAM through WDR

### (2) Bit Operation

The HD66768 supports a write data mask function that selects data into the GRAM in bit units. For details, see the Graphics Operation Function section.

### (3) Address Counter (AC)

The address counter (AC) assigns address to the GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC. After writing into the GRAM, the AC is automatically incremented by 1 (or decrement by 1). After reading from the GRAM, the AC is not updated.

### (4) Graphics RAM (GRAM)

The graphics RAM (GRAM) has 16 bits/pixel does the bit-pattern data of 104 x 84 bytes.

### (5) PWM Grayscale Palette Circuit

The grayscale palette generates a PWM signal, which corresponds to specified grayscale level. Refer to "grayscale pallet" for details.

**(6) Grayscale Control Circuit**

The grayscale control circuit performs 16-grayscale control with the pulse width modulation (PWM) method for grayscale display for each color.

**(7) Timing Generator**

The timing generator generates timing signals for the operation of internal circuits such as the GRAM. The RAM read timing for display and internal operation timing by MPU access is generated separately to avoid interference with each other.

**(8) Oscillation Circuit (OSC)**

The HD66768 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced.

**(9) Liquid Crystal Display Driver Circuit**

The liquid crystal display driver circuit consists of 84 common signal drivers (COM1 to COM84) and 312 segment signal drivers (SEG1 to SEG312).

Display pattern data from GRAM is latched to the 312-bit latch circuit. The latched data then enables the segment signal drivers to generate drive waveform outputs. The common driver outputs one of the VCH, VM or VCL voltage level. The SGS bit can change the shift direction of 312-bit data for the segment. The CMS bit can also change the shift direction for the common by selecting an appropriate direction for the device-mounting configuration.

When display is off, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

**(10) LCD drive power supply circuit**

LCD drive power supply circuit generates necessary voltage to drive LCD panel.

8. GRAM ADDRESS DIAGRAM (HD66768)

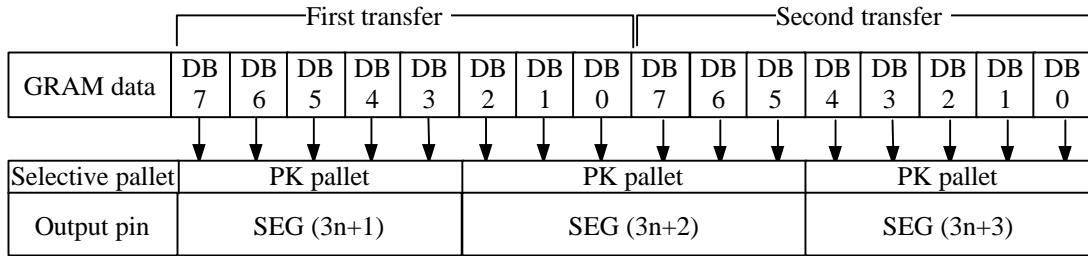
Table 5 Relationship between GRAM address and display position (SGS = "0")

SEG/COM pins		SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	.....	SEG301	SEG302	SEG303	SEG304	SEG305	SEG306	SEG307	SEG308	SEG309	SEG310	SEG311	SEG312
CMS=0	CMS=1	DB 15	DB 0	DB 15	DB 0	DB 15	DB 0	DB 15	DB 0	DB 15	DB 0	DB 15	DB 0		DB 15	DB 0	DB 15	DB 0	DB 15	DB 0	DB 15	DB 0	DB 15	DB 0	DB 15	DB 0
COM1	COM84	"0000"	"H	"0001"	"H	"0002"	"H	"0003"	"H	.....	"0064"	"H	"0065"	"H	"0066"	"H	"0067"	"H								
COM2	COM83	"0100"	"H	"0101"	"H	"0102"	"H	"0103"	"H	.....	"0164"	"H	"0165"	"H	"0166"	"H	"0167"	"H								
COM3	COM82	"0200"	"H	"0201"	"H	"0202"	"H	"0203"	"H	.....	"0264"	"H	"0265"	"H	"0266"	"H	"0267"	"H								
COM4	COM81	"0300"	"H	"0301"	"H	"0302"	"H	"0303"	"H	.....	"0364"	"H	"0365"	"H	"0366"	"H	"0367"	"H								
COM5	COM80	"0400"	"H	"0401"	"H	"0402"	"H	"0403"	"H	.....	"0464"	"H	"0465"	"H	"0466"	"H	"0467"	"H								
COM6	COM79	"0500"	"H	"0501"	"H	"0502"	"H	"0503"	"H	.....	"0564"	"H	"0565"	"H	"0566"	"H	"0567"	"H								
COM7	COM78	"0600"	"H	"0601"	"H	"0602"	"H	"0603"	"H	.....	"0664"	"H	"0665"	"H	"0666"	"H	"0667"	"H								
COM8	COM77	"0700"	"H	"0701"	"H	"0702"	"H	"0703"	"H	.....	"0764"	"H	"0765"	"H	"0766"	"H	"0767"	"H								
COM9	COM76	"0800"	"H	"0801"	"H	"0802"	"H	"0803"	"H	.....	"0864"	"H	"0865"	"H	"0866"	"H	"0867"	"H								
COM10	COM75	"0900"	"H	"0901"	"H	"0902"	"H	"0903"	"H	.....	"0964"	"H	"0965"	"H	"0966"	"H	"0967"	"H								
COM11	COM74	"0A00"	"H	"0A01"	"H	"0A02"	"H	"0A03"	"H	.....	"0A64"	"H	"0A65"	"H	"0A66"	"H	"0A67"	"H								
COM12	COM73	"0B00"	"H	"0B01"	"H	"0B02"	"H	"0B03"	"H	.....	"0B64"	"H	"0B65"	"H	"0B66"	"H	"0B67"	"H								
COM13	COM72	"0C00"	"H	"0C01"	"H	"0C02"	"H	"0C03"	"H	.....	"0C64"	"H	"0C65"	"H	"0C66"	"H	"0C67"	"H								
COM14	COM71	"0D00"	"H	"0D01"	"H	"0D02"	"H	"0D03"	"H	.....	"0D64"	"H	"0D65"	"H	"0D66"	"H	"0D67"	"H								
COM15	COM70	"0E00"	"H	"0E01"	"H	"0E02"	"H	"0E03"	"H	.....	"0E64"	"H	"0E65"	"H	"0E66"	"H	"0E67"	"H								
COM16	COM69	"0F00"	"H	"0F01"	"H	"0F02"	"H	"0F03"	"H	.....	"0F64"	"H	"0F65"	"H	"0F66"	"H	"0F67"	"H								
COM17	COM68	"1000"	"H	"1001"	"H	"1002"	"H	"1003"	"H	.....	"1064"	"H	"1065"	"H	"1066"	"H	"1067"	"H								
COM18	COM67	"1100"	"H	"1101"	"H	"1102"	"H	"1103"	"H	.....	"1164"	"H	"1165"	"H	"1166"	"H	"1167"	"H								
COM19	COM66	"1200"	"H	"1201"	"H	"1202"	"H	"1203"	"H	.....	"1264"	"H	"1265"	"H	"1266"	"H	"1267"	"H								
COM20	COM65	"1300"	"H	"1301"	"H	"1302"	"H	"1303"	"H	.....	"1364"	"H	"1365"	"H	"1366"	"H	"1367"	"H								
⋮	⋮	⋮		⋮		⋮		⋮			⋮		⋮		⋮		⋮									
COM77	COM8	"4C00"	"H	"4C01"	"H	"4C02"	"H	"4C03"	"H	.....	"4C64"	"H	"4C65"	"H	"4C66"	"H	"4C67"	"H								
COM78	COM7	"4D00"	"H	"4D01"	"H	"4D02"	"H	"4D03"	"H	.....	"4D64"	"H	"4D65"	"H	"4D66"	"H	"4D67"	"H								
COM79	COM6	"4E00"	"H	"4E01"	"H	"4E02"	"H	"4E03"	"H	.....	"4E64"	"H	"4E65"	"H	"4E66"	"H	"4E67"	"H								
COM80	COM5	"4F00"	"H	"4F01"	"H	"4F02"	"H	"4F03"	"H	.....	"4F64"	"H	"4F65"	"H	"4F66"	"H	"4F67"	"H								
COM81	COM4	"5000"	"H	"5001"	"H	"5002"	"H	"5003"	"H	.....	"5064"	"H	"5065"	"H	"5066"	"H	"5067"	"H								
COM82	COM3	"5100"	"H	"5101"	"H	"5102"	"H	"5103"	"H	.....	"5164"	"H	"5165"	"H	"5166"	"H	"5167"	"H								
COM83	COM2	"5200"	"H	"5201"	"H	"5202"	"H	"5203"	"H	.....	"5264"	"H	"5265"	"H	"5266"	"H	"5267"	"H								
COM84	COM1	"5300"	"H	"5301"	"H	"5302"	"H	"5303"	"H	.....	"5364"	"H	"5365"	"H	"5366"	"H	"5367"	"H								

Relation between GRAM data and display contents (SGS = "0")

- SPR 1/0 = "00" 65,000 color mode

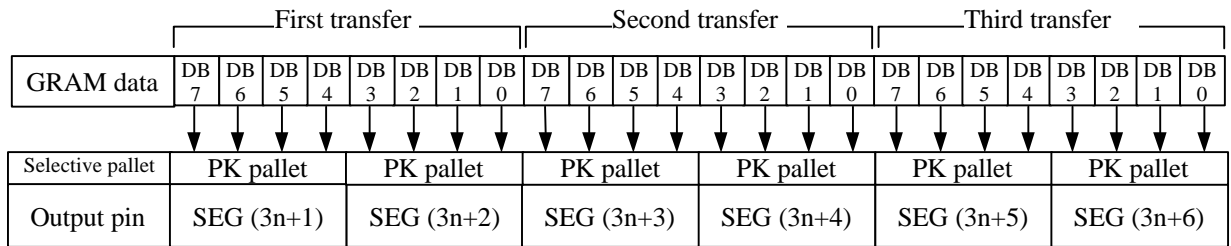
Figure 3



Note) n = Address lower 8-bit (0 to 101)

- SPR 1/0 = "01" 4,096 color mode

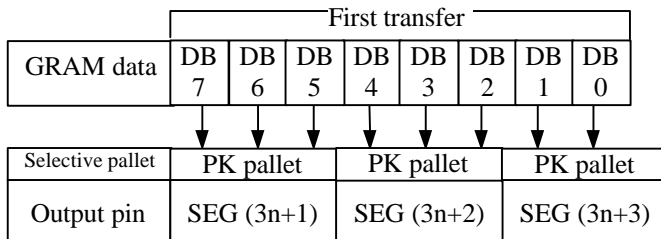
Figure 4



Note) n = Address lower 8-bit (0 to 102)

- SPR 1/0 = "10" 256 color mode

Figure 5



Note) n = address lower 8-bit (0 to 101)

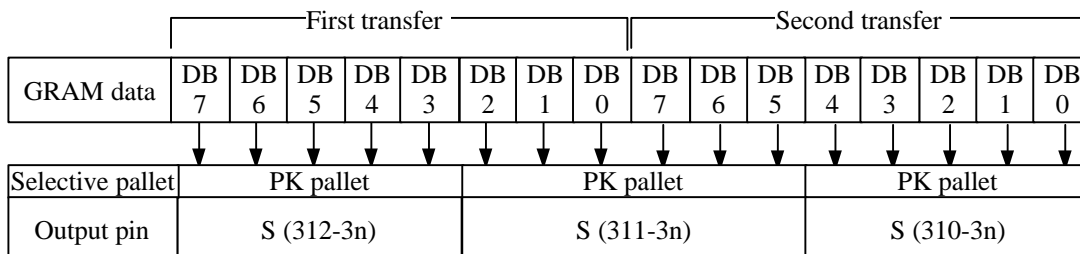
Table 6 Relationship between GRAM address and display position (SGS = "1")

SEG/COM pins		SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	...	SEG301	SEG302	SEG303	SEG304	SEG305	SEG306	SEG307	SEG308	SEG309	SEG310	SEG311	SEG312
CMS=0	CMS=1	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>	DB <sub>15</sub> ... DB <sub>0</sub>
COM1	COM84	"0067"H	"0066"H	"0065"H	"0064"H	.....	"0003"H	"0002"H	"0001"H	"0000"H																
COM2	COM83	"0167"H	"0166"H	"0165"H	"0164"H	.....	"0103"H	"0102"H	"0101"H	"0100"H																
COM3	COM82	"0267"H	"0266"H	"0265"H	"0264"H	.....	"0203"H	"0202"H	"0201"H	"0200"H																
COM4	COM81	"0367"H	"0366"H	"0365"H	"0364"H	.....	"0303"H	"0302"H	"0301"H	"0300"H																
COM5	COM80	"0467"H	"0466"H	"0465"H	"0464"H	.....	"0403"H	"0402"H	"0401"H	"0400"H																
COM6	COM79	"0567"H	"0566"H	"0565"H	"0564"H	.....	"0503"H	"0502"H	"0501"H	"0500"H																
COM7	COM78	"0667"H	"0666"H	"0665"H	"0664"H	.....	"0603"H	"0602"H	"0601"H	"0600"H																
COM8	COM77	"0767"H	"0766"H	"0765"H	"0764"H	.....	"0703"H	"0702"H	"0701"H	"0700"H																
COM9	COM76	"0867"H	"0866"H	"0865"H	"0864"H	.....	"08030"H	"0802"H	"0801"H	"0800"H																
COM10	COM75	"0967"H	"0966"H	"0965"H	"0964"H	.....	"0903"H	"0902"H	"0901"H	"0900"H																
COM11	COM74	"0A67"H	"0A66"H	"0A65"H	"0A64"H	.....	"0A03"H	"0A02"H	"0A01"H	"0A00"H																
COM12	COM73	"0B67"H	"0B66"H	"0B65"H	"0B64"H	.....	"0B03"H	"0B02"H	"0B01"H	"0B00"H																
COM13	COM72	"0C67"H	"0C66"H	"0C65"H	"0C64"H	.....	"0C03"H	"0C02"H	"0C01"H	"0C00"H																
COM14	COM71	"0D67"H	"0D66"H	"0D65"H	"0D64"H	.....	"0D03"H	"0D02"H	"0D01"H	"0D00"H																
COM15	COM70	"0E67"H	"0E66"H	"0E65"H	"0E64"H	.....	"0E03"H	"0E02"H	"0E01"H	"0E00"H																
COM16	COM69	"0F67"H	"0F66"H	"0F65"H	"0F64"H	.....	"0F03"H	"0F02"H	"0F01"H	"0F00"H																
COM17	COM68	"1067"H	"1066"H	"1065"H	"1064"H	.....	"1003"H	"1002"H	"1001"H	"1000"H																
COM18	COM67	"1167"H	"1166"H	"1165"H	"1164"H	.....	"1103"H	"1102"H	"1101"H	"1100"H																
COM19	COM66	"1267"H	"1266"H	"1265"H	"1264"H	.....	"1203"H	"1202"H	"1201"H	"1200"H																
COM20	COM65	"1367"H	"1366"H	"1365"H	"1364"H	.....	"1303"H	"1302"H	"1301"H	"1300"H																
...	...	...	...	...	...	...	...	...	...	...																
COM77	COM8	"4C67"H	"4C66"H	"4C65"H	"4C64"H	.....	"4C03"H	"4C02"H	"4C01"H	"4C00"H																
COM78	COM7	"4D67"H	"4D66"H	"4D65"H	"4D64"H	.....	"4D03"H	"4D02"H	"4D01"H	"4D00"H																
COM79	COM6	"4E67"H	"4E66"H	"4E65"H	"4E64"H	.....	"4E03"H	"4E02"H	"4E01"H	"4E00"H																
COM80	COM5	"4F67"H	"4F66"H	"4F65"H	"4F64"H	.....	"4F03"H	"4F02"H	"4F01"H	"4F00"H																
COM81	COM4	"5067"H	"5066"H	"5065"H	"5064"H	.....	"5003"H	"5002"H	"5001"H	"5000"H																
COM82	COM3	"5167"H	"5166"H	"5165"H	"5164"H	.....	"5103"H	"5102"H	"5101"H	"5100"H																
COM83	COM2	"5267"H	"5266"H	"5265"H	"5264"H	.....	"5203"H	"5202"H	"5201"H	"5200"H																
COM84	COM1	"5367"H	"5366"H	"5365"H	"5364"H	.....	"5303"H	"5302"H	"5301"H	"5300"H																

Relation between GRAM data and display contents (SGS = "1")

- SPR 1/0 = "00" 65,000 color mode

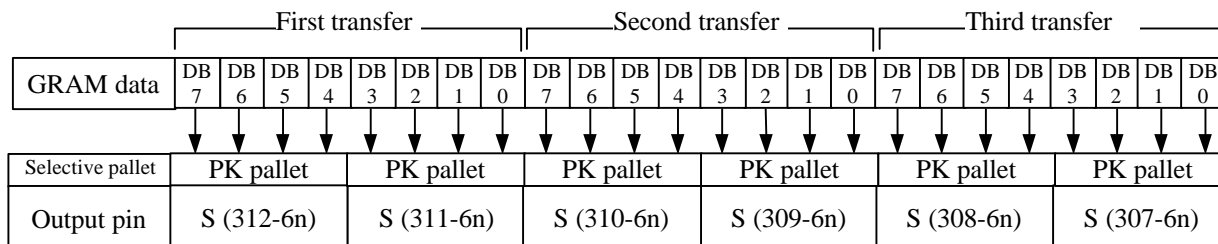
Figure 6



Note) n = Address lower 8-bit (0 to 103)

- SPR 1/0 = "01" 4,096 color mode

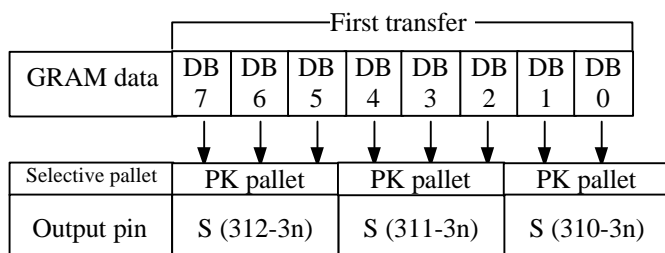
Figure 7



Note) n = Address lower 8-bit (0 to 51)

- SPR 1/0 = "10" 256 color mode

Figure 8



Note) n = address lower 8-bit (0 to 103)

## **9. Instructions**

### **Outline**

The HD66768 uses the 8-bit bus architecture. Before the internal operation of the HD66768 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the HD66768 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB15 to DB0), make up the HD66768 instructions.

There are eight categories of instructions that:

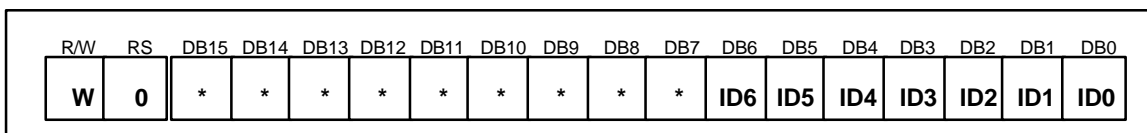
- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale palette table

Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load. Because instructions are executed in 0 cycles, they can be written continuously.

**Instruction Descriptions**

**9-1. Index: IR**

The index instruction specifies the RAM control indexes (R00h to R42h). It sets the register number in the range of “0000000” to “1111111” in binary form. However, R43 to R7F are disabled since they are test registers.



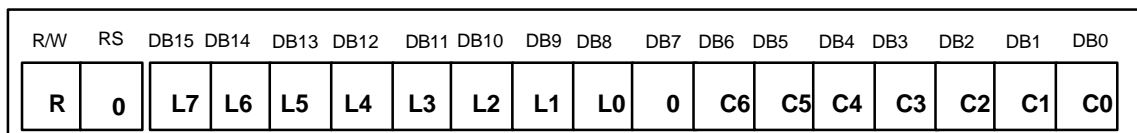
**Figure 9 Index Instruction**

**9-2. Status Read: SR**

The status read instruction reads the internal status of the HD66768.

**L7-0:** Indicate the driving raster-row position where the liquid crystal display is being driven.

**C6-0:** Read the contrast setting values (CT6-0)

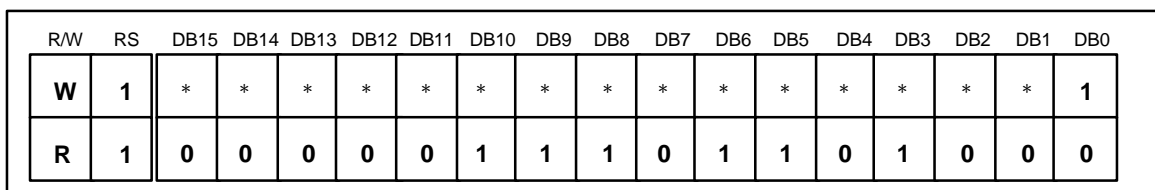


**Figure 10 Status Read Instruction**

**9-3. Start Oscillation (R00h)**

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly by 8-bit bus interface, “0768”H is read. It can not be read through a serial interface.



**Figure 11 Start Oscillation Instruction**

9-4. Driver Output Control (R01h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
w	1	0	0	0	0	0	CS FT	CMS	SGS	0	0	4L	NL4	NL3	NL2	NL1	NL0

Figure 12 Driver Output Control Instruction

**CSFT:** Selects the output scan form of common driver. Set CSFT according to the mounting method.

**CMS:** Selects the output shift direction of a common driver. Set CMS according to the mounting method.

**SGS:** Selects the output shift direction of the segment driver.

When SGS = "0", data are output SEG1 to SEG312.

When SGS = "1", data are output SEG312 to SEG1.

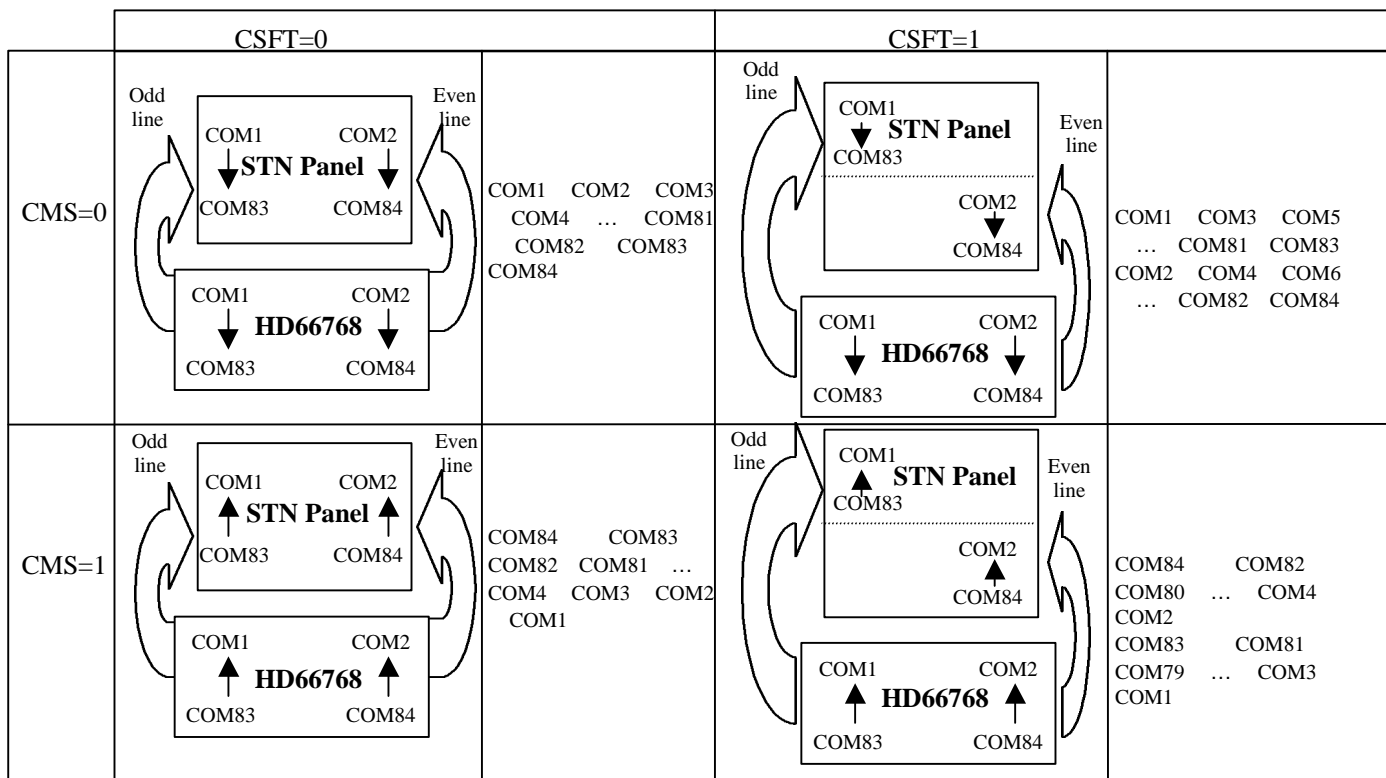
When SGS = "0", SEG1 pin assigns the color display to <R><G><B>.

When SGS = "1", SEG312 pin assigns <R><G><B>. Re-write to the RAM when intending to change the SGS bit.

**4L:** Displays display RAM data 4 times large lengthways. When 4L = "1", display RAM one line's worth of data is enlarged 4 times lengthways and displayed within the range of display RAM line scan according to the display duty. Output shift direction of common driver can be selected by CMS.

**NL4-0:** Specify the LCD drive duty ratio. The duty ratio can be adjusted for every eight raster-rows.

GRAM address mapping does not depend on the setting value of the drive duty ratio.



\*Quadruple display mode (4L = "1") is available when CSFT = "0".

Figure 13 Scan mode setting

Table 7: NL Bits and Drive Duty

NL4	NL3	NL2	NL1	NL0	Display Size	LCD drive Duty cycle
0	0	0	0	0	312 x 8 dots	1/8 Duty
0	0	0	0	1	312 x 16 dots	1/16 Duty
0	0	0	1	0	312 x 24 dots	1/24 Duty
0	0	0	1	1	312 x 32 dots	1/32 Duty
0	0	1	0	0	312 x 40 dots	1/40 Duty
0	0	1	0	1	312 x 48 dots	1/48 Duty
0	0	1	1	0	312 x 56 dots	1/56 Duty
0	0	1	1	1	312 x 64 dots	1/64 Duty
0	1	0	0	0	312 x 72 dots	1/72 Duty
0	1	0	0	1	312 x 80 dots	1/80 Duty
0	1	0	1	0	312 x 84 dots	1/84 Duty

9-5. LCD-Driving-Waveform Control (R02h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	RST	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

Figure14 LCD-Driving-Waveform Control Instruction

**RST:** When RST= 1, software are reset function is started. This function is the same as hardware RESET pin. It takes 10 clock cycle period. This bit is automatically cleared after reset function is completed. Therefore, before 10-clock cycle other instruction can not be issued. Do not set the RST bit during stand-by mode.

**B/C:** When B/C = 0, a B-attern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a C-pattern waveform is generated and alternates in each reaste-row specified by bits EOR and NW4-NW0 in the LCD-driving waveform control register. For details, see the n-raster-row Reversed AC Drive section.

**EOR:** When the C-pattern waveform is set (B/C =1) and EOR =1, the odd.even frme-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the number of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

**NW5-0:** Specify the number of raster-rows n that will alternate at the C-pattern wavefrom setting (B/C = 1). NW5-NW0 alternate for every set value + 1 raster-row, and the 2<sup>nd</sup> to the 64<sup>h</sup> raster-rows can be selected. Setting NW5-0 = "000000" (While alternating 1 line) is inhibited.

9-6. Power Control 1 (R03h)

9-7. Power Control 2 (R0Ch)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
w	1	0	0	BS2	BS1	BS0	0	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB
w	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0

Figure 15 Power Control Instrucion

**BS2-0:** The LCD drive bias value is set. The LCD drive bias value can be selected according to this drive duty ratio and voltage.

**BT1-0:** The output factor of step-up circuit is switched, The LCD drive voltage level can be selected according to tis drive duty ratio and bias. Lower amplification of the step-up circuit consumes less current.

**DC2-0:** The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit becomes high, but the current consumption is increased. Adjust the frequency considering the step-up ability and the current consumption.

**AP2-0:** Turn ON and OFF the operation of an operation amplifier and a step-up circuit. During no display, when AP2-0 = "000", the current consumption can be reduced by stopping the operational amplifier and step-up circuit operation.

**SLP:** When  $SLP = 1$ , the HD66768 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. Only the following instructions can be executed during the sleep mode.

Power control (BS2-0, BT1-0, DC2-0, AP2-0, SLP, and STB)

During the sleep mode, the other GRAM data and instructions cannot be updated although they are retained.

**STB:** When  $STB = 1$ , the HD66768 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section. Only the following instructions can be executed during the standby mode.

a. Standby mode cancel ( $STB = "0"$ )

b. Start oscillation

During the standby mode, the GRAM data instructions are lost. To prevent this, they must be set again after the standby mode is canceled.

**VC2-0:** Set an adjustment factor for the  $V_{ci1}$  voltage (VC2-0).

Setting LCD driving bias value  
Table 8

BS2	BS1	BS0	LCD driving bias value
0	0	0	1/11 bias driving
0	0	1	1/10 bias driving
0	1	0	1/9 bias driving
0	1	1	1/8 bias driving
1	0	0	1/7 bias driving
1	0	1	1/6 bias driving
1	1	0	1/5 bias driving
1	1	1	1/4 bias driving

Setting output magnification of step up circuit  
Table 9

BT1	BT0	Step up circuit 1	Step up circuit2 VLPS output
0	0	2 x Vci1	3 x Vci2
0	1	2 x Vci1	2 x Vci2
1	0	2 x Vci1	2.5 x Vci2
1	1	2 x Vci1	1.5 x Vci2

Operating clock frequency of the Booster 1 and 2  
Table 10

DC2	DC1	DC0	Operating clock frequency in the booster 1	Operating clock frequency in the voltage inverting circuit and the booster 2
0	0	0	32-divided clock	64-divided clock
0	0	1	28-divided clock	56-divided clock
0	1	0	24-divided clock	48-divided clock
0	1	1	20-divided clock	40-divided clock
1	0	0	16-divided clock	32-divided clock
1	0	1	12-divided clock	24-divided clock
1	1	0	8-divided clock	16-divided clock
1	1	1	4-divided clock	8-divided clock

Setting DC current magnification of bias circuit  
Table 11

AP2	AP1	AP0	Bias circuit1	Bias circuit2
0	0	0	Stop	Stop
0	0	1	62.5 %	100 %
0	1	0	71.4%	100 %
0	1	1	100 %	100 %
1	0	0	125 %	150 %
1	0	1	143 %	150 %
1	1	0	167 %	200 %
1	1	1	200 %	200 %

Bias circuit 1: LCD driving level generating amplifier of voltage.

Bias circuit 2: Vci1 generating amplifier.

Setting an adjustment magnification of Vci1 voltage  
Table 12

VC2	VC1	VC0	VciL adjustment magnification
0	0	0	1.00 x VciL
0	0	1	0.965 x VciL
0	1	0	0.917 x VciL
0	1	1	0.873 x VciL
1	0	0	0.833 x VciL
1	0	1	0.797 x VciL
1	1	0	0.764 x VciL
1	1	1	Stop amplifier operation of VciL adjustment amplifier. (VciL is output externally)

When Vci1 is input externally:  $Vci1 \leq VciL$

9-8. Contrast Control (R04h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	VRCNT	VR4	VR3	VR2	VR1	VR0	VRON	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Figure16 Contrast Control Instruction

**VRCNT:** A bit for connecting the output of internal reference voltage to VREFLCD inside LSI. When VRCNT = 1, the output of internal reference voltage and VREFL are connected. When connecting to an external thermistor circuit, set VRCNT = 0, and do not connect to internal reference voltage.

**VR4-0:** These bits amplify 2.0 to 10.0 times the VREFLCD as output voltage VREFH of LCD drive reference voltage generation circuit. The VREFLCD should be smaller than Vci2 level.

**VRON:** Activation bit of an internal reference voltage. When VRON = 1, an internal reference voltage outputs 3.0V (± 30mV (Ta: 85°C at designed value)) without depending on temperature. Step-up circuit 1 should be set to keep constant Vci2 output voltage between 4.5 and 5.5V.

**CT6-0:** These bits control the LCD drive voltage to adjust 128-step contrast.

Table 13 Contrast control

CT setting value							Contrast
CT6	CT5	CT4	CT3	CT2	CT1	CT0	
0	0	0	0	0	0	0	6.35R (Minimum)
0	0	0	0	0	0	1	6.30R
0	0	0	0	0	1	0	6.25R
0	0	0	0	0	1	0	6.20R
0	0	0	0	0	1	1	6.15R
↓							
1	1	1	1	1	1	0	0.05R
1	1	1	1	1	1	1	0.00R (Maximum)

Setting of output voltage of LCD driving reference voltage generating circuit

Table 14

VR4	VR3	VR2	VR1	VR0	VREFH voltage
0	0	0	0	0	VREFLCD x 2.0
0	0	0	0	1	VREFLCD x 2.3
0	0	0	1	0	VREFLCD x 2.7
0	0	0	1	1	VREFLCD x 3.0
0	0	1	0	0	VREFLCD x 3.3
0	0	1	0	1	VREFLCD x 3.7
0	0	1	1	0	VREFLCD x 4.0
0	0	1	1	1	VREFLCD x 4.3
0	1	0	0	0	VREFLCD x 4.7
0	1	0	0	1	VREFLCD x 5.0
0	1	0	1	0	VREFLCD x 5.3
0	1	0	1	1	VREFLCD x 5.7
0	1	1	0	0	VREFLCD x 6.0
0	1	1	0	1	VREFLCD x 6.3
0	1	1	1	0	VREFLCD x 6.7
0	1	1	1	1	VREFLCD x 7.0

Table 15

VR4	VR3	VR2	VR1	VR0	VREFH voltage
1	0	0	0	0	VREFLCD x 2.5
1	0	0	0	1	VREFLCD x 3.0
1	0	0	1	0	VREFLCD x 3.5
1	0	0	1	1	VREFLCD x 4.0
1	0	1	0	0	VREFLCD x 4.5
1	0	1	0	1	VREFLCD x 5.0
1	0	1	1	0	VREFLCD x 5.5
1	0	1	1	1	VREFLCD x 6.0
1	1	0	0	0	VREFLCD x 6.5
1	1	0	0	1	VREFLCD x 7.0
1	1	0	1	0	VREFLCD x 7.5
1	1	0	1	1	VREFLCD x 8.0
1	1	1	0	0	VREFLCD x 8.5
1	1	1	0	1	VREFLCD x 9.0
1	1	1	1	0	VREFLCD x 9.5
1	1	1	1	1	VREFLCD x 10.0

9-9. Entry Mode (R05h)

9-10. Compare register (R06h)

The write data sent from the microcomputer is modified in the HD66768 and written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For detail, see the Graphics Operation Function section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	SPR1	SPR0	0	0	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
W	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Figure 17 Compare Resister Instruction

**SPR1-0:** Sets displaying colors. Be aware that writing format to GRAM is different according to the setting of SPR1-0. **Table 16**

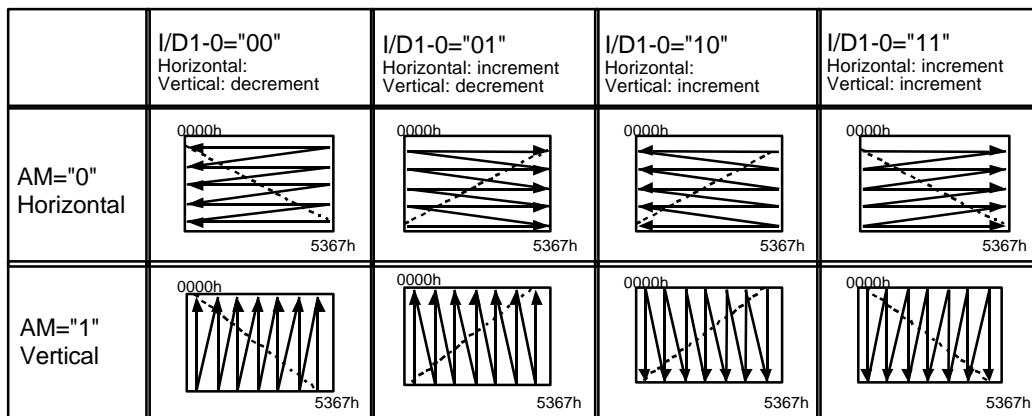
SPR1	SPR0	Displaying color
0	0	65,000 colors display
0	1	4,096 colors display
1	0	256 colors display

**HWM:** When HWM=1, data can be written to the GRAM at high speed. In high-speed write mode, four words of data are written to the GRAM in a single operation after the writing to RAM four times. Write to RAM less than four times, otherwise the four words cannot be written to the GRAM. Thus, set the lower 2 bits to 0 when setting the RAM address. For details, see the High-Speed RAM Write Mode section.

**I/D1-0:** When I/D1-0 = "1", the address counter (AC) is automatically incremented by 1 after the data is written to the GRAM. When I/D1-0 = "0", the AC is automatically decremented by 1 after the data is written to the GRAM. The increment/decrement setting of the address counter by I/D1-0 is done independently for the upper (AD15-8) and lower (AD7-0) addresses. The AM bit sets the direction of moving through the addresses when the data is written to GRAM.

**AM:** Set the automatic update method of the AC after the data is written to the GRAM. When AM= "0", the data is continuously written horizontally. When AM = "1", the data is continuously written vertically. When window address range is specified, the GRAM in the window address range can be written to according to the I/D1-0 and AM settings.

Note: SPR 1/0 bit must be set before writing data into display RAM. After writing data into display RAM, displaying color mode can not be changed by changing SPR1/0 bit.

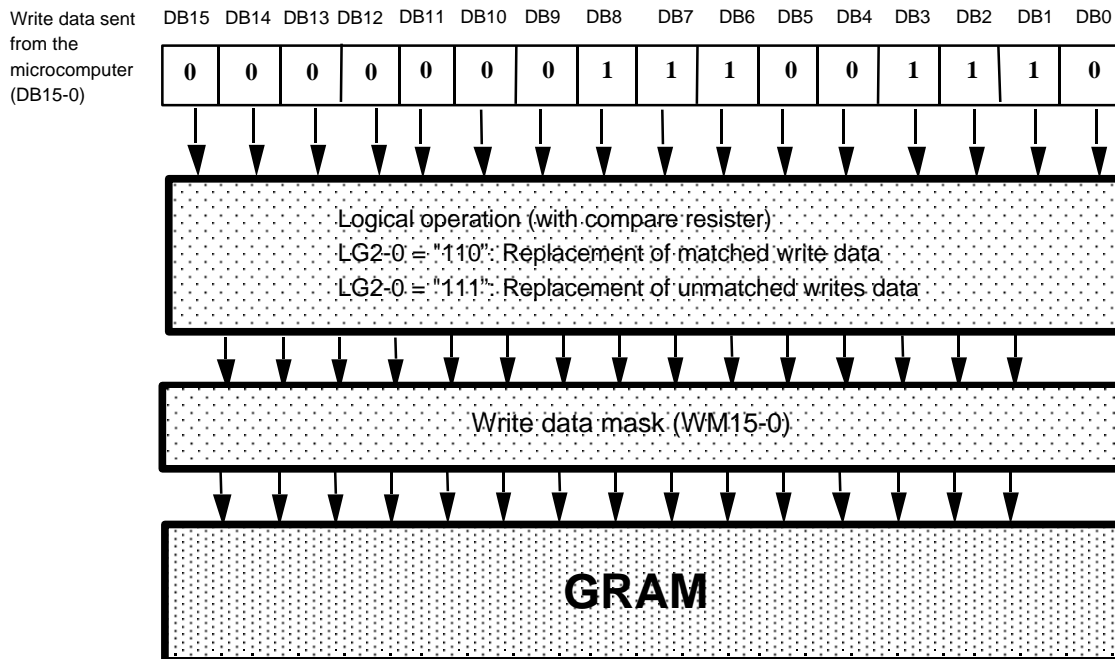


Note: When a window address range has been set the GRAM can only be written to within that range.

Figure18 Address Direction Settings

**LG2-0:** Compare the data written into the GRAM by the microcomputer with the compare registers (CP15-0) by a compare/logical operation and writes the results to GRAM. For details, see the Logical/Compare Operation Function.

**CP15-0:** Set the compare register for the compare operation with the data read from the GRAM or written by the microcomputer.



Note: The write data mask ( WM15-0 ) is set by the resister in the (20) RAM Write Data Mask section.

**Figure 19 Logical/Compare Operation for the GRAM**

9-11. Display Control (R07h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	VLE2	VLE1	SPT	0	0	0	0	B/W	REV	D1	D0

Figure 20 Display Control

**VLE2-1:** When VLE1 = “1”, a vertical scroll is performed in the 1<sup>st</sup> screen. When VLE2 = “1”, a vertical scroll is performed in the 2<sup>nd</sup> screen. Vertical scrolling on the two screens can be independently controlled.

**SPT:** When SPT = “1”, the 2-division LCD drive is performed. For details, see the Screen-division Driving Function section.

**B/W:** When B/W = “1”, displayed data can be “all on” or “all off” regardless GRAM contents. (B/W = “1”, REV = “0”: all pixel on, B/W = “1”, REV = “1”: all pixel off) When switching B/W, grayscale palette has to be default value.

**REV:** Displays all character and graphics display sections with reversal when REV = “1”. For details, see the Reversed Display Function section. Since the grayscale level can be reversed, display of the same data is enabled on normally-white and normally-black panels.

**D1-0:** Display is on when D1 = “1” and off when D1 = “0”. When off, the display data remains in the GRAM, and can be displayed instantly by setting D1 = “1”. When D1 = “0”, the display is off with all of the SEG/COM pin outputs set to the GND level. Because of this, the HD66768 can control the charging current for the LCD with AC driving.

When D1-0 = “01”, the internal display of the HD66768 is performed although the display is off. When D1-0 = “00”, the internal display operation halts and the display is off.

Table 17 D Bits and Operation

HD66768 Internal Display			
D1	D0	SEG/COM Output	Operation
0	0	GND	Halt
0	1	GND	Operate
1	0	Unlit display	Operate
1	1	Display	Operate

- Notes:
1. Writing from the microcomputer to the GRAM is independent from the state of D1-0.
  2. In the sleep and standby modes, it is the same status as D1-0 = “00”. However, the register contents of D1-0 are not modified.

9-12. Frame Cycle Control (R0Bh)

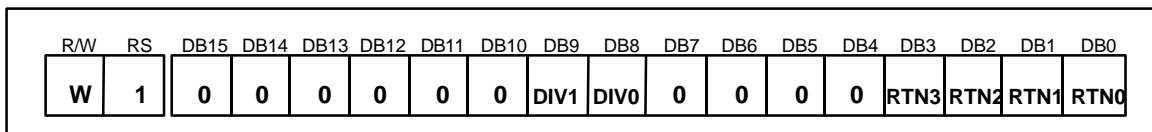


Figure 21

**RTN3-0:** Set the line retrace period (RTN3-0) to be added to raster-row cycles. The raster-row cycle becomes long according to the number of clocks set at RTN3-0.

**DIV1-0:** Set the division ratio of clocks for internal operation (DIV1-0). Internal operations are driven by clocks which are frequency divided according to the DIV1-0 setting. Frame frequency can be adjusted along with the line retrace period (RTN3-0). When changing the drive-duty, adjust the frame frequency. For details, see the Frame Frequency Adjustment Function section.

Table 18 RTN Bits and Clock Cycles

RTN3	RTN2	RTN1	RTN0	Line retrace period (Clock Cycles)	Clock Cycles per one raster-row
0	0	0	0	0 clock	25 clock
0	0	0	1	1 clock	26 clock
0	0	1	0	2 clock	27 clock
0	0	1	1	3 clock	28 clock
:	:	:	:	:	:
1	1	1	0	14 clock	39 clock
1	1	1	1	15 clock	40 clock

Table 19 DIV Bits and Clock Frequency

DIV1	DIV0	Division ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

\* fosc=R-C oscillation frequency

Formula for the frame frequency

Frame frequency =  $\frac{fosc}{\text{Clock cycles per raster-row} \times \text{division ratio} \times 1/\text{Duty}}$  [Hz]

fosc: RC oscillation frequency  
 Duty: Drive duty (NL bit)  
 Division ratio: DIV bit  
 Clock cycles per raster-row: (RTN+25) clock

9-13. Vertical Scroll Control (R11h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10

Figure 22 Vertical Scroll Control Instruction

**VL17-10:** Specify the display-start raster-row at the 1<sup>st</sup> screen display for vertical smooth scrolling. Any raster-row from the first to 84th can be selected. After the 84th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL17-10) is valid only when VLE1 = "1". The raster-row display is fixed when VLE1 = "0". (VLE1 is the 1<sup>st</sup>-screen vertical-scroll enable bit.)

**VL27-20:** Specify the display-start raster-row at the 2<sup>nd</sup> screen display. The display-start raster-row (VL27-20) is valid only when VLE2 = "1". The raster-row display is fixed when VLE2 = "0". (VLE2 is the 2<sup>nd</sup> -screen vertical-scroll enable bit.)

Table 20

VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10	Display start line
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 <sup>st</sup> raster - row
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	2 <sup>nd</sup> raster - row
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	3 <sup>rd</sup> raster - row
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	83rd raster - row
0	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	84th raster - row

Note: Do not set over the 84th ("53"H) raster - row

9-14. 1<sup>st</sup> Screen Driving Position (R14h)

9-15. 2<sup>nd</sup> Screen Driving Position (R15h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 23

**SS17–10:** Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value + 1' common driver.

**SE17–10:** Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SS17–10 = “07”H and SE17–10 = “10”H are set, the LCD driving is performed from COM8 to COM17, and non-selection driving is performed from COM1 to COM7, COM18 and others. Ensure that SS17–10 ≤ SE17–10 ≤ “53”H. For details, see the Screen-division Driving Function section.

**SS27–20:** Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' common driver. The second screen is driven when SPT = “1”.

**SE27–20:** Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SPT = “1”, SS27–20 = “20”H, and SE27–20 = “53”H are set, the LCD driving is performed from COM33 to COM84. Ensure that SS17–10 ≤ SE17–10 < SS27–20 ≤ SE27–20 ≤ “53”H. For details, see the Screen-division Driving Function section.

9-16. Horizontal RAM Address Position (R16h)

9-17. Vertical RAM Address Position (R17h)

RAW	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Figure 24 Horizontal/Vertical RAM Address Position Instruction

**HSA7-0/HEA7-0:** Specify the horizontal start/end positions of a window for access in GRAM. Data can be written to the GRAM until the address specified by HEA7-0 from the address specified by HSA7-0. Note that an address must be set before RAM is written to. Ensure  $00h \leq HSA7-0 \leq HEA7-0 \leq 67h$

**VSA7-0/VEA7-0:** Specify the vertical start/end positions of a window for access in GRAM. Data can be written to the GRAM until the address specified by VEA7-0 from the address specified by VSA7-0. Note that an address must be set before RAM is written to. Ensure  $00h \leq VSA7-0 \leq VEA7-0 \leq 53h$ .

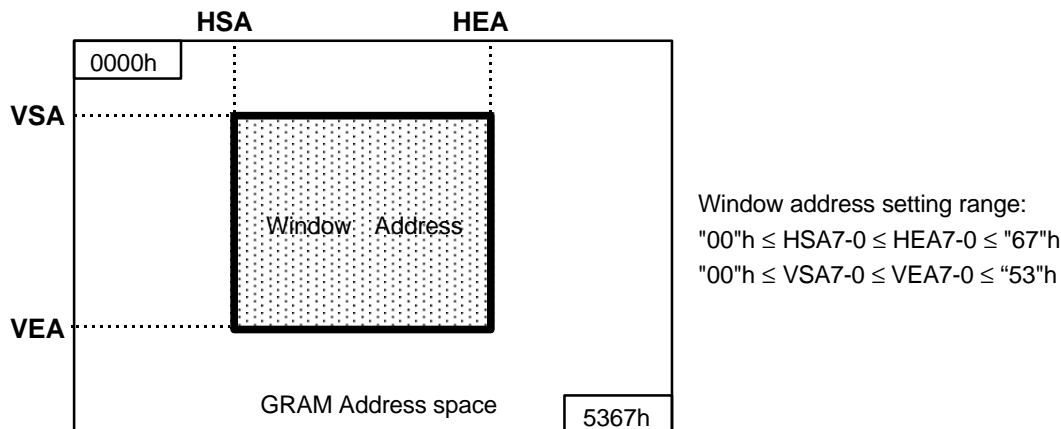


Figure 25 Window Address Setting Range

- Note:
1. Ensure that the window address area is within the GRAM address space.
  2. In high-speed write mode, data are written to GRAM in four-words.  
Thus, dummy write operations should be inserted depending on the window address area. For details, see the High-Speed Burst RAM Write Function section.

9-18. RAM Write Data Mask (R20h)

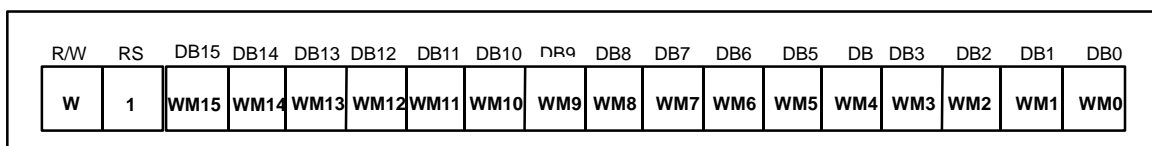


Figure 26 RAM Write Data Mask Instruction

**WM15–0:** In writing to the GRAM, these bits mask writing in a bit unit. When WM15 = “1”, this bit masks the write data of DB15 and does not write to the GRAM. Similarly, the WM14 to 0 bits mask the write data of DB14 to 0 in a bit unit. For details, see the Write Data Mask Function section.

9-19. RAM Address Set (R21h)

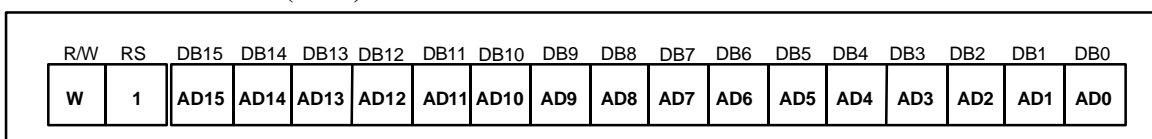


Figure 27 RAM Address Set Instruction

**AD15–0:** Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting addresses. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address.

Table 21 GRAM Address Range

AD15 to AD0	GRAM Setting
"0000"H to "0067"H	Bitmap data for COM1
"0100"H to "0167"H	Bitmap data for COM2
"0200"H to "0267"H	Bitmap data for COM3
"0300"H to "0367"H	Bitmap data for COM4
⋮	⋮
"5000"H to "5067"H	Bitmap data for COM81
"5100"H to "5167"H	Bitmap data for COM82
"5200"H to "5267"H	Bitmap data for COM83
"5300"H to "5367"H	Bitmap data for COM84

9-20. Write Data to GRAM (R22h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0

Figure 28 Write Data to GRAM Instruction

**WD15-0:** Write 16-bit data into GRAM. This data calls each grayscale palette. After a write, the address is automatically updated according to the AM and I/D bit settings. During the stand by mode, the GRAM cannot be accessed.

Table 22

GRAM data setting					Grayscale palette
R4	R3	R2	R1	R0	
B4	B3	B2	B1	B0	
0	0	0	0	0	PK04-00
0	0	0	0	1	Middle grayscale between PK04-00 and PK14-10
0	0	0	1	0	PK14-10
0	0	0	1	1	Middle grayscale between PK14-10 and PK24-20
0	0	1	0	0	PK24-20
0	0	1	0	1	Middle grayscale between PK24-20 and PK34-30
0	0	1	1	0	PK34-30
0	0	1	1	1	Middle grayscale between PK34-30 and PK44-40
0	1	0	0	0	PK44-40
0	1	0	0	1	Middle grayscale between PK44-40 and PK54-50
0	1	0	1	0	PK54-50
0	1	0	1	1	Middle grayscale between PK54-50 and PK64-60
0	1	1	0	0	PK64-60
0	1	1	0	1	Middle grayscale between PK64-60 and PK74-70
0	1	1	1	0	PK74-70
0	1	1	1	1	Middle grayscale between PK74-70 and PK84-80
			⋮		
1	1	1	0	0	PK144-140
1	1	1	0	1	Middle grayscale between PK144-140 and PK154-150
1	1	1	1	0	PK154-150
1	1	1	1	1	PK154-150

Table 23

GRAM data setting						Grayscale palette
G5	G4	G3	G2	G1	G0	
0	0	0	0	0	0	PK04-00
0	0	0	0	0	1	1/4 grayscale between PK04-00 and PK14-10
0	0	0	0	1	0	1/2 grayscale between PK04-00 and PK14-10
0	0	0	0	1	1	3/4 grayscale between PK04-00 and PK14-10
0	0	0	1	0	0	PK14-10
0	0	0	1	0	1	1/4 grayscale between PK14-10 and PK24-20
0	0	0	1	1	0	1/2 grayscale between PK14-10 and PK24-20
0	0	0	1	1	1	3/4 grayscale between PK14-10 and PK24-20
0	0	1	0	0	0	PK24-20
0	0	1	0	0	1	1/4 grayscale between PK24-20 and PK34-30
0	0	1	0	1	0	1/2 grayscale between PK24-20 and PK34-30
0	0	1	0	1	1	3/4 grayscale between PK24-20 and PK34-30
0	0	1	1	0	0	PK34-30
0	0	1	1	0	1	1/4 grayscale between PK34-30 and PK44-40
0	0	1	1	1	0	1/2 grayscale between PK34-30 and PK44-40
0	0	1	1	1	1	3/4 grayscale between PK34-30 and PK44-40
⋮						
1	1	1	1	0	0	PK144-140
1	1	1	1	0	1	1/4 grayscale between PK144-140 and PK154-150
1	1	1	1	1	0	1/2 grayscale between PK144-140 and PK154-150
1	1	1	1	1	1	3/4 grayscale between PK144-140 and PK154-150
1	1	1	1	0	0	PK154-150
1	1	1	1	0	1	PK154-150
1	1	1	1	1	0	PK154-150
1	1	1	1	1	1	PK154-150

9-21. Read Data from GRAM (R22h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	1	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure 29 Read Data from GRAM Instruction

**RD15-0:** When interface is 80system 8-bit parallel, read 16-bit data from the GRAM. When the data is read to the microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB7-0) becomes invalid and the second-word read is normal.

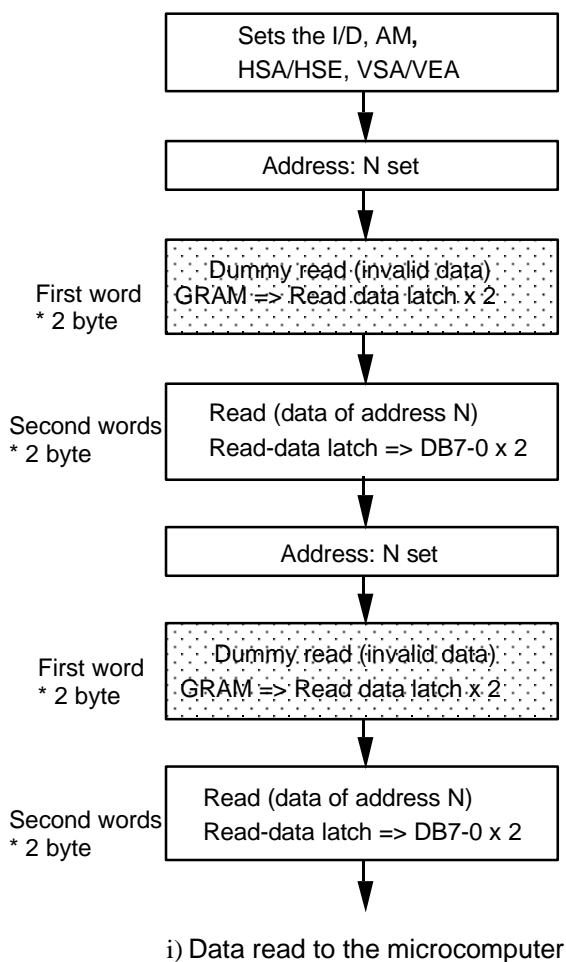


Figure 30 GRAM Read Sequence

9-22. Gray Scale Palette Control (R30h to R37h)

Table 24 Grayscale Palette Control Instruction

	R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R30	W	1	0	0	0	PK 14	PK 13	PK 12	PK 11	PK 10	0	0	0	PK 04	PK 03	PK 02	PK 01	PK 00
R31	W	1	0	0	0	PK 34	PK 33	PK 32	PK 31	PK 30	0	0	0	PK 24	PK 23	PK 22	PK 21	PK 20
R32	W	1	0	0	0	PK 54	PK 53	PK 52	PK 51	PK 50	0	0	0	PK 44	PK 43	PK 42	PK 41	PK 40
R33	W	1	0	0	0	PK 74	PK 73	PK 72	PK 71	PK 70	0	0	0	PK 64	PK 63	PK 62	PK 61	PK 60
R34	W	1	0	0	0	PK 94	PK 93	PK 92	PK 91	PK 90	0	0	0	PK 84	PK 83	PK 82	PK 81	PK 80
R35	W	1	0	0	0	PK 114	PK 113	PK 112	PK 111	PK 110	0	0	0	PK 104	PK 103	PK 102	PK 101	PK 100
R36	W	1	0	0	0	PK 134	PK 133	PK 132	PK 131	PK 130	0	0	0	PK 124	PK 123	PK 122	PK 121	PK 120
R37	W	1	0	0	0	PK 154	PK 153	PK 152	PK 151	PK 150	0	0	0	PK 144	PK 143	PK 142	PK 141	PK 140

**PK15-00:** Specify the grayscale level for 16 palettes from the 24-grayscale level. For details, see the Grayscale Palette and the Grayscale Palette Table sections.

9-23. E<sup>2</sup>PROM interface control (1) (R40h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R/W	1	0	0	0	TE	0	0	OP1	OP0	0	0	A5	A4	A3	A2	A1	A0

Figure 31

A5-0: Address of E<sup>2</sup>PROM.

OP1-0: Operation code of E<sup>2</sup>PROM.

TE: Transfer enable signal of E<sup>2</sup>PROM interface. When TE= “0”, transfer is available. When TE = “1”, transfer to E<sup>2</sup>PROM starts. When transfer ends, TE = “0”. Interval for more than 25 ms is necessary after finishing the transfer to E2PROM, because writing transferred data into E2PROM requires more than 25 ms. Refer to “E2PROM interface” for details.

Table 25

OP1	OP0	A5-0	Order
0	0	000000	Writing inhibited
0	0	110000	Writing available
0	1	000000-111111	Writing
1	0	000000-111111	Reading

9-24. E<sup>2</sup>PROM interface control (2) (R41h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	TD 15	TD 14	TD 13	TD 12	TD 11	TD 10	TD 9	TD 8	TD 7	TD 6	TD 5	TD 4	TD 3	TD 2	TD 1	TD 0

Figure 32

TD15-0: Transfer data of E2PROM.

9-25. E<sup>2</sup>PROM interface control (3) (R42h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	DPM	IDX 7	IDX 6	IDX 5	IDX 4	IDX 3	IDX 2	IDX 1	IDX 0

Figure 33

IDX7-0: Index of (HD66768) for setting data read from E2PROM.

DPM: Data can be written into the index set by IDX7-0. When DPM = “1”, writing is available.

Note 1) Data of TD15-0 must be set as to be the same bit sequence as instruction of HD66768.

Note 2) It is inhibited to set more than “37h” to IDX7-0.

Instruction List (HD66768)

Table 26

Register No.	Register	Upper Code										Lower Code										Executing cycle	
		R/W	RS	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0				
IR	Index	0	0	*	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0		
SR	Status read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0	0			
R00h	Oscillation start	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	10ms		
	Device code read	1	1	0	0	0	0	0	0	1	1	1	0	1	1	0	0	1	1	0	0		
R01h	Driver output control	0	1	0	0	0	0	0	CSFT	CMS	SGS	0	0	4L	NL4	NL3	NL2	NL1	NL0	0			
R02h	LCD operating alternation control	0	1	0	0	0	0	0	RST	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0	0			
R03h	Power control (1)	0	1	0	0	BS2	BS1	BS0	0	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB	0			
R04h	Contrast control	0	1	0	0	VRC NT	VR4	VR3	VR2	VR1	VR0	VRO N	CT6	CT5	CT4	CT3	CT2	CT1	CT0	0			
R05h	Entry mode	0	1	SPR1	SPR0	0	0	0	0	HW M	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0	0			
R06h	Compare resistor	0	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	0			
R07h	Display control	0	1	0	0	0	0	0	VLE2	VLE1	SPT	0	0	0	0	B/W	REV	D1	D0	0			
R08h	Flame cycle control	0	1	0	0	0	0	0	0	DIV1	DIV0	0	0	0	0	RTN 3	RTN 2	RTN 1	RTN 0	0			
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0	0			
R11h	Vertical scroll control	0	1	VL 27	VL 26	VL 25	VL 24	VL 23	VL 22	VL 21	VL 20	VL 17	VL 16	VL 15	VL 14	VL 13	VL 12	VL 11	VL 10	0			
R14h	First screen operating position	0	1	SE 17	SE 16	SE 15	SE 14	SE 13	SE 12	SE 11	SE 10	SE 17	SE 16	SE 15	SE 14	SE 13	SE 12	SE 11	SE 10	0			
R15h	Second screen operating position	0	1	SE 27	SE 26	SE 25	SE 24	SE 23	SE 22	SE 21	SE 20	SE 27	SE 26	SE 25	SE 24	SE 23	SE 22	SE 21	SE 20	0			
R16h	Horizontal RAM address position	0	1	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0	HAS 7	HAS 6	HAS 5	HAS 4	HAS 3	HAS 2	HAS 1	HAS 0	0			
R17h	Vertical RAM address position	0	1	VEA 7	VEA 6	VEA 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	0			
R20h	RAM write data mask	0	1	WM 15	WM 14	WM 13	WM 12	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0	0			
R21h	RAM address set	0	1	AD15-8 (Upper)										AD7-0 (Lower)									
R22h	RAM data write	0	1	Write Data (Upper)										Write Data (Lower)									
	RAM data read	0	1	Read Data (Upper)										Read Data (Lower)									
R30h	Grayscale palette control (1)	0	1	0	0	0	PK 14	PK 13	PK 12	PK 11	PK 10	0	0	0	PK 04	PK 03	PK 02	PK 01	PK 00	0			
R31h	Grayscale palette control (2)	0	1	0	0	0	PK 34	PK 33	PK 32	PK 31	PK 30	0	0	0	PK 24	PK 23	PK 22	PK 21	PK 20	0			
R32h	Grayscale palette control (3)	0	1	0	0	0	PK 54	PK 53	PK 52	PK 51	PK 50	0	0	0	PK 44	PK 43	PK 42	PK 41	PK 40	0			
R33h	Grayscale palette control (4)	0	1	0	0	0	PK 74	PK 73	PK 72	PK 71	PK 70	0	0	0	PK 64	PK 63	PK 62	PK 61	PK 60	0			
R34h	Grayscale palette control (5)	0	1	0	0	0	PK 94	PK 93	PK 92	PK 91	PK 90	0	0	0	PK 84	PK 83	PK 82	PK 81	PK 80	0			
R35h	Grayscale palette control (6)	0	1	0	0	0	PK 114	PK 113	PK 112	PK 111	PK 110	0	0	0	PK 104	PK 103	PK 102	PK 101	PK 100	0			
R36h	Grayscale palette control (7)	0	1	0	0	0	PK 134	PK 133	PK 132	PK 131	PK 130	0	0	0	PK 124	PK 123	PK 122	PK 121	PK 120	0			
R37h	Grayscale palette control (8)	0	1	0	0	0	PK 154	PK 153	PK 152	PK 151	PK 150	0	0	0	PK 144	PK 143	PK 142	PK 141	PK 140	0			
R40h	E2PROM interface control (1)	0/1	1	0	0	0	TE	0	0	OP1	OP0	0	0	A5	A4	A3	A2	A1	A0	0			
R41h	E2PROM interface control (2)	0	1	TD 15	TD 14	TD 13	TD 12	TD 11	TD 10	TD 9	TD 8	TD 7	TD 6	TD 5	TD 4	TD 3	TD 2	TD 1	TD 0	0			
R42h	E2PROM interface control (3)	0	1	0	0	0	0	0	0	0	DPM	IDX 7	IDX 6	IDX 5	IDX 4	IDX 3	IDX 2	IDX 1	IDX 0	0			

Note: 1. "\*" means doesn't matter.

2. High-speed write mode is available only for the RAM writing.

**Reset Function**

The HD66768 is internally initialized by RESET input. The reset input must be held for at least 200  $\mu$ s. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

**Instruction Set Initialization:**

1. Start oscillation executed
2. Driver output control (CSFT = "0", 4L = "0", NL4-0 = "01010", SGS = "0", CMS = "0")
3. B-pattern waveform AC drive (B/C = "0", EOR = "0", NW5-0 = "000000")
4. Power control 1 (DC2-0 = "000", AP2-0 = "000": LCD power off, STB = "0": Standby mode off, SLP = "0", BS2-0 = "000", BT2-0 = "000")
5. Contrast control (Weak contrast VRCNT = "0", VR2-0 = "000", VRON = "0", CT6-0 = "0000000")
6. Entry mode set ( SPR1-0 = "00", HWM = "0", I/D1-0 = "11": Increment by 1, AM = "0": Horizontal move, LG2-0="000":Replace mode )
7. Compare resistor : (CP15-0 = "0000H")
8. Display control (VLE2-1 = "00": No vertical scroll, SPT = "0", B/W: "0" = ALL off, REV = "0", D1-0 = "00": Display off)
9. Frame cycle control (DIV1-0 = "00": 1-divided clock, RTN3-0: No line retrace period)
10. Power control 2 (VC2-0 = "000")
11. Vertical scroll (VL27-20 = "00000000", VL17-10 = "00000000")
12. 1st screen division (SE17-10 = "11111111", SS17-10 = "00000000")
13. 2nd screen division (SE27-20 = "11111111", SS27-20 = "00000000")
14. Horizontal RAM address position (HEA7-0 = "0110011", HSA7-0 = "00000000")
15. Vertical RAM address position (VEA7-0 = "01010011", VSA7-0 = "00000000")
16. RAM write data mask (WM15-0 = "000"H: No mask)
17. RAM address set (AD15-0 = "0000"H)
18. Grayscale Palette  
(PK0 = "0000", RK1 = "00011", PK2 = "00101", PK3 = "00111",  
PK4 = "01000", PK5 = "01001", PK6 = "01010", PK7 = "01011",  
PK8 = "01100", PK9 = "01101", PK10 = "01110", PK11 = "01111",  
PK12 = "10001", PK13 = "10011", PK14 = "10110", PK15 = "11001")
19. E2PROM interface control (1) (TE = "0", OP1-0 = "00", A5-0 = "00000")
20. E2PROM interface control (2) (TD15-0 = "0000"H)
21. E2PROM interface control (3) (DPM = "0", IDX7-0 = "00"H)

**GRAM Data Initialization:**

This is not automatically initialized by reset input but must be initialized by software while display is off (D1-0 = "00").

**Output Pin Initialization:**

1. LCD driver output pins (SEG/COM): Output GND level
2. Oscillator output pin (OSC2): Output oscillation signal

### 10. Parallel Data Transfer

#### 1) 8-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the “GND”/“Vcc”/“Vcc” level allows 80-system bit parallel data transfer with DB7 to DB0 pins. HD66768 separates 16-bit instruction and RAM data into upper 8-bit and lower 8-bit, and upper 8-bit are transferred first.

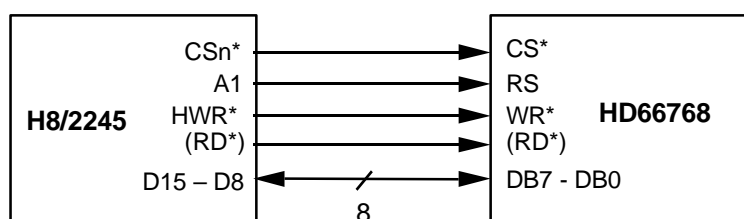


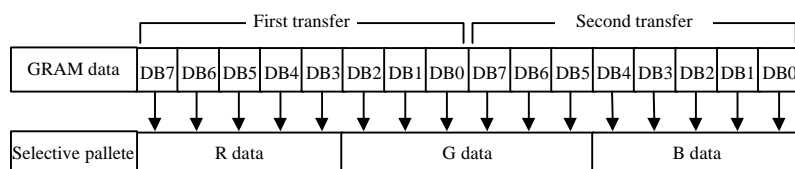
Figure 34 Interface to 8-bit Microcomputer

#### 2) Data format of 8-bit Bus Interface

HD66768 is equipped with three colors display modes; 65,000 color display, 4,096 color display mode, and 256 color display mode. Display data format of 65,000 color mode is 16-bit, and data should be transferred by every two-bytes from MSB. When SPR1-0 = “01”, HD66768 displays 4,096 colors. Display data format is consist of 12 bit and data should be transferred by every three-bytes from MSB. When SPR1-0 = “10”, HD66768 display 256 colors. Display data format is consist of 8 bit and data should be transferred by every one-byte from MSB. Data fiormat of data register except index and GRAM is consist of 16-bit and data should be transferred by every two-bytes from MSB.

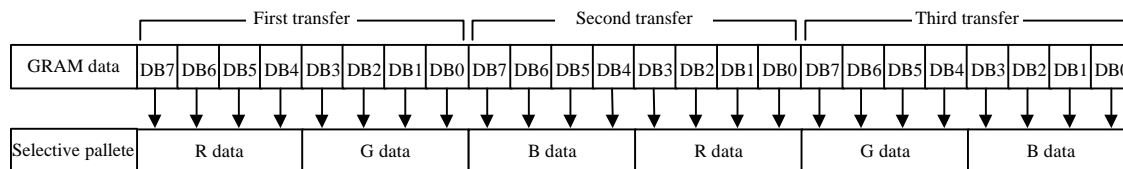
SPR1/0 = “00” 65K colors mode

Figure 35



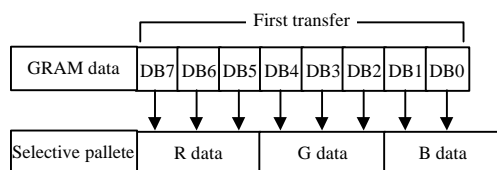
SPR1/0 = “01” 4,096 colors mode

Figure 36



SPR1/0 = “10” 256 colors mode

Figure 37



Note: Transfer synchronization function for an 8-bit bus interface

The HD66768 supports the transfer synchronization function that resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a "00"H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

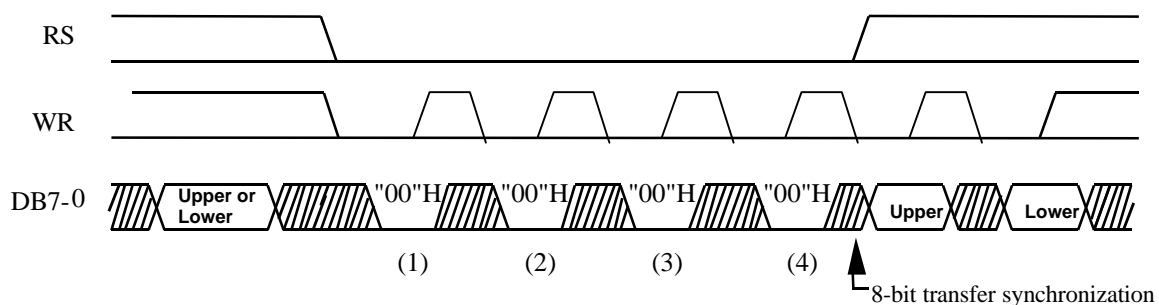


Figure 38 8-bit Transfer Synchronization

## 11. Serial Data Transfer

### Serial Interface

HD66768 has two types of clock synchronized serial interface. When IM2 pin is fixed to Vcc and IM1 pin is fixed to GND, HD66768 selects clock synchronized 3 lines serial interface. When IM2 pin is fixed to Vcc, IM1 pin to Vcc, and IM0 pin to GND, HD66768 selects clock synchronized four lines serial interface. Three lines and Four lines serial interface are only for writing data, and they can not be used for status read nor reading data from display RAM.

#### 1) Three lines serial interface

Setting the IM2 pin to the “Vcc” level and the IM1 pin to the “GND” level allows three lines clock-synchronized serial data transfer, using the chip select line (CS\*), serial transfer clock line (SCL), serial input data line (SDI). For a serial interface, the IM0/ID pin is used as an ID pin. If HD66768 is set up for serial interface, the DB7-2 pins, which are not used, must be fixed at “Vcc” or “GND”.

The HD66768 initiates serial data transfer by transferring the start byte at the falling edge of CS\* input. It ends serial data transfer at the rising edge of CS\* input.

The HD66768 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66768. Selected HD66768 receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The upper five bits must be “01110”. Because the seventh bit of the start byte is used as a resistor select bit (RS): that is, when RS = “0”, data can be written to the index resistor, and when RS = “1”, an instruction can be issued or data can be written to RAM.

After receiving the start byte, the HD66768 receives the subsequent data byte-by-byte. The data is transferred with the MSB first. All HD66768 instructions are 16 bits. Two bytes are received with the MSB first, and then the instructions are internally executed.

#### Start byte format

**Table 27**

Example of transfer bit	S	1	2	3	4	5	6	7	8
Start byte format	Start	Device ID code					ID	RS	0
		0	1	1	1	0			

#### RS bit function

**Table 28**

RS	Function
0	Index register setting
1	Instruction write RAM data writing

a) Timing of basic data-transfer through three lines system clock synchronized serial interface

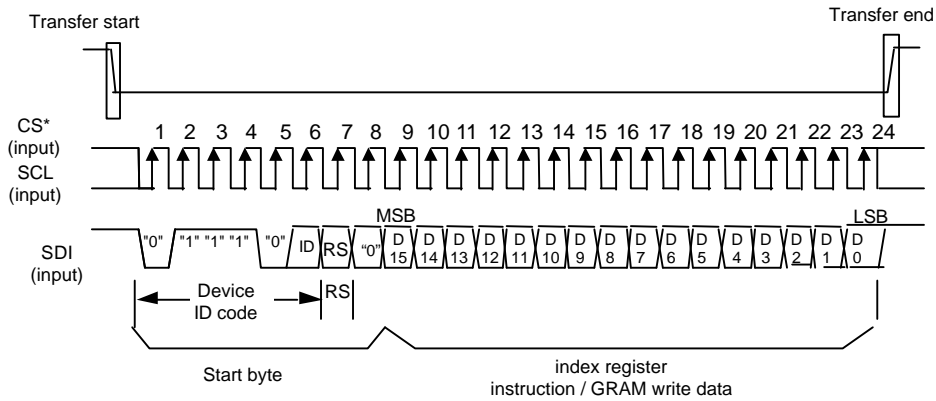


Figure 39: Procedure for transfer through the clock synchronized serial interface (a)

b) Timing of consecutive data transfer through three lines system clock synchronized serial interface

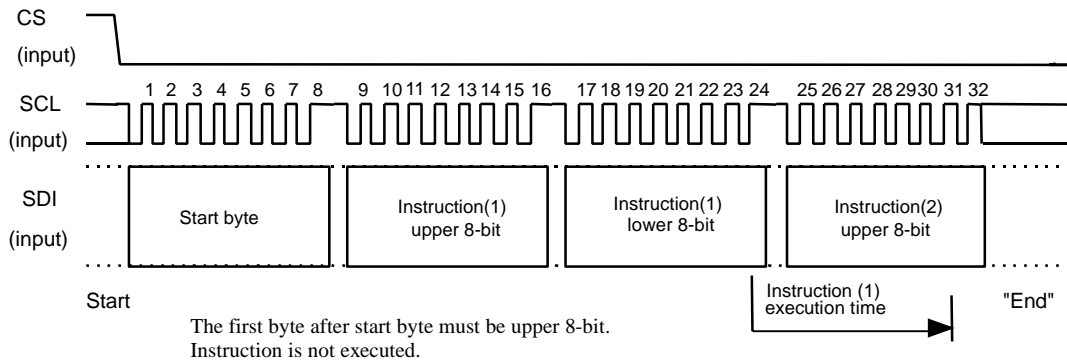


Figure 40: Procedure for transfer through the clock synchronized serial interface (b)

2) Four lines serial interface

Setting the IM2 pin to the “Vcc” level, the IM1 pin to the “Vcc” level, and IM0 pin to “GND” level allows 4 lines serial data transfer, using the chip select line (CS\*), register select line (RS\*), serial transfer clock line (SCL), and serial input data line (SDI). If HD66768 is set up for serial interface, the DB7-2 pins, which are not used, must be fixed at “Vcc” or “GND” level.

The HD66768 initiates serial data transfer by transferring the start byte at the falling edge of CS\* input, and receives the subsequent data string. It ends serial data transfer at the rising edge of CS\* input. HD66768 receives register select line (RS\*) at the eighth rising edge of transfer clock line (SCL). HD66768 should receive register select line (RS\*) every one byte. When RS = “0”, data can be written to the index register, and when RS = “1”, an instruction can be issued or data can be written to RAM. At the falling edge of CS\* input, HD66768 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first.

RS terminal function

Table 29

RS	Function
0	Index register setting
1	Instruction write RAM data writing

a) The basic transfer of four lines system clock synchronized transfer

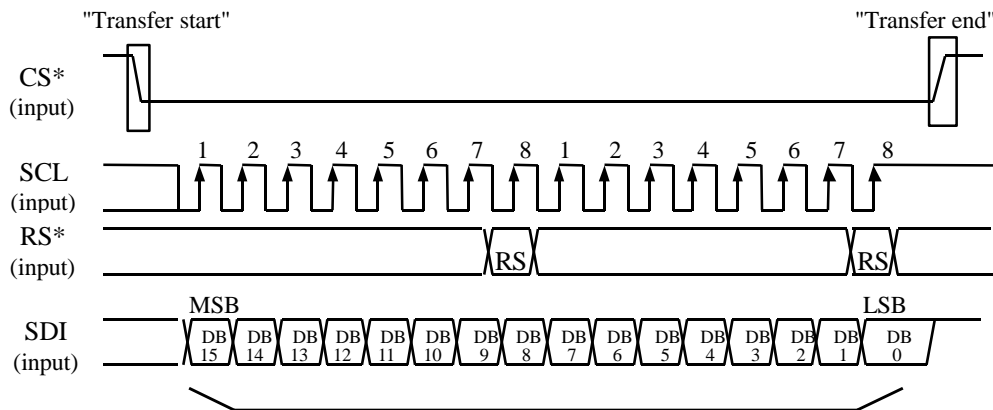


Figure 41 Index register set, Instruction, RAM data

3) Data format of Serial Interface (Common to Three lines and Four lines serial interface)

HD66768 has three types of color display mode. 65,000 colors, 4,096 colors display mode, and 256 colors display mode. When SPR1-0 = "00", displays 65,000 colors format. Display data format is 16 bit. Transfer data by every two bytes from MSB. When SPR1-0 = "01", displays 4,096 colors. Display data format is twelve bit. Transfer data by every three bytes from MSB. When SPR1-0 = "10", displays 256 colors. Display data format is 8 bit. Transfer data by every one byte from MSB. Data format of data register except index and GRAM is consist of 16-bit and data should be transferred every two-bit.

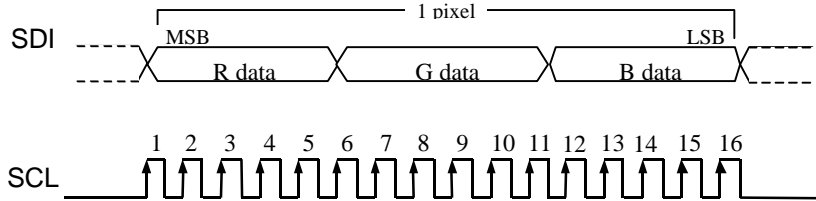
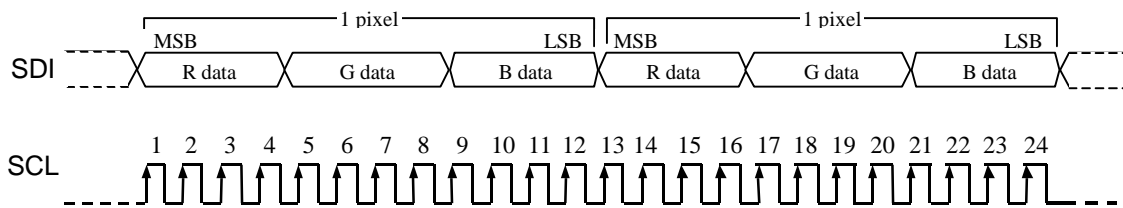


Figure 42 Data format of 65k colors display mode



\* The pixel number of writing to display RAM must be odd number.

Figure 43 Write data format of 4,096 colors display mode

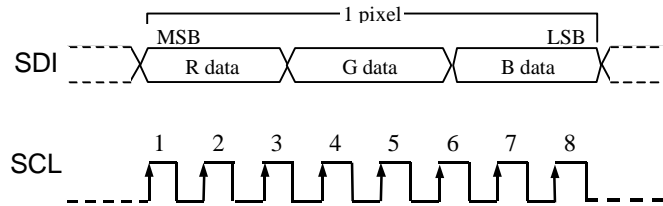


Figure 44 Write data format of 256 colors display mode

4) Setting of instruction register and access to display RAM

After setting index and instructions, do not continuously access to display RAM with CS remaining at low because data format varies according to display color mode. Also after accessing to RAM, do not continuously set index and instructions with CS remaining at low. Once CS must be set to high and released, then reset CS. Before accessing to RAM, set CS to low, set index (R22), set CS to high, and set CS to low again.

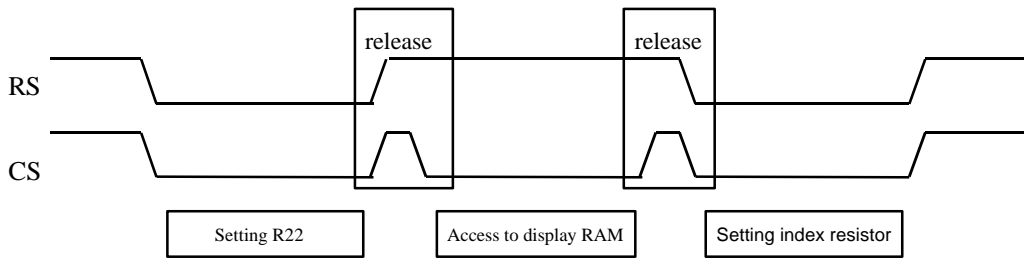


Figure 45: Example of setting instruction register and access to display RAM

### 12. High-Speed Burst RAM Write Function

The HD66768 has a high-speed burst RAM-write function that can be used to write data to RAM in one-fourth the access time required for an equivalent standard RAM-write operation. This function is especially suitable for applications that require the high-speed rewriting of the display data, for example, display of color animations, etc.

When the high-speed RAM-write mode (HWM="1") is selected, data for writing to RAM is once stored to the HD66768 internal register. When data is selected eight times per word, all data is written to the RAM. While this is taking place, the next data can be written to an internal register so that high-speed and consecutive RAM writing can be executed for animated displays, etc.

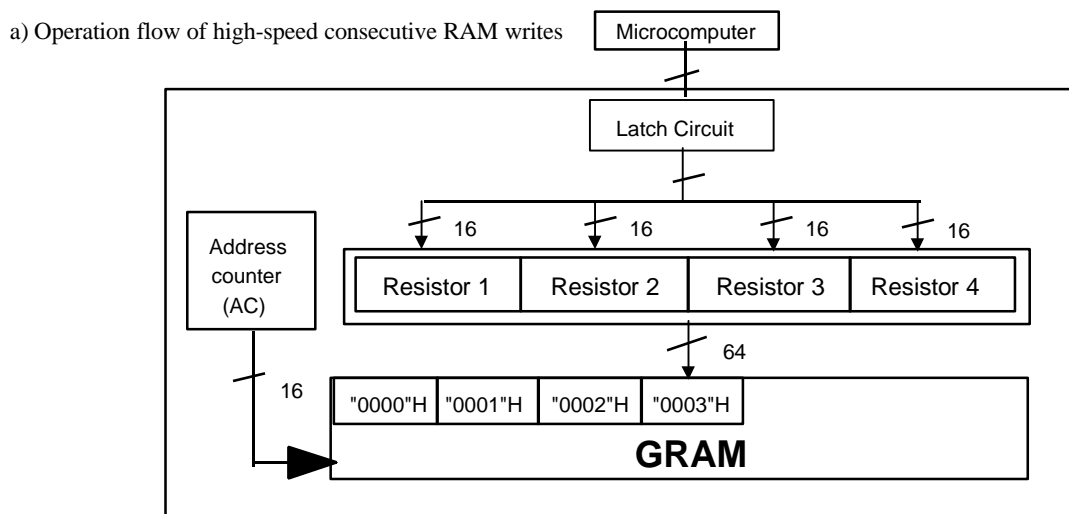
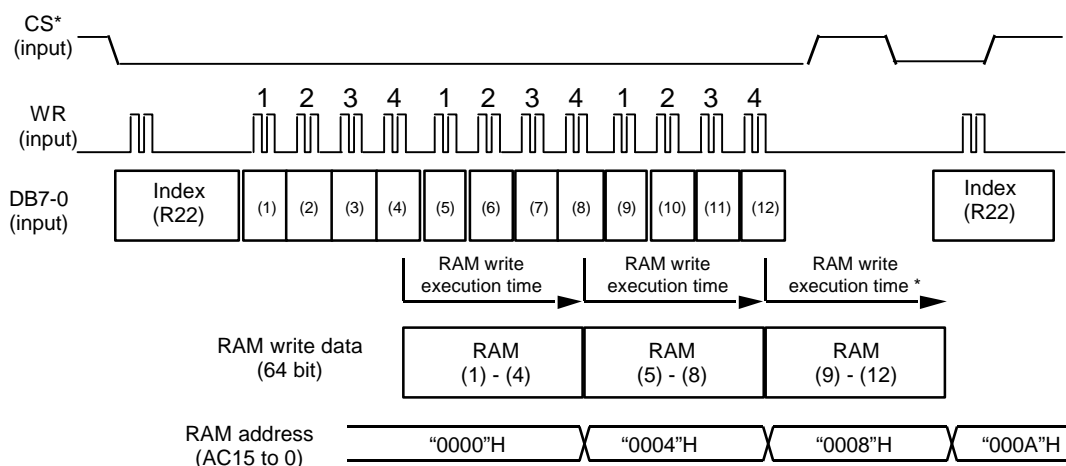


Figure 46 Flow of Operation in High-Speed Consecutive Writing to RAM

b) Example of the operation of high-speed consecutive writing to RAM (HWM = "1")

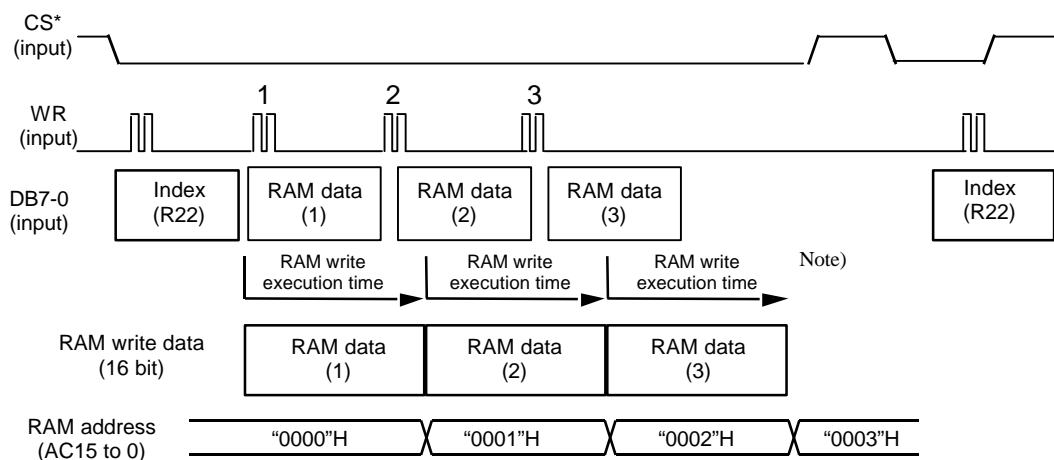


\* The lower two bits of the address must be set in the following way in high-speed write mode.  
 When D0 = "0", the lower two bits of the address must be set to "11".  
 When D1 = "1", the lower two bits of the address must be set to "00".

Note: When a high-speed RAM write is canceled, the next instruction must only be executed after the RAM write execution time has elapsed.

Figure 47 Example of the Operation of High-Speed Consecutive Writing to RAM (HWM = "1")

c) Example of the operation of normal writing to RAM (HWM = "0")



Note the following when using high-speed RAM write mode.

**Figure 48 Example of the Operation of Normal Writing to RAM (HWM = "0")**

- Notes:
1. The logical and compare operation cannot be used.
  2. Data is written to RAM each four words. When an address is set, the lower two bits in the address must be set to the following values.
    - \*When I/D0=0, the lower two bits in the address must be set to "11" and be written to RAM.
    - \*When I/D0=1, the lower two bits in the address must be set to "00" and be written to RAM.
  3. Data is written to RAM each four words. If less than four words of data are written to RAM, the last data will not be written to RAM.
  4. When the index register and RAM data write ("22"H) have been selected, the data is always written first. RAM cannot be written to and read from at the same time. HWM must be set to "0" when RAM is being read.
  5. High-speed and normal RAM write operations cannot be executed at the same time. The mode must be switched and the address must then be set.
  6. When high-speed RAM write is used with a window address-range specified, dummy write operation may be required to suit the window address range-specification. Refer to the High-Speed RAM Write in the Window Address section.

Table 30 Comparison between Normal and High-Speed RAM Write Operations

	Normal RAM Write (HWM= "0")	High-Speed RAM Write (HWM= "1")
Logical operation function	Can be used	Cannot be used
Compare operation function	Can be used	Cannot be used
Write mask function	Can be used	Can be used
RAM address set	Can be specified by word	ID0 bit=0: Set the lower two bits to "11" ID0 bit=1: Set the lower two bits to "00"
RAM read	Can be read by word	Cannot be used
RAM write	Can be written by word	Can be set by four words
Window address	Can be set by word	Dummy write operations may have to be inserted according to a window address-range specification

**High-Speed RAM Write in the Window Address**

When a window address range is specified, RAM data which is in an optional window area can be rewritten consecutively and quickly by inserting dummy write operations so that RAM access counts become  $4N$  as shown in the tables below.

Dummy write operations may have to be inserted as the first or last operations for a row of data, depending on the horizontal window-address range specification bits (HSA1-0, HEA1-0). The number of dummy writes operations of a row must be  $4N$ .

**Table 31 Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)**

HSA1	HSA0	Number of Dummy Write Operations to be Inserted at the Start of a Row
0	0	0
0	1	1
1	0	2
1	1	3

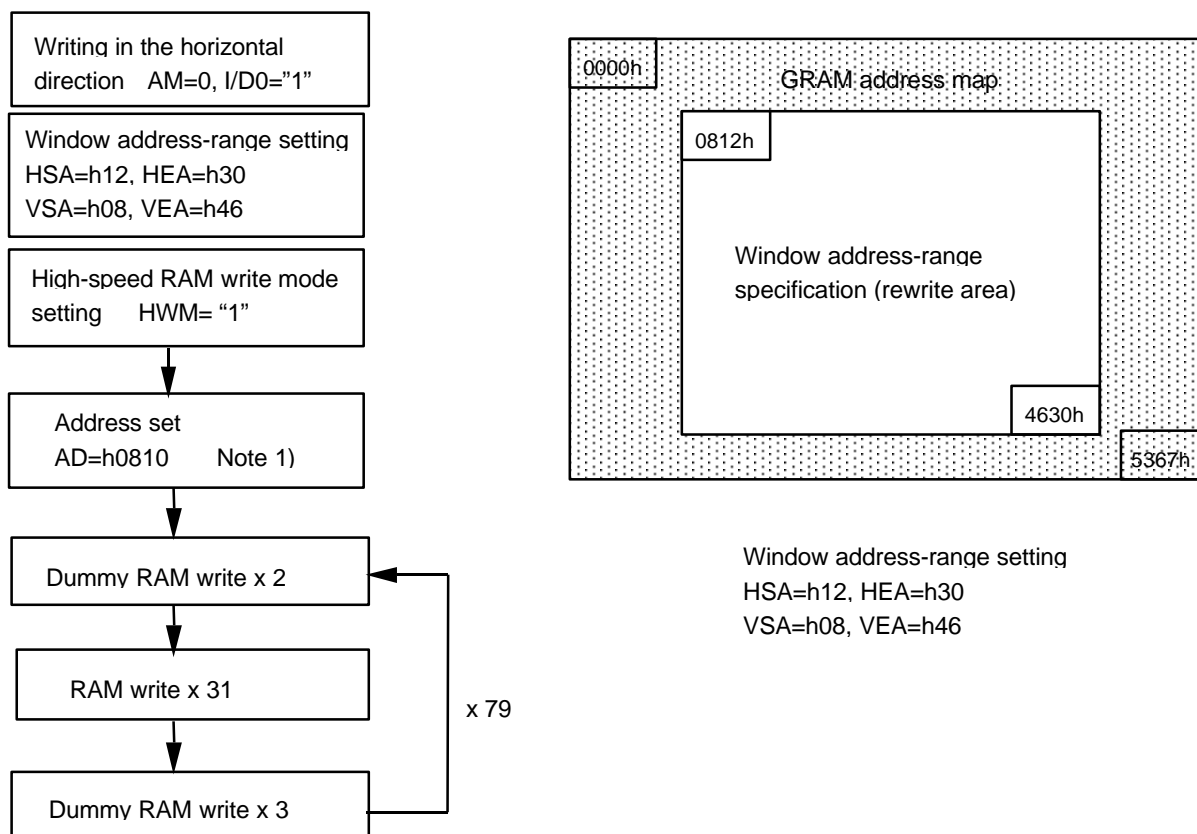
**Table 32 Number of Dummy Write Operations in High-Speed RAM Write (HEA Bits)**

HEA1	HEA0	Number of Dummy Write Operations to be Inserted at the End of a Row
0	0	3
0	1	2
1	0	1
1	1	0

Each row of access must consist of  $4 \times N$  operations, including the dummy writes.

Horizontal access count = first dummy write count + write data count + last dummy write count =  $4 \times N$

An example of high-speed RAM write with a window address-range specified is shown below. The window address-range can be rewritten to consecutively and quickly by inserting two dummy writes at the start of a row and three dummy writes at the end of a row, as determined by using the window address-range specification bits (HSA1-0= "10", HEA1-0= "00").



Note1) The address set for the high-speed RAM write must be "00" or "11" according to the value of I/D1-0 bit. Only RAM in the specified window address-range will be overwritten.

Figure 49 Example of the High-Speed RAM write with a window address-range specification

### 13. Window Address Function

When data is written to the on-chip GRAM, a window address-range which is specified by the horizontal address register (start: HSA7-0, end: HEA7-0) or the vertical address register (start: VSA7-0, end: VEA7-0) can be written to consecutively.

Data is written to addresses in the direction specified by the AM bit (increment/decrement). When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.

The window must be specified to be within the GRAM address area described below. Addresses must be set within the window address.

[Restriction on window address-range settings]

(horizontal direction) "00"H ≤ HSA7-0 ≤ HEA7-0 ≤ "67"H

(vertical direction) "00"H ≤ VSA7-0 ≤ VEA7-0 ≤ "53"H

[Restriction on address settings during the window address]

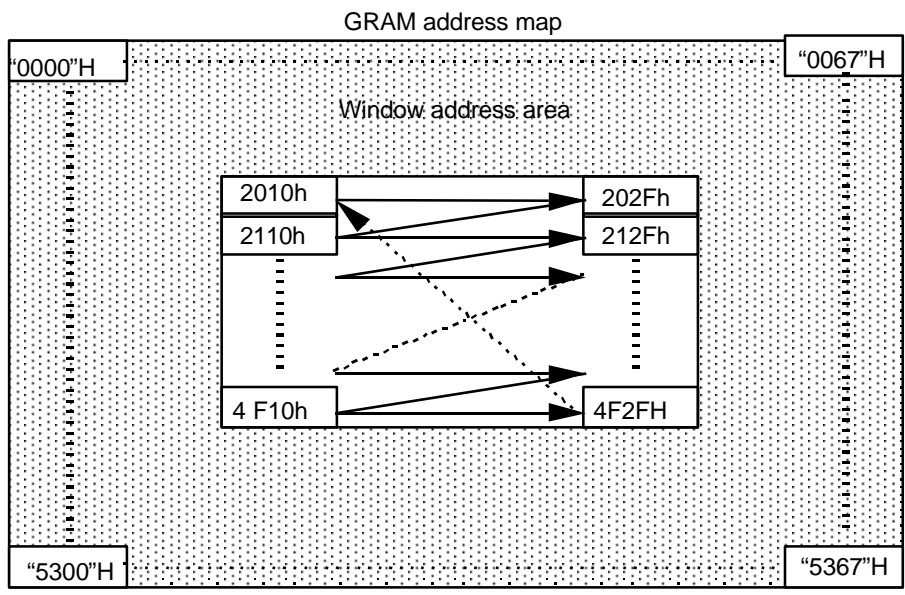
(RAM address) HSA7-0 ≤ AD7-0 ≤ HEA7-0

VSA7-0 ≤ AD15-8 ≤ VEA7-0

Note: In high-speed RAM-write mode, the lower two bits of the address must be set as shown below according to the value of the ID0 bit.

I/D0=0: The lower two bits of the address must be set to "11".

I/D0=1: The lower two bits of the address must be set to "00".



Window address-range specification area  
 HSA7-0="10"H, HEA7-0="2F"H      I/D0="1" (increment)  
 VSA7-0="20"H, VEA7-0="4F"H      AM="0" (horizontal writing)

Figure 50 Example of Address Operation in the Window Address Specification

### 14. Graphic Operation Function

The HD66768 can greatly reduce the load of the microcomputer graphics software processing through the 8-bit bus architecture and internal graphics-bit operation function. This function supports the following:

1. A write data mask function that selectively rewrites some of the bits in the 16-bit write data.
2. A conditional write function that compares the write data and compare-bit data and writes the data sent from the microcomputer only when the conditions match. Even if the display size is large, the display data in the graphics RAM ( GRAM ) can be quickly rewritten. The graphics bit operation can be controlled by combining the entry mode resister. The bit set value of the RAM-write –data mask resister, and the write from the microcomputer.

Operation Mode	Bit Setting			Operation and Usage
	I/D	AM	LG2-0	
Write mode 1	0 /1	0	000	Horizontal data replacement, horizontal - border drawing
Write mode 2	0 /1	1	000	Vertical data replacement, vertical - border drawing
Write mode 3	0 /1	0	110,111	Conditional horizontal data replacement, horizontal - border drawing
Write mode 4	0 /1	1	110,111	Conditional vertical data replacement, vertical - border drawing

Table 33 Graphics operation

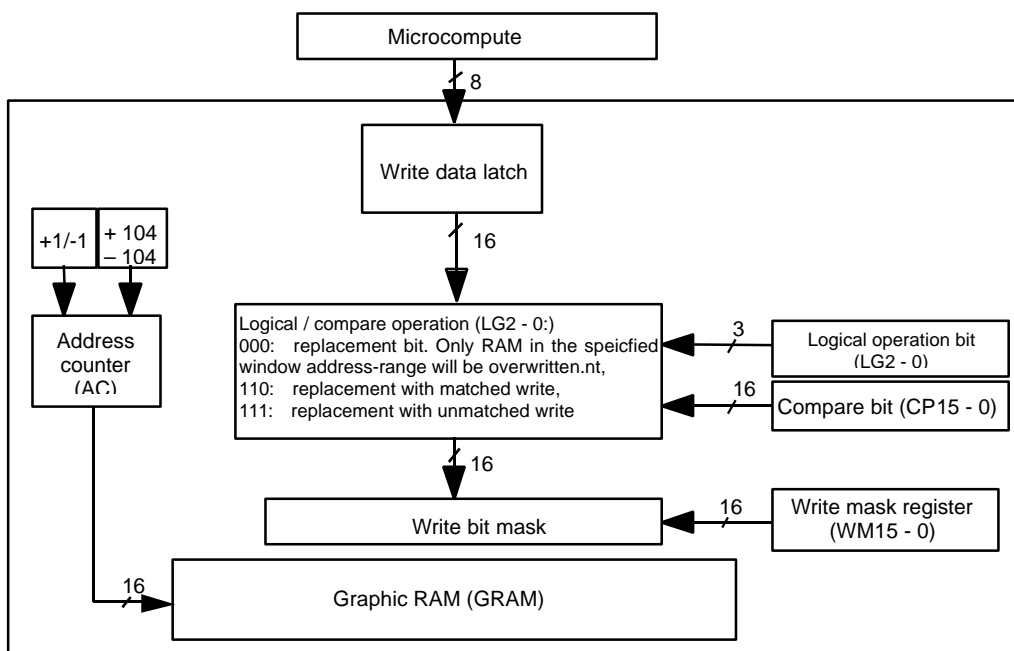
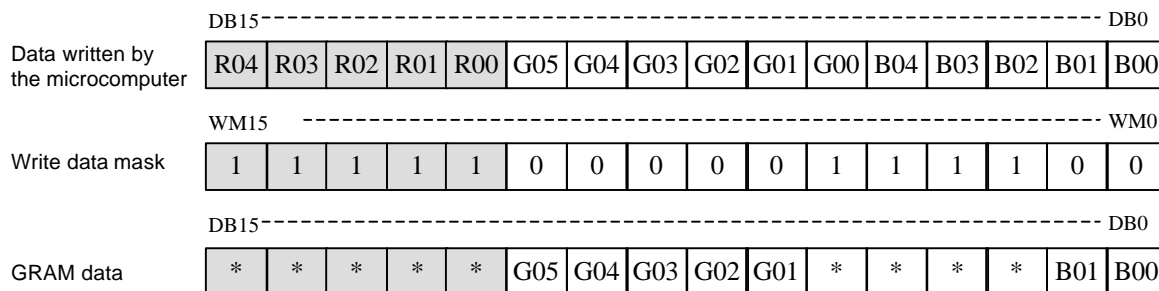


Figure 51 Graphics Operation flow

**Write-data Mask Function**

The HD66768 has a bit-wise write-data mask function that controls writing the 8-bit data from the microcomputer to the GRAM. Bits that are “0” in the write-data mask register (WM15-0) cause the corresponding DB bit to be written to the GRAM. Bits that are “1” prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is retained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.



**Figure 52 Write-data Mask Function Operation**

Graphics Operation Processing

1. Write mode 1: AM = "0", LG2-0 = "000"

This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The write-data mask function (WM15-0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster below after it has reached the left or right edge of the GRAM.

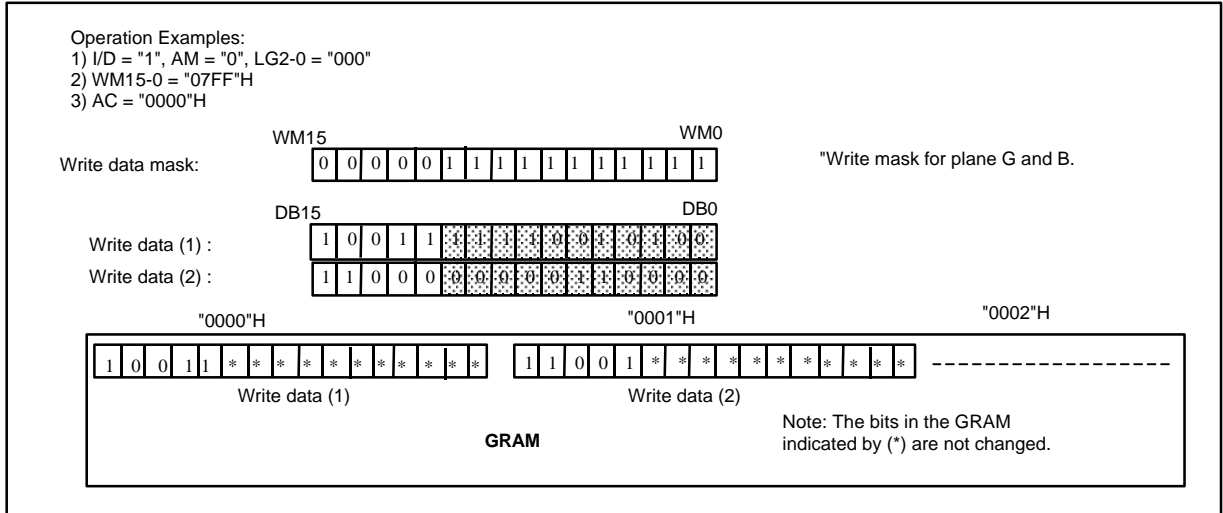


Figure 53 Writing Operation of Write Mode 1

2. Write mode 2: AM = "1", LG2-0 = "000"

This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The write-data mask function (WM15-0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1 ) or upper-left edge ( I/D = 0 ) following the I/D bit after it has reached the lower edge of the GRAM.

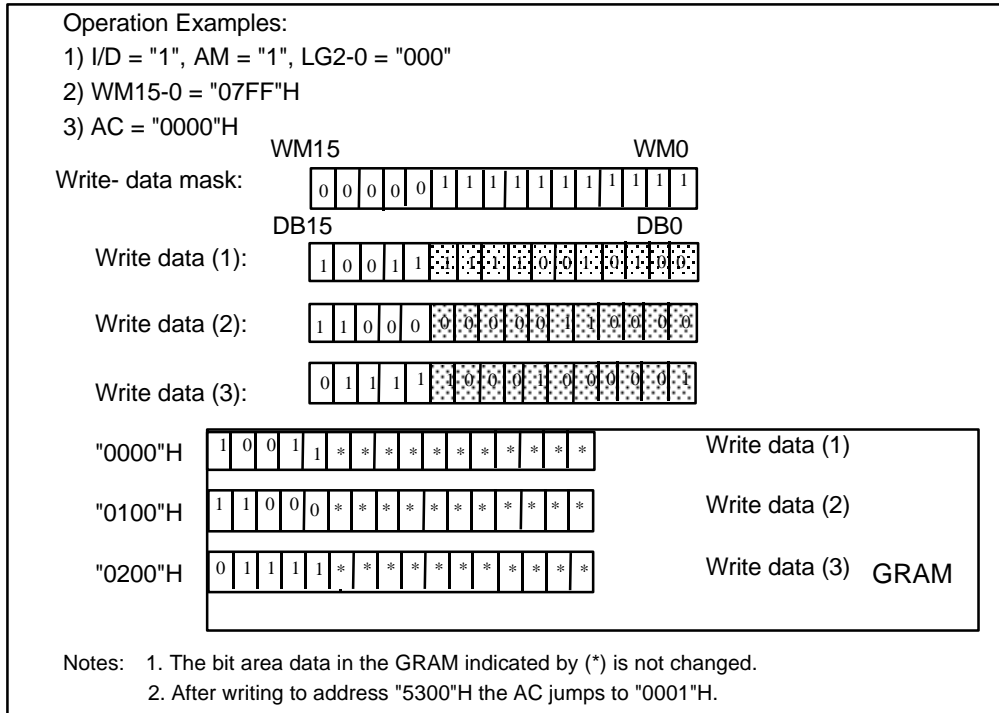


Figure 54 Operation of Write Mode 2

3. Write mode 3: AM = "0", LG2-0 = "110"/"111"

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP15-0). When the result of the comparison in a byte unit satisfies the condition write-data mask function (WM15-0) is also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D =1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

Operation Examples:

- 1) I/D = "1", AM = "0", LG2-0 = "110" (Matched write)
- 2) CP15-0 = "2860"H
- 2) WM15-0 = "0000"H
- 3) AC = "0000"H

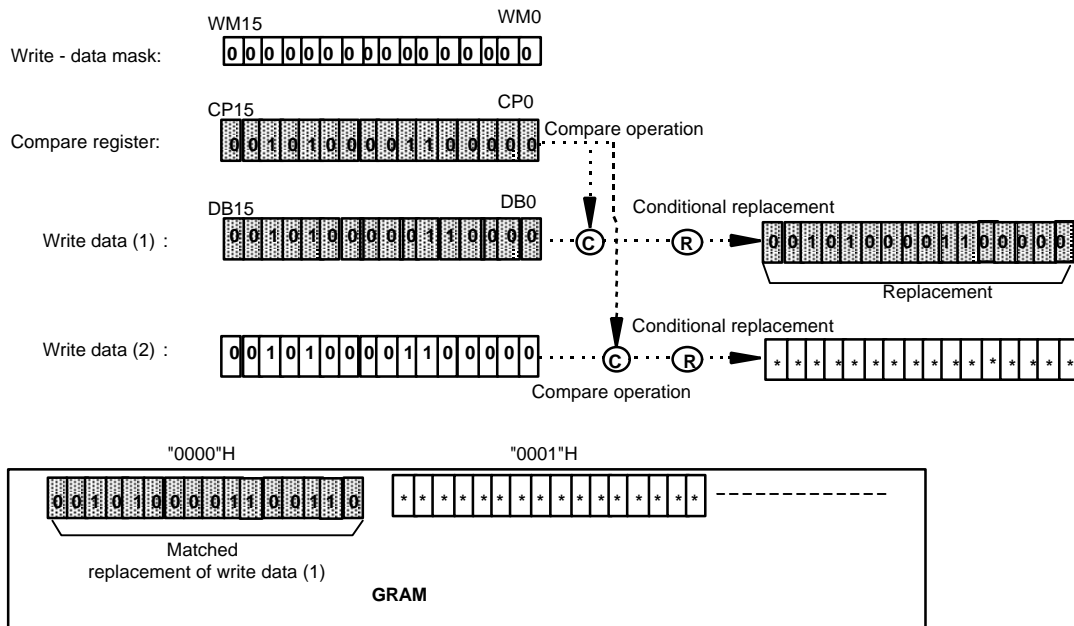


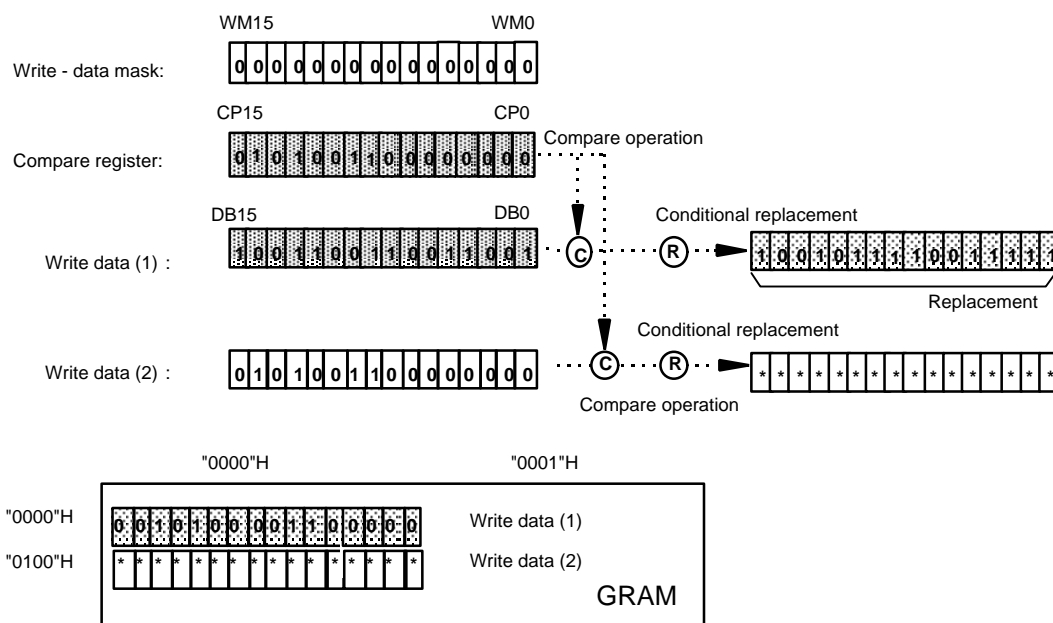
Figure 55 Operation of Write Mode 3

4. Write mode 4: AM = "1", LG2-0 = "110"/"111"

This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP15-0) to write the data. When the result by the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, write data mask function (WM15-0) is also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

Operation Examples:

- 1) I/D = "1", AM = "1", LG2-0 = "111" (Unmatched write)
- 2) WM15-0 = "2860"H
- 2) CP15-0 = "0000"H
- 3) AC = "0000"H



- Notes: 1. The bit area data in the GRAM indicated by (\*) is not changed.
- 2. After writing to address "5300"H the AC jumps to "0001"H.

Figure 56 Writing Operation of Write Mode 4

15. 4096 colors Display Function

HD66768 is equipped with 4096 colors display function. When SPR1-0 = "01", HD66768 selects 4,096 colors display mode.

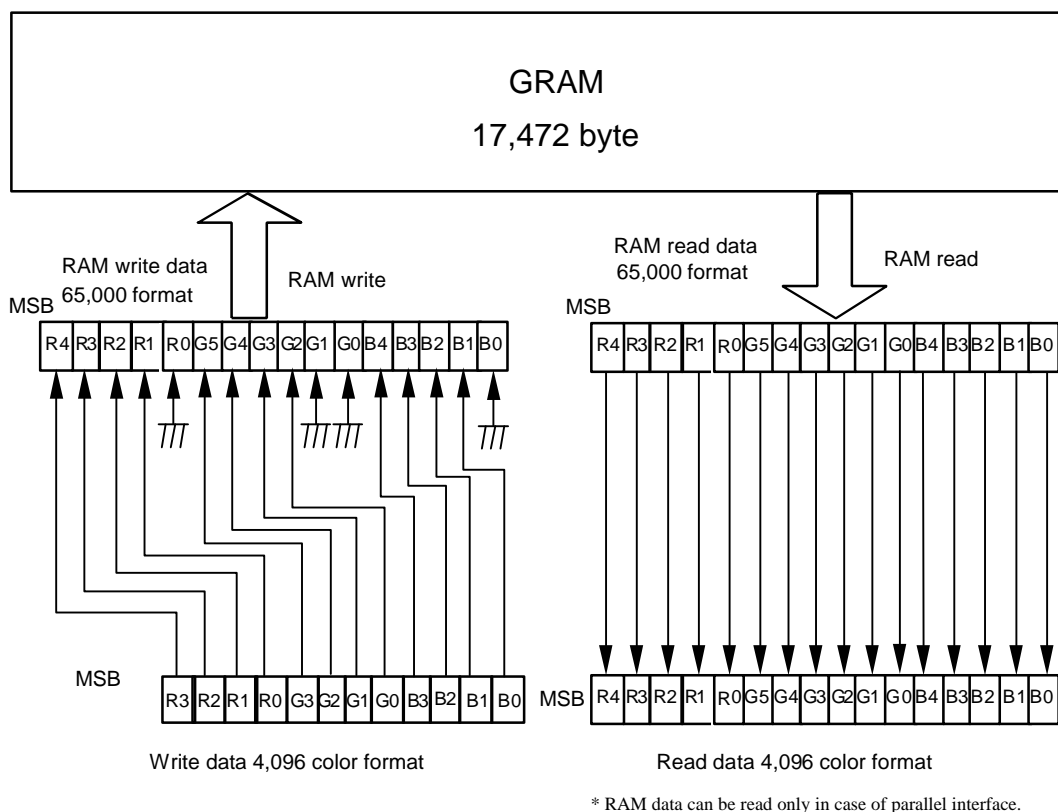


Figure57 4,096 color display data write and read format

4,096 color R, G, B data and selective grayscale palette

Table 34

Setting GRAM data				Grayscale palette				
R3	R2	R1	R0					
G3	G2	G1	G0					
B3	B2	B1	B0					
0	0	0	0	PK04	PK03	PK02	PK01	PK00
0	0	0	1	PK14	PK13	PK12	PK11	PK10
0	0	1	0	PK24	PK23	PK22	PK21	PK20
0	0	1	1	PK34	PK33	PK32	PK31	PK30
0	1	0	0	PK44	PK43	PK42	PK41	PK40
0	1	0	1	PK54	PK53	PK52	PK51	PK50
0	1	1	0	PK64	PK63	PK62	PK61	PK60
0	1	1	1	PK74	PK73	PK72	PK71	PK70
1	0	0	0	PK84	PK83	PK82	PK81	PK80
1	0	0	1	PK94	PK93	PK92	PK91	PK90
1	0	1	0	PK104	PK103	PK102	PK101	PK100
1	0	1	1	PK114	PK113	PK112	PK111	PK110
1	1	0	0	PK124	PK123	PK122	PK121	PK120
1	1	0	1	PK134	PK133	PK132	PK131	PK130
1	1	1	0	PK144	PK143	PK142	PK141	PK140
1	1	1	1	PK154	PK153	PK152	PK151	PK150

16. 256 Colors Display Function

HD66768 is equipped with 256 colors display function. When SPR1-0 = "10", HD66768 selects 256 colors display mode. When executing graphic operation, HD66768 expands 8-bit data inside LSI to 16-bit data, and write them into RAM. Take the expansion of data format into consideration because graphic operation is executed after expanding 8-bit data to 16-bit data while selecting 256 colors display mode.

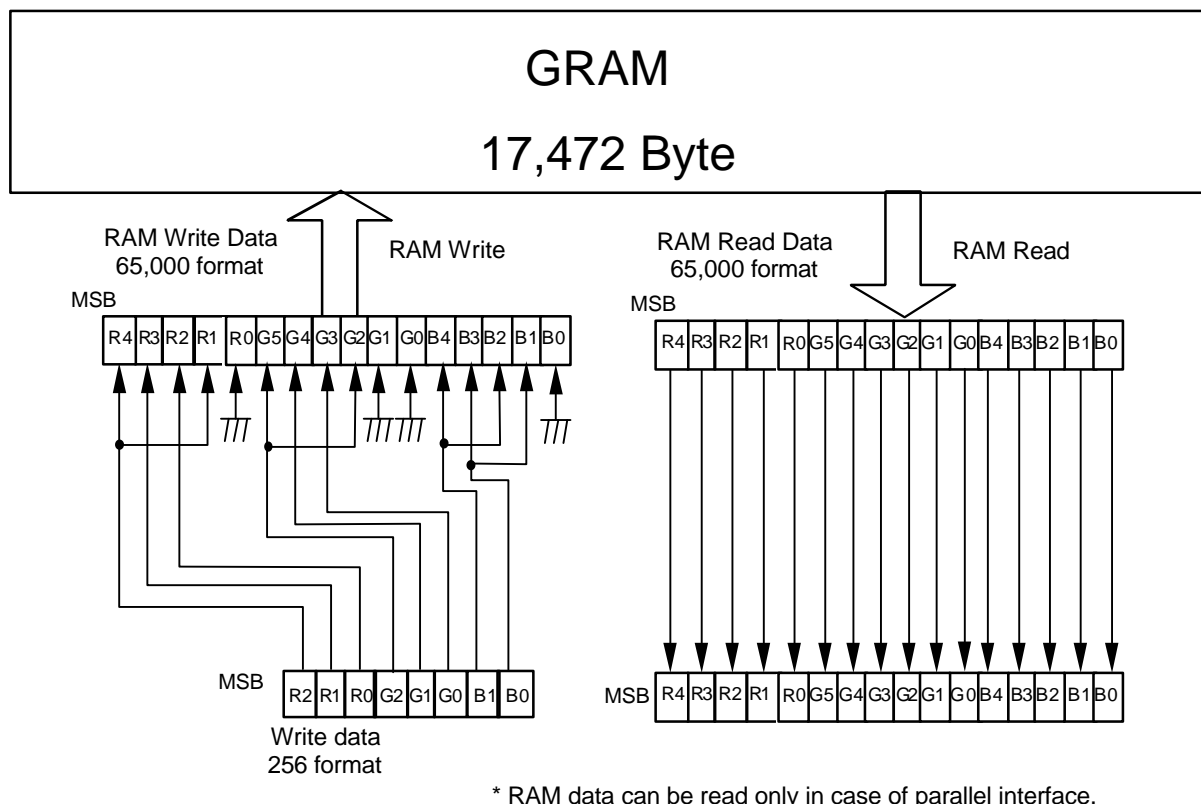


Figure 58 256 color display data write and read format

256 color R,G,B data and selective grayscale palette

R, G data and selective palette

Table 35

R,G data	Selective palette
000	PK0
001	PK2
010	PK4
011	PK6
100	PK9
101	PK11
110	PK13
111	PK15

B data and selective palette

Table 36

B data	Selective palette
00	PK0
01	PK6
10	PK9
11	PK15

### 17. Grayscale Palette

The HD66768 incorporates a grayscale palette to simultaneously display 4,096 of the 65,000 possible colors. The grayscales consist of 16 5-bit palettes. The 24-stage grayscale levels can be selected from the 5-bit palette data.

For the display data, the four-bit data in the GRAM written from the microcomputer is used. In this palette, a pulse-width modulation (PWM) is used to eliminate flicker in the LCD display. The time over which the LCDs are switched on is adjusted according to the level and grayscales are displayed so that flicker is reduced and grayscales are clearly displayed.

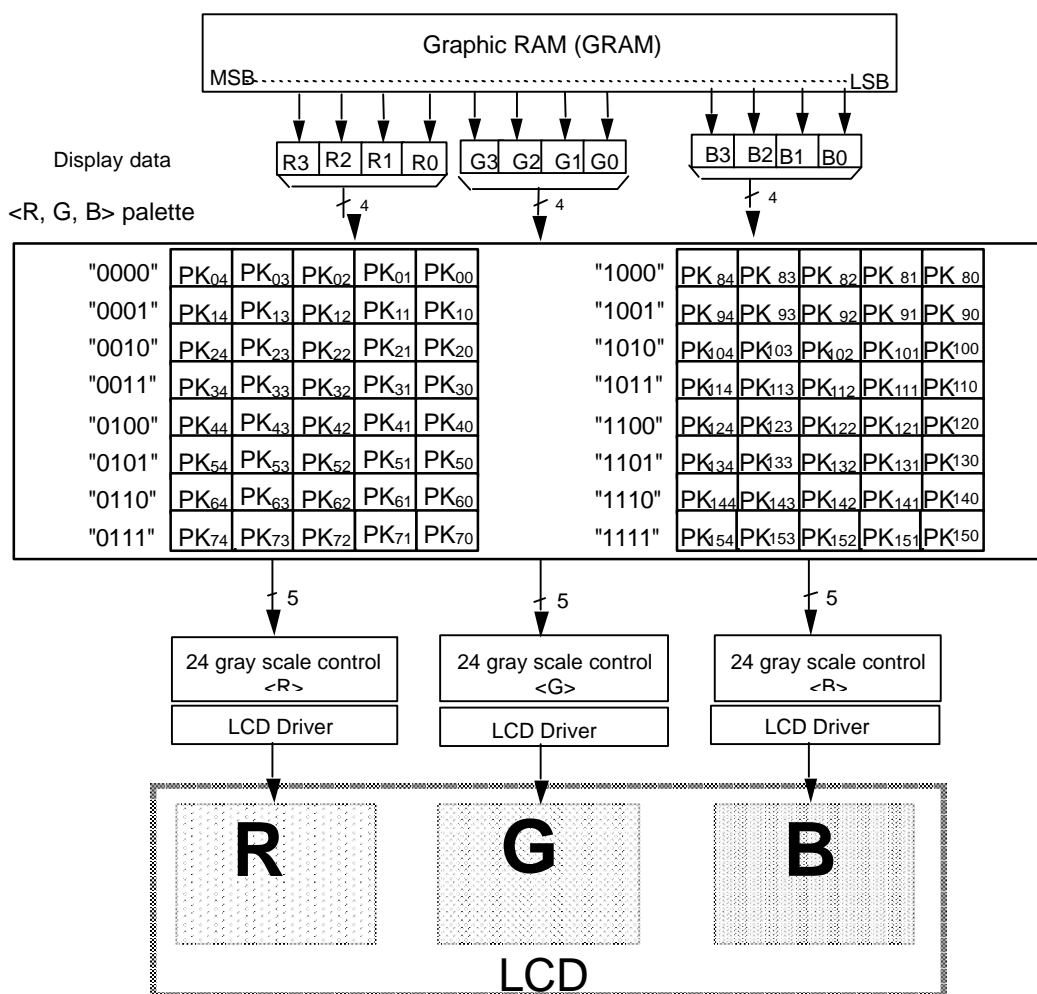


Figure 59 Grayscale Palette Control

### Grayscale Palette Table

The grayscale register that is set for each palette register (PK) can be set to any level. 25-grayscale lighting levels can be set according to palette values (“00000” to “11001”).

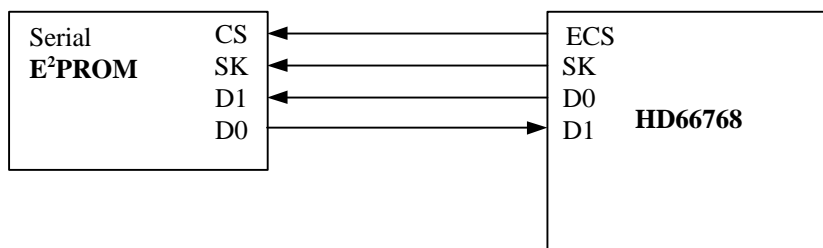
**Table 37 Grayscale Control Level**

Palette register value (PK)					Grayscale control level
0	0	0	0	0	Non lit (Note 1)
0	0	0	0	1	1/25
0	0	0	1	0	2/25
0	0	0	1	1	3/25
0	0	1	0	0	4/25
0	0	1	0	1	5/25
0	0	1	1	0	6/25
0	1	1	1	1	7/25
0	1	0	0	0	8/25
0	1	0	0	1	9/25
0	1	0	1	0	10/25
0	1	0	1	1	11/25
0	1	1	0	0	12/25
0	1	1	0	1	13/25
0	1	1	1	0	14/25
0	1	1	1	1	15/25
1	0	0	0	0	16/25
1	0	0	0	1	17/25
1	0	0	1	0	18/25
1	0	0	1	1	19/25
1	0	1	0	0	20/25
1	0	1	0	1	21/25
1	0	1	1	0	22/25
1	0	1	1	1	23/25
1	1	0	0	0	24/25
1	1	0	0	1	All lit (Note 2)

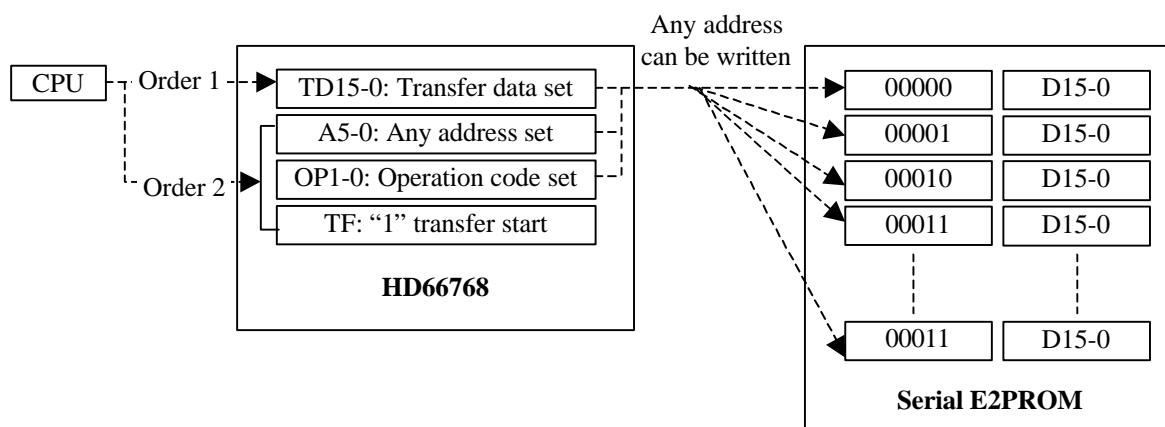
- Notes:
1. The unlit level corresponds to a black display when a normally-black color-LCD panel is used, and a white display when a normally-white color-LCD panel is used.
  2. The all-lit level corresponds to a white display when a normally-black color-LCD panel is used, and a black display when a normally-white color-LCD panel is used.

**18. E2PROM interface**

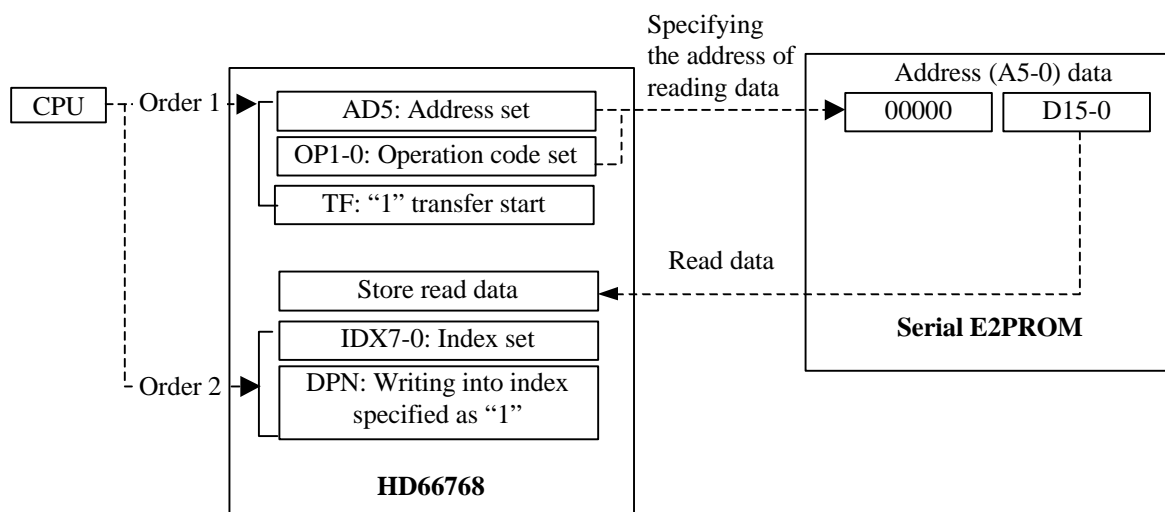
HD66768 is equipped with serial E2PROM interface that is capable of interface with serial E<sup>2</sup>PROM. When using it for write interface, data set in TD15-0 is written into any E<sup>2</sup>PROM address according to the order from CPU. When using it for read interface read data specified by A5-0 is written into HD66768 index specified by IDX7-0 according to the order from CPU.



**Figure60 Example of interfaced with serial E<sup>2</sup>PROM**



**Figure61 Example of writing into serial E<sup>2</sup>PROM**



**Figure62 Example of reading from serial E<sup>2</sup>PROM**

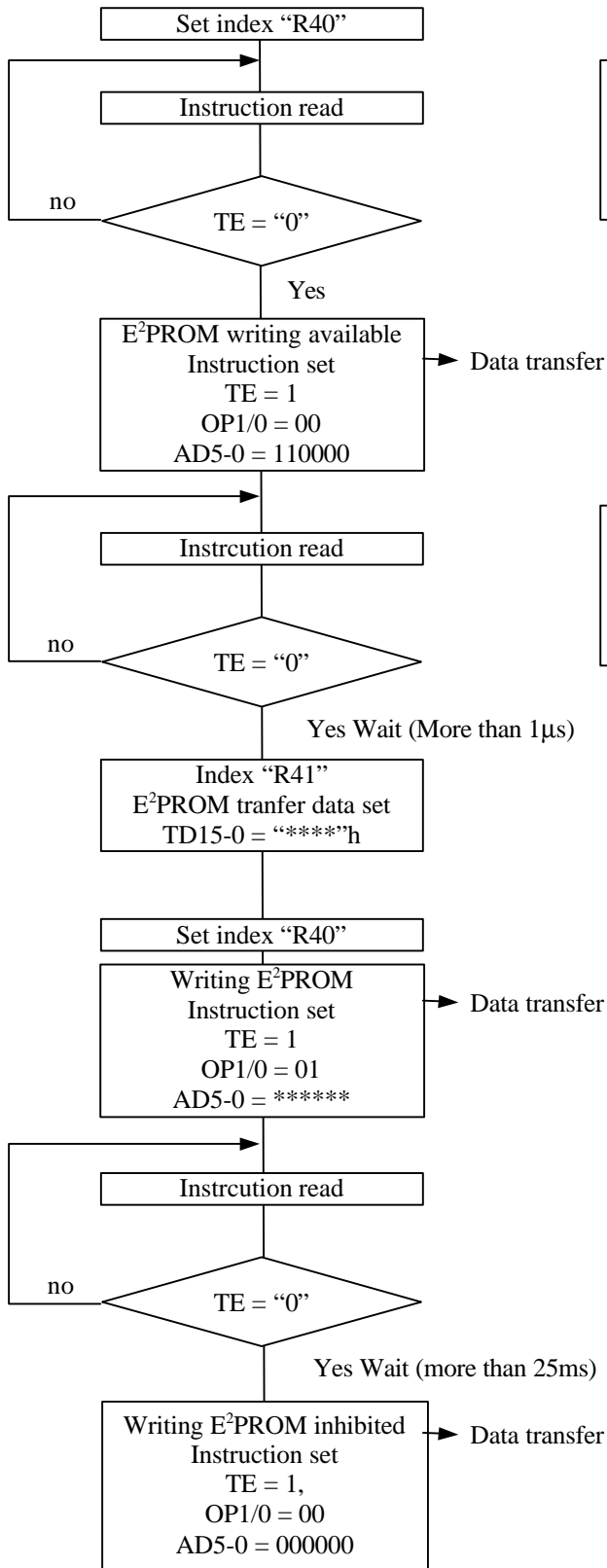


Figure 63 Data write flow

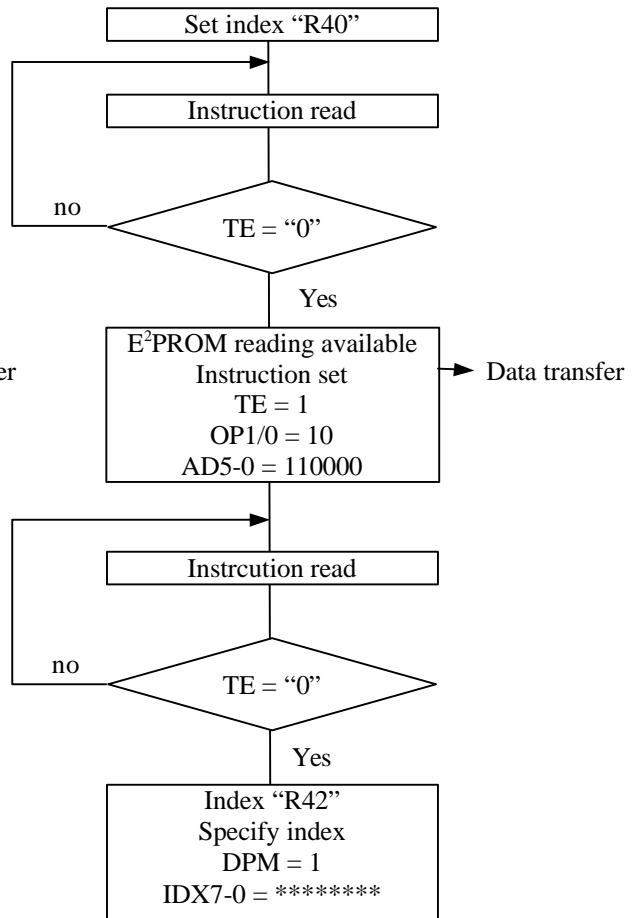


Figure 64 Data read flow

a) Example of serial E<sup>2</sup>PROM and write operation

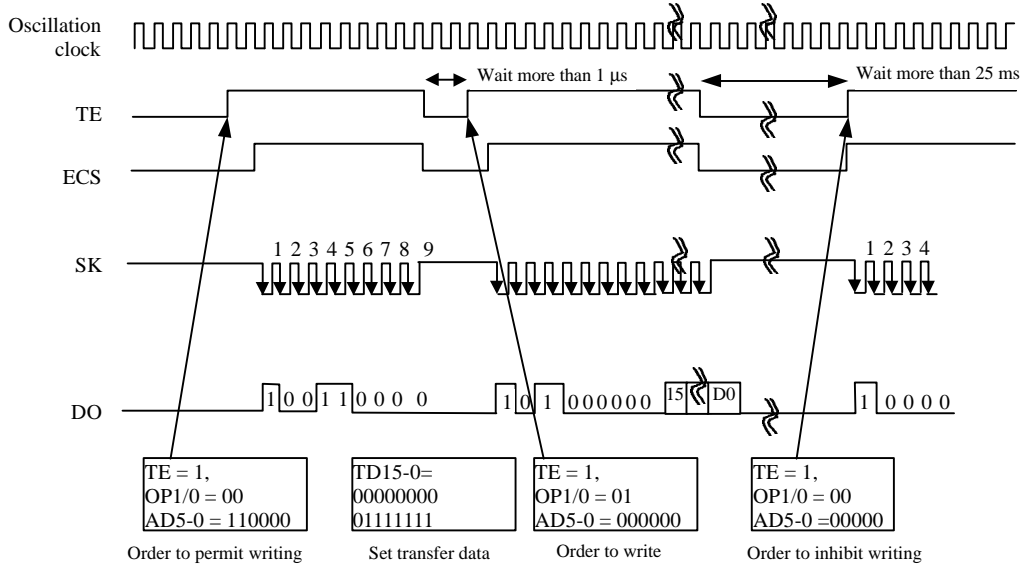


Figure 65 Example of serial E<sup>2</sup>PROM and write operation

b) Example of serial E<sup>2</sup>PROM and read operation

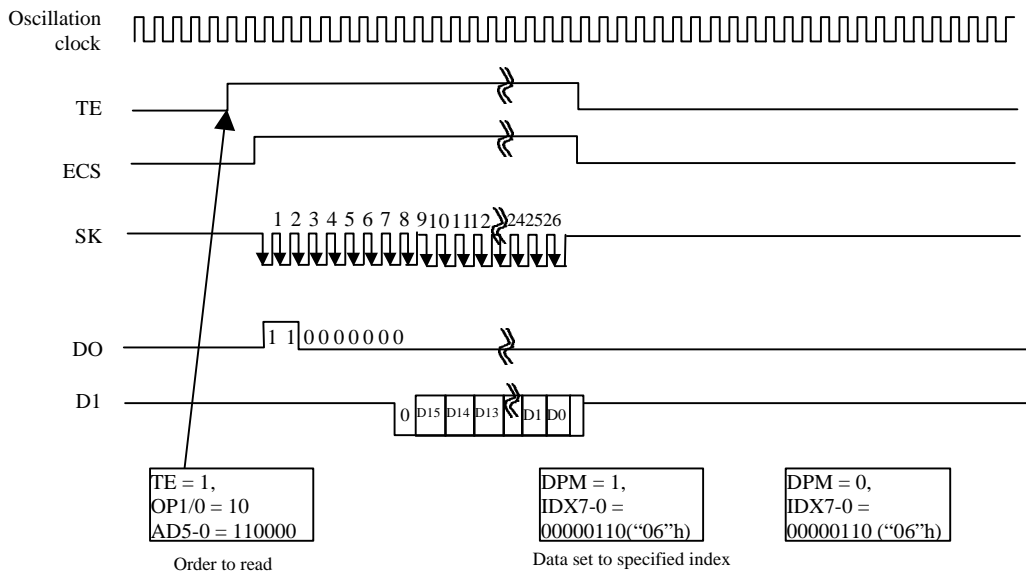


Figure 66 Example of serial E<sup>2</sup>PROM and read operation

**19. Setting flow for low power consumption instruction**

**Sleep Mode**

Setting the sleep mode bit (SLP) to “1” puts the HD66768 in the sleep mode, where the device stops all internal display operations, thus reducing current consumption. Specifically, LCD operation is completely halted. Here, all the SEG (SEG1 to SEG312) and all the COM (COM1 to COM84) pins output the GND level, resulting in no display. If the AP2-0 bits in the power control register are set to “000” in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

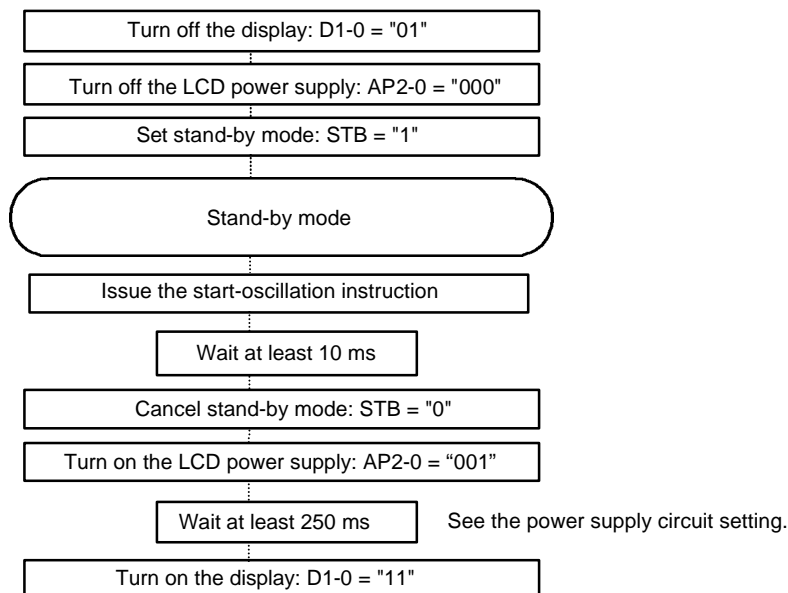
**Table 38 Comparison of Sleep Mode and Standby Mode**

Function	Sleep Mode (SLP = “1”)	Standby Mode (STB = “1”)
LCD control	Turned off	Turned off
R-C oscillation circuit	Operates normally	Operation stopped

**Standby Mode**

Setting the standby mode bit (STB) to “1” puts the HD66768 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, all the SEG (SEG1 to SEG312) and all the COM (COM1 to COM84) pins output the GND level, resulting in no display. If the AP2-0 transfer data by every two bytes from MSB. Bits are set to “000” in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than the start-oscillation instruction and the stand-by cancellation instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to “0”.



Procedure for Setting and Canceling Standby Mode

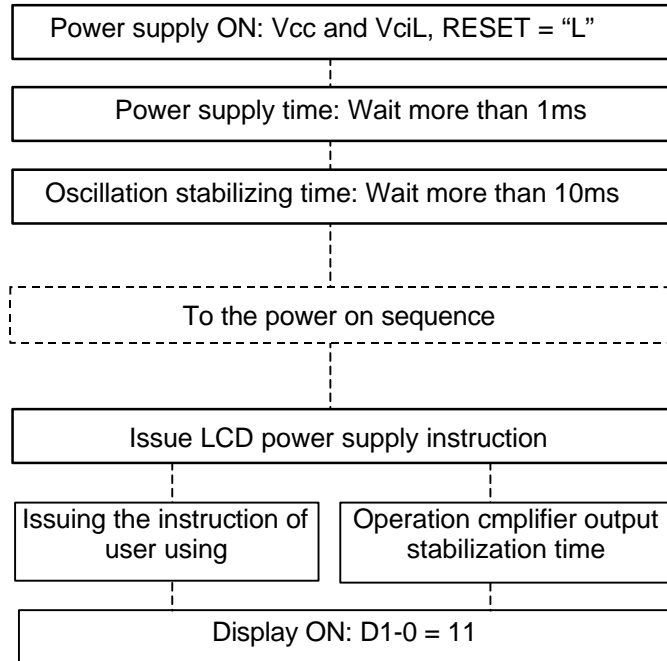
**Figure 67 Procedure for Setting and Canceling Standby Mode**

**20. Setting flow for power supply and display instruction**

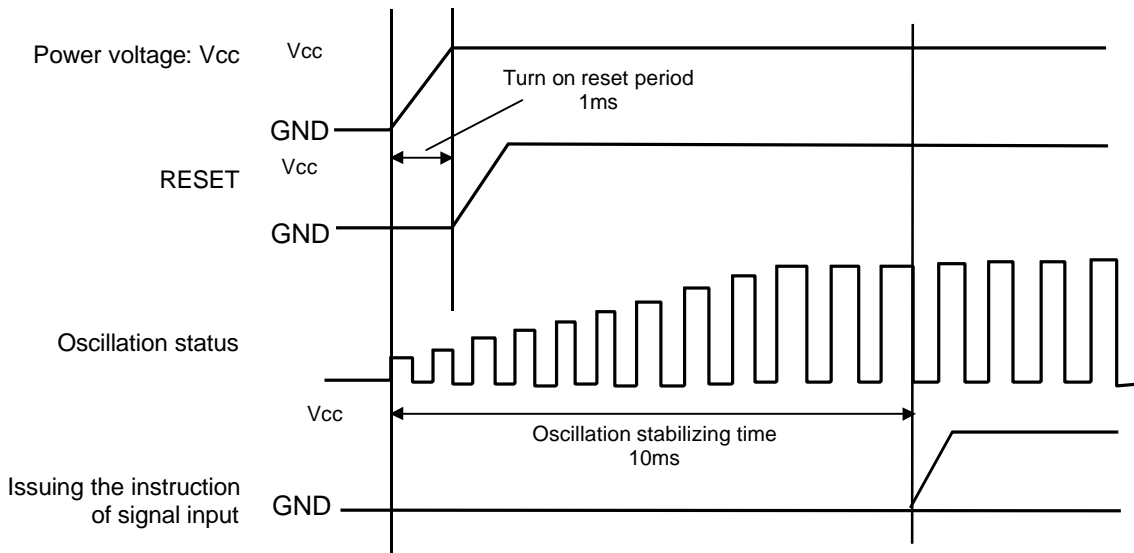
**Power-on / off Sequence**

To prevent pulse lighting of LCD screens at power-on/off, the power-on/off sequence is activated as shown below. However, since the sequence depends on LCD materials to be used, confirm the conditions by using each system.

**Power-on sequence**



**Figure 68**



Note: When hardware reset is input during the power-off period, the D1-0 bits are cleared to "00" and SEG/COM output is forcibly lowered to the GND levels.

**Figure 69**

Power off sequence

Normal operation

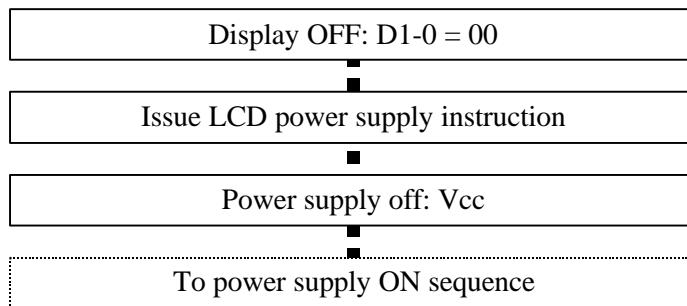


Figure 70

Emergency operation

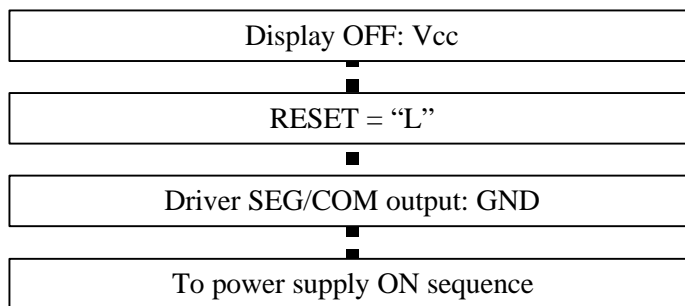
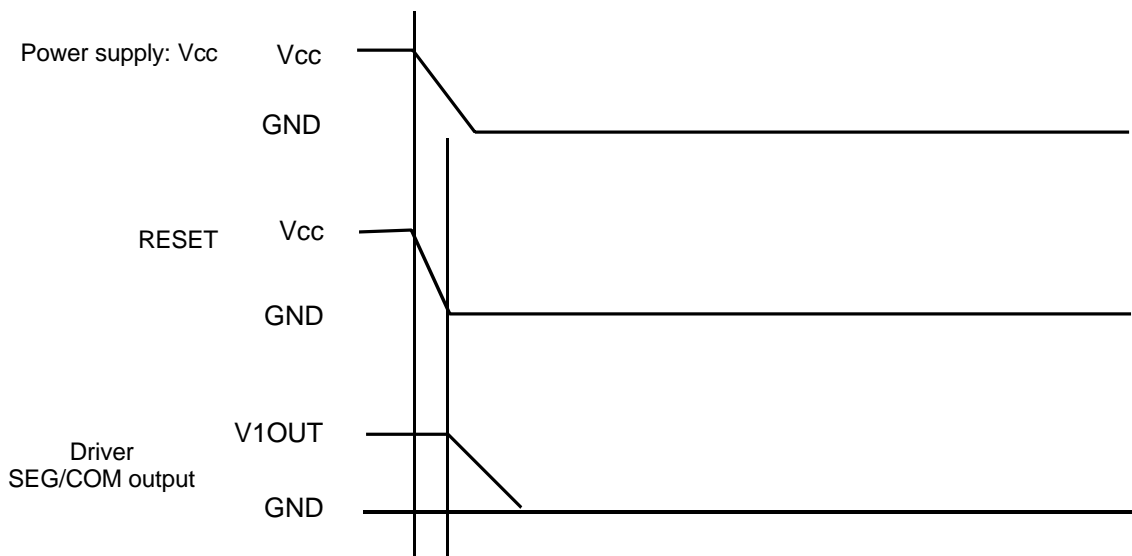


Figure 71

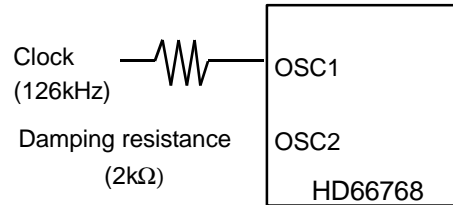
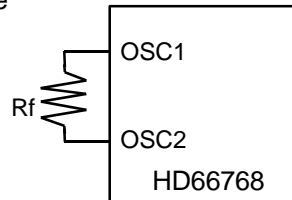


Note: When executing hardware reset while power supply is off, D1-0 bit becomes "00" at the timing of reat. Output level of SEG/COM is force to be set to GND level.

Figure 72

**21. Oscillation Circuit**

The HD66768 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If  $R_f$  is increased or power supply voltage is decreased, the oscillation frequency decreases. For the relationship between  $R_f$  resistor value and oscillation frequency, see the Electric Characteristics Notes section.

**1) External clock mode****Figure 73****2) External resistance oscillation mode**

Note:  $R_f$  resistance must be located near the OSC1/OSC2 pins.

**Figure 74**

## 22. Frame-Frequency Adjustment Function

The HD66768 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD drive as the oscillation frequency is always the same. When the display duty is changed, the frame frequency can be adjusted to be the same.

If the oscillation frequency is set to high, an animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching, for an animated display, etc. is required, the frame frequency can be set high.

### Relationship between LCD Drive Duty and Frame Frequency

The relationship between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the retrace-line period bit (RTN) and in the operation clock division bit (DIV) by the instruction.

(Formula for the frame frequency)

$$\text{Frame frequency} = \frac{f_{osc}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times 1/\text{duty}} \quad [\text{Hz}]$$

$f_{osc}$ : R-C oscillation frequency

Duty: drive duty (NL bit)

Clock cycles per raster-row: (RTN + 25) clock cycles

Division ratio: DIV bit

### Example Calculation 1 Setting the maximum frame frequency to 60 Hz

Display duty: 1/84

Retrace-line period: 0 clock (RTN3-0 = "0000")

Operation clock division ratio: 1 division

$$f_{osc} = 60 \text{ Hz} \times (0 + 25) \text{ clock} \times 1 \text{ division} \times 84 \text{ lines} = 126 \text{ (kHz)}$$

In this case, the R-C oscillation frequency becomes 126kHz. The external resistance value of the R-C oscillator must be adjusted to be 126 kHz. The display duty can be changed by the partial display, etc. and the frame frequency can be the same by setting the RNT bit and DIV bit to achieve the following.

(Partial display): Display duty: 1/40

Retrace-line period: 1 clock (RTN3-0 = "0010")

Operation clock division ratio: 2 division

$$\text{Frame frequency} = 126 \text{ kHz} / ((2 + 25) \text{ clock} \times 2 \text{ division} \times 40 \text{ lines}) = 58.3 \text{ (Hz)}$$

### Example Calculation 2 Switching the frame frequency to suit animation/static image display

(Animation display): Frame frequency: 90 Hz

Display duty: 1/84

Retrace-line period: 0 clock (RTN3-0 = "0000")

Operation clock division ratio: 1 division

$$f_{osc} = 90 \text{ Hz} \times (0 + 25) \text{ clock} \times 1 \text{ division} \times 84 \text{ lines} = 189 \text{ (kHz)}$$

(Static image display): Frame frequency: 90 Hz

Display duty: 1/84

Retrace-line period: 1 clock (RTN3-0 = "1101")

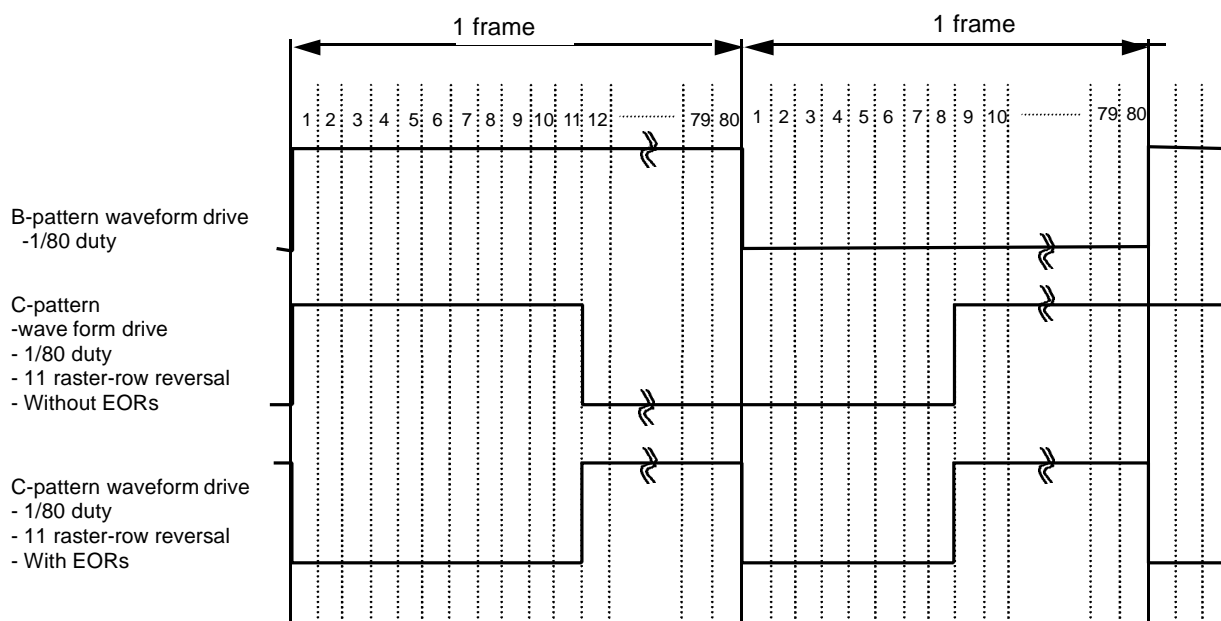
Operation clock division ratio: 1 division

$$\text{Frame frequency} = 189 \text{ kHz} / ((13 + 25) \text{ clock} \times 1 \text{ division} \times 84 \text{ lines}) = 59.2 \text{ (Hz)}$$

### 23. n-raster-row Reversed AC Drive

The HD66768 has not only the LCD reversed AC drive in a one-frames unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from two to 64 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as crosstalk at high-duty driving of more than 1/64 duty, the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality.

Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.



Notice: Specify the number of AC drive raster-rows and the necessity of EOR so that the DC bias is not generated to the LCD.

Figure 75 Example of an AC Signal under n-raster-row Reversed AC Drive

### 24. Screen-division Driving Function

The HD66768 can select and drive two screens at any position with the screen-driving position registers (R14h and R15h). Any two screens required for display are selectively driven and a duty ratio is lowered by LCD-driving duty setting (NL4-0), thus reducing LCD-driving voltage and power consumption. For the 1st division screen, start line (SS17-10) and end line (SE17-10) are specified by the 1st screen-driving position register (R14h). For the 2nd division screen, start line (SS27-20) and end line (SE27-20) are specified by the 2nd screen-driving position register (R15h). The 2nd screen control is effective when the SPT bit is "1". The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.

1/24 duty driving on 2 screen

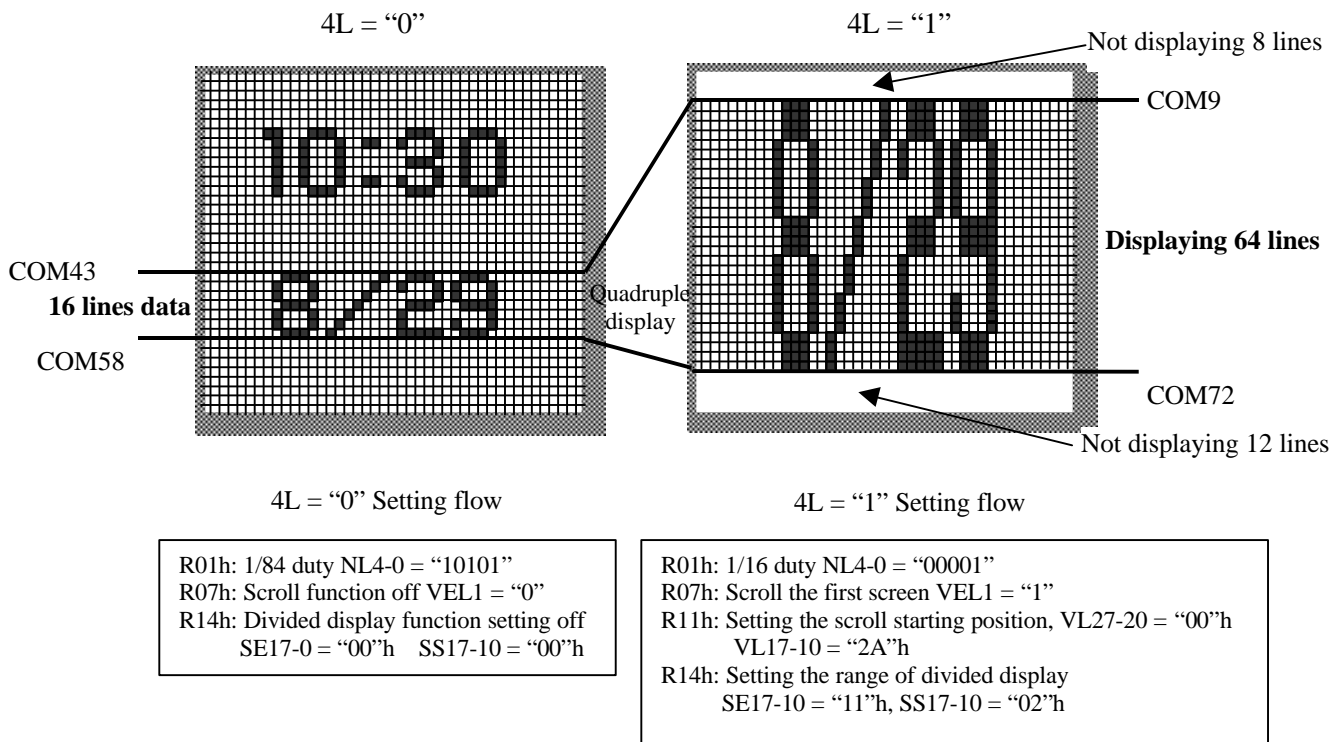


- Driving duty: NL4-0 = "00010" (1/24 duty)
- 1st screen setting: SS17-10 = "00"H, SE17-10 = "06" H
- 2nd screen setting: SS27-20 = "19"H, SE27-20 = "29" H, SPT = "1"

Figure 76 Display example in 2-screen division driving

### Quadruple display mode

By setting quadruple display mode (4L = "1"), HD66768 can display quadruple of normal display data (4L = "0") in vertical direction. Quadruple display mode enables wide range of display with low duty operation voltage.



\* Quadruple display mode can be used with scroll function and divided display function at the same time.

Figure 77 Example of setting quadruple display mode

**Restrictions on the 1st/2nd Screen Driving Position Register Settings**

The following restrictions must be satisfied when setting the start line (SS17-10) and end line (SE17-10) of the 1st screen driving position register (R14h) and the start line (SS27-20) and end line (SE27-20) of the 2nd screen driving position register (R15h) for the HD66768. Note that incorrect display may occur if the restrictions are not satisfied.

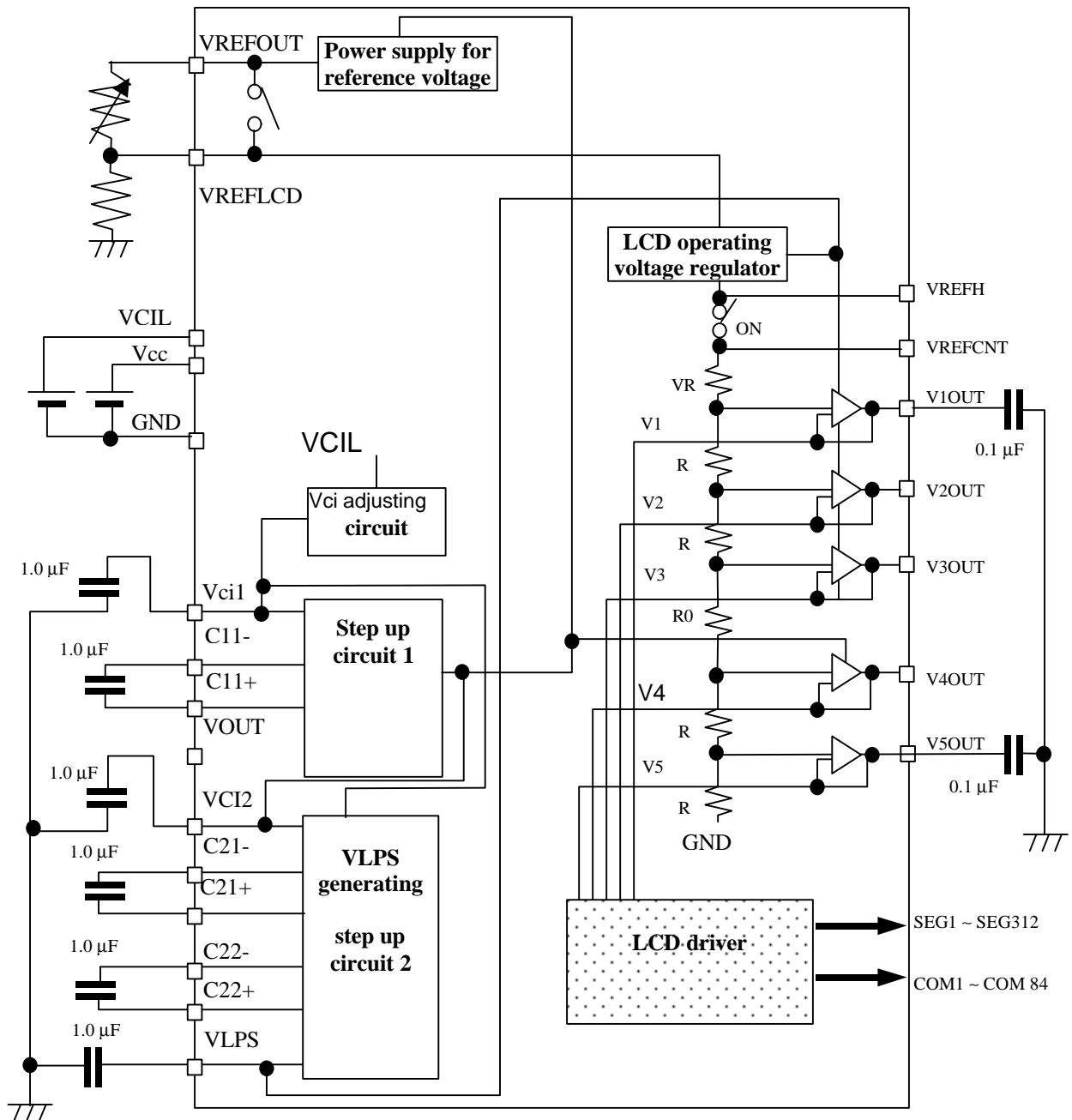
**Table 39 Restrictions on the 1st/2nd Screen Driving Position Register Settings**

	1st Screen Driving (SPT = 0)	2nd Screen Driving (SPT = 1)
Register setting	SS17-10 ≤ SE17-10 ≤ "53"H	SS17-10 ≤ SE17-10 < SS27-20 ≤ SE27-20 ≤ "53"H
Display operation	<ul style="list-style-type: none"> <li>• Time-sharing driving for COM pins (SS1+1) to (SE1+1)</li> <li>• Non-selection level driving for others</li> </ul>	<ul style="list-style-type: none"> <li>• Time-sharing driving for COM pins (SS1+1) to (SE1+1) and (SS2+1) to (SE2+1)</li> <li>• Non-selection level driving for others</li> </ul>

- Notes:
1. When the total line count in screen division driving settings is less than the duty setting, non-selection level driving is performed without the screen division driving setting range.
  2. When the total line count in screen division driving settings is larger than the duty setting, between the start line and the duty-setting line are displayed and non-selection level driving is performed for other lines.
  3. For the 1st screen driving, the SS27-20 and SE27-20 settings are ignored.

25. CD Voltage Generation Circuit

Figure shows a configuration of the HD66768 LCD drive voltage generation circuit. It consists of three circuits; step up circuit 1, step up circuit 2, and polarity inverting circuit. Step up circuit 1 generates VOUT by doubling the voltage applied to Vci1. Step up circuit 2 generates the negative voltage by multiplying Vci2 by 1.5 to 3 times. These circuits generate VCH and VCL to operate LCD functions. VSH and VM for LCD operation is generated by dividing the output voltage of VREF Control amplifier.



Note 1) Use capacitors with character B ( $\pm 10\%$  of capacity change).

Figure 78 Configuration of internal power circuit

Power supply level correlation

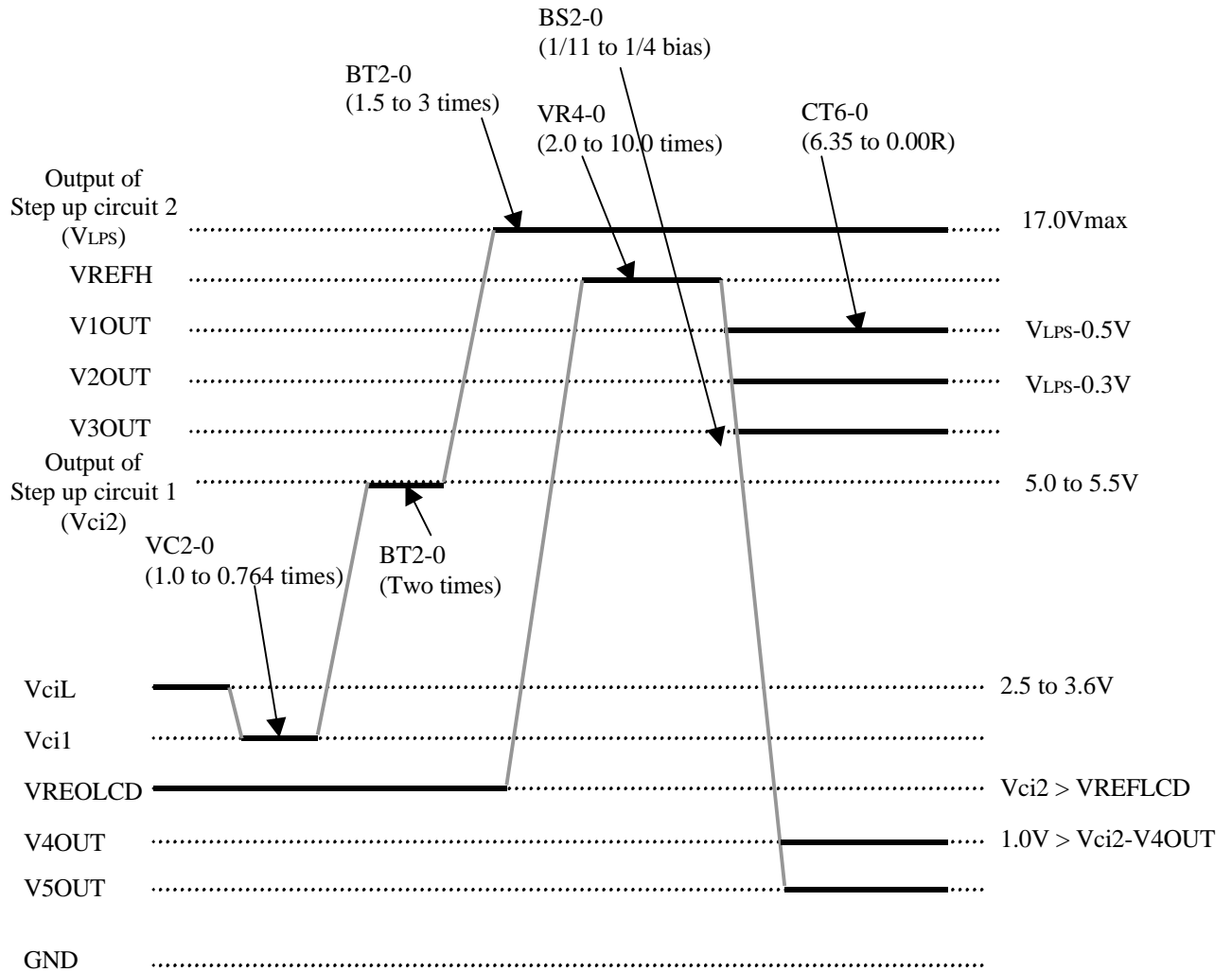


Figure 79 HD66768 Power supply level correlation

26. Step up factor and external connecting circuit with step up circuit 1 and 2

- Connecting example between step up circuit 1 and external capacitor

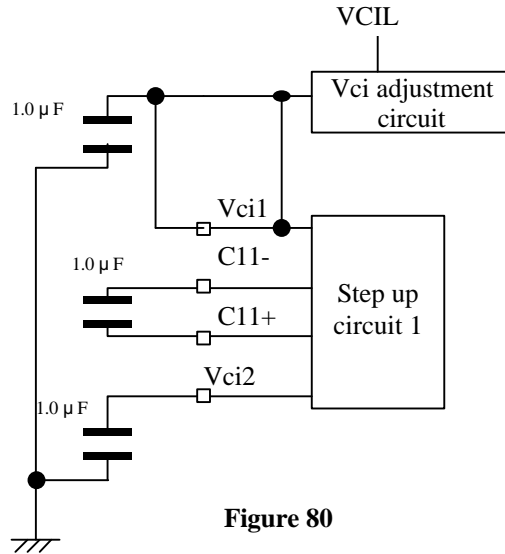


Figure 80

- Connecting example between step up circuit 2 and external capacitor

(1) 3 times step up ( $3 \times V_{ci2}$ )

(2) 2.5times step up ( $2.5 \times V_{ci2}$ )

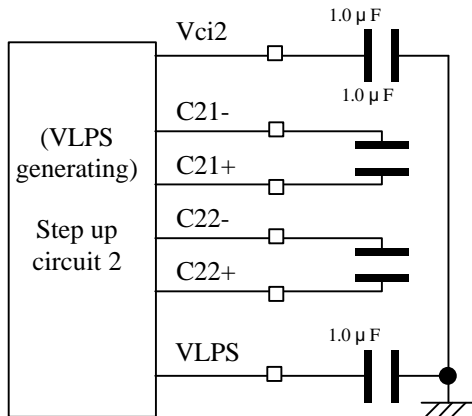


Figure 81

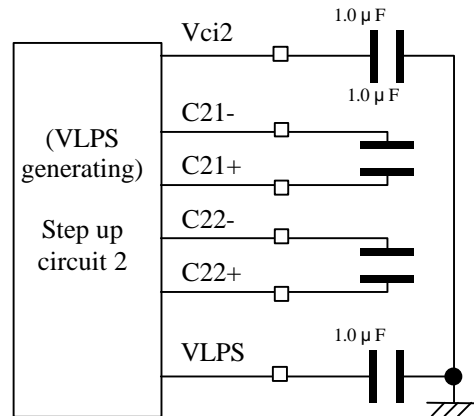


Figure 82

(3) 2 times step up ( $2 \times V_{ci2}$ )

(4) 1.5 times step up ( $1.5 \times V_{ci2}$ )

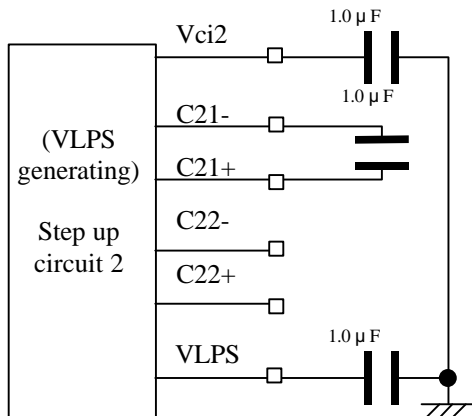


Figure 83

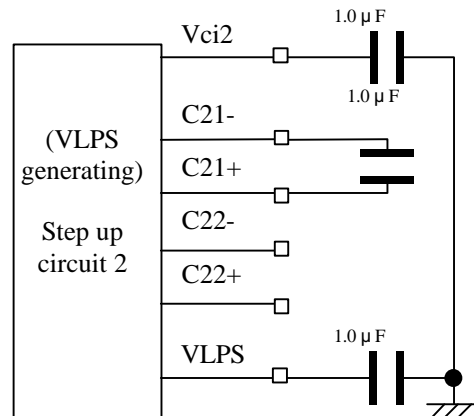


Figure 84

Caution:

1. Generate an output voltage (Vci2) from step-up circuit 1 within the range from 5.0 to 5.5V.
2. Do not allow the output voltage (VLPS) from step-up circuit 2 to exceed 17.0V.
3. Generate an output voltage of (Vci2) and V4 level (V4OUT) within the range of 1.0V > Vci2-V4OUT.
4. Be sure that V1 output level is set lower than (VLPS-0.5)V.
5. Be sure that V3 output level is set lower than (VLPS-3.0)V.
6. When capacitor with polarity is used, be sure that an inverted voltage is not applied to it in any state of the system.
7. Rated voltage of capacitors possible to be used is as described below. Required voltage depends on used panels. When actual voltage is less than 16V, capacitors with 16V rated voltage can be used.  
 6.3V: Vci1, Vci2, C11+, C11-, V5OUT  
 25V(16V): VLPS, C21+, C21-, C22+, C22-, V1OUT

**LCD Drive Bias**

BS2-0 bit selects the best suited LCD drive bias according to the LCD drive duty setting (NL4-0 bit). LCD drive duty and bias value can be switched with software according to the display status on LCD panel. According to the setting of LCD driving duty (NL4-0 bit), BS2-0 bit selects best suited LCD driving bias. According to the display status, LCD driving duty and bias value can be displayed by switching software. An optimal bias can be calculated by applying the following expression. The value that has been calculated is theoretically optimal. If a lower bias value than the optimal value is used to drive the LCD, contrast may be reduced depending on lighting conditions. However, the power consumption can be reduced by lowering the drive voltage. Adjust the value according to the system to be used.

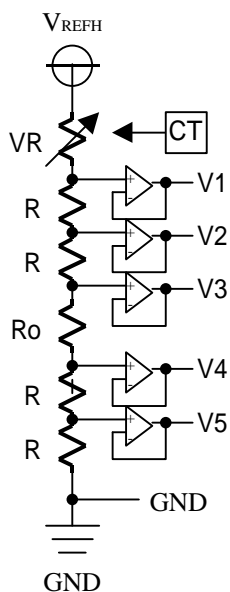
$$\text{Best suited bias value when operating } 1/N \text{ duty} = \frac{1}{\sqrt{N} + 1}$$

**Table 40**

LCD operating duty	1/84	1/80	1/72	1/64	1/56	1/48	1/40	1/32	1/24	1/16	1/8
NL4-0 (Setting value)	"0A"H	"09"H	"08"H	"07"H	"06"H	"05"H	"04"H	"03"H	"02"H	"01"H	"00"H
Best operating bias	1/11	1/10	1/10	1/9	1/9	1/8	1/8	1/7	1/6	1/5	1/4
BS2-0 (Setting value)	"000"	"001"	"001"	"010"	"010"	"011"	"011"	"100"	"101"	"110"	"111"

**Contrast adjustment**

Contrast can be adjusted in 128 stages with software by controlling LCD driving voltage (voltage difference between VREFH and V1) with contrast adjusting register (CT bit). Various register VR between VREFH and V1 can be finely adjusted by 0.05 x R unit within the range from 0.00 x R to 6.35 x R against dividing basic register value R.



**Figure 85**

**Table 41**

CT setting value							Various resistance value	Voltage difference between V1-GND	Display color
CT6	CT5	CT4	CT3	CT2	CT1	CT0			
0	0	0	0	0	0	0	6.35R	Min. ↑ ↓ Max.	Dark ↑ ↓ Light
0	0	0	0	0	0	1	6.30R		
0	0	0	0	0	1	0	6.25R		
0	0	0	0	0	1	1	6.20R		
0	0	0	0	1	0	0	6.15R		
0	0	0	0	1	0	1	6.10R		
0	0	0	0	1	1	0	6.05R		
0	0	0	0	1	1	1	6.00R		
				⋮			⋮		
1	0	0	0	0	0	0	3.15R		
1	0	0	0	0	0	1	3.10R		
1	0	0	0	0	1	0	3.05R		
1	0	0	0	0	1	1	3.00R		
				⋮			⋮		
1	1	1	1	1	0	0	0.15R		
1	1	1	1	1	0	1	0.10R		
1	1	1	1	1	1	0	0.05R		
1	1	1	1	1	1	1	0.00R		

## 27. Absolute Maximum Ratings

**Table 42**

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	Vcc	V	-0.3 to + 4.6	1, 2
Power supply voltage (2)	Vcil	V	-0.3 to + 4.6	1, 3
Power supply voltage (3)	VLPS-GND	V	-0.3 to + 17.5	1, 4
Input voltage	Vt	V	-0.3 to Vcc + 0.3	1
Operating temperature	Topr	°C	-40 to + 85	1, 4
Storage temperature	Tstg	°C	-55 to + 110	1, 5

Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

2.  $V_{cc} \geq GND$  must be maintained
3.  $V_{cil} \geq GND$  must be maintained.
4.  $VLPS \geq GND$  must be maintained
5. For die and wafer products, specified up to 85 °C.

## 28. DC Characteristics

DC Characteristics ( $V_{CC} = 1.7$  to  $3.6$  V, VLPS=5V to 17V,  $T_a = -40$  to  $+85^\circ\text{C}$  \*<sup>1</sup>)

Table43

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Input high voltage	$V_{IH}$	V	$V_{CC} = 1.7$ to $3.6$ V	$0.7 V_{CC}$	—	$V_{CC}$	2, 3
Input low voltage	$V_{IL}$	V	$V_{CC} = 1.7$ to $3.6$ V	-0.3	—	$0.15V_{CC}$	2, 3
Output high voltage (1) (Dpins)	$V_{OH1}$	V	$I_{OH} = 0.1$ mA	$0.75V_{CC}$	—	—	2
Output low voltage (1) (DB7-0)	$V_{OL1}$	V	$V_{CC} = 1.7$ to $2.4$ V, $I_{OL} = 0.1$ mA	—	—	$0.2 V_{CC}$	2
			$V_{CC} = 2.4$ to $3.6$ V, $I_{OL} = 0.1$ mA	—	—	$0.15V_{CC}$	2
Driver ON resistance (SEG pins)	$R_{SEG}$	k $\Omega$	$\pm I_d = 0.05$ mA, VLPS = 10 V	—	TBD	TBD	4
Driver ON resistance (COM pins)	$R_{COM}$	k $\Omega$	$\pm I_d = 0.05$ mA, VLPS = 10 V	—	TBD	TBD	4
I/O leakage current	$I_{Li}$	$\mu\text{A}$	$V_{IN} = 0$ to $V_{CC}$	-1	—	1	5
Current Consumption ( $V_{CC} - \text{GND}$ )	Normal operation mode (LSI drive power supply step-up function)	$I_{OP}$	$\mu\text{A}$	—	TBD	TBD	—
	Standby mode	$I_{ST}$	$\mu\text{A}$	$V_{CC} = 3$ V, $T_a = 25^\circ\text{C}$	—	TBD	TBD

Electrical Characteristics Notes

- 1. For bare die and wafer products, specified up to 85°C.
- 2. The following three circuits are I pin, I/O pin, O pin configurations.

Pins: RESET\*, CS\*, E/WR, RW/RD, RS, OSC1, IM2-1, IM0/ID, TEST

Pins: OSC2

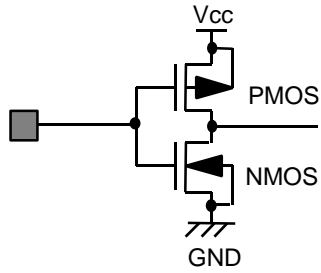


Figure 86

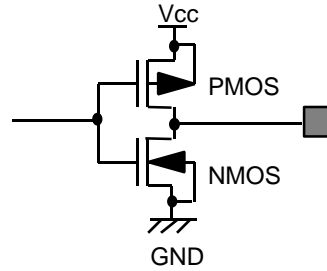


Figure 87

Pins: DB7 -DB2, DB1/SD0, DB0/SD1

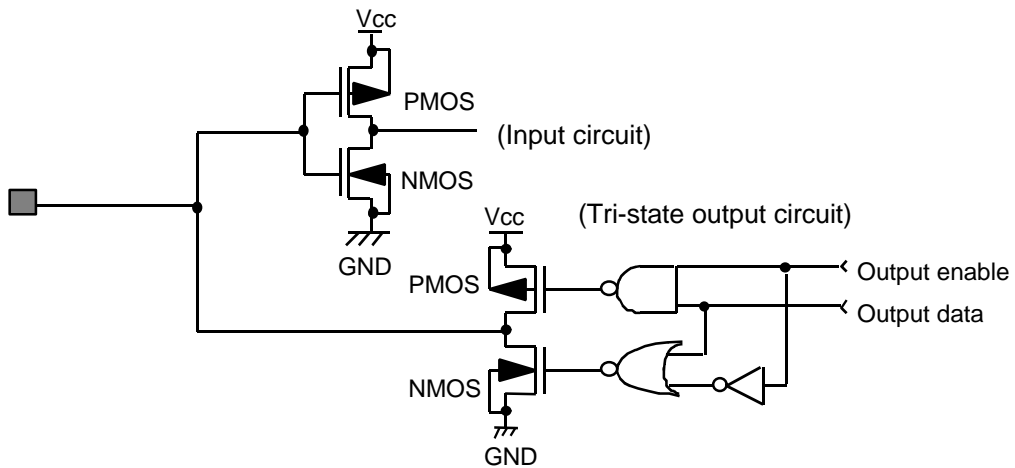


Figure 88 I/O Pin Configuration

3. The TEST1, TEST2 pins must be grounded and the IM2/1 and IM0/ID pins must be grounded or connected to Vcc.
4. Applies to the register value from V1OUT, V2OUT, V5OUT and GND terminal to each common signal terminal (RCOM) and the register value from V1OUT, V3OUT, V4OUT, and GND terminal to each segment signal terminal (RSEG).
5. This excludes the current flowing through output drive MOSs.
6. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating. Even if the CS pin is low or high when an access with the interface pin is not performed, current consumption does not change.
7. Applies to the external clock input (figure ).

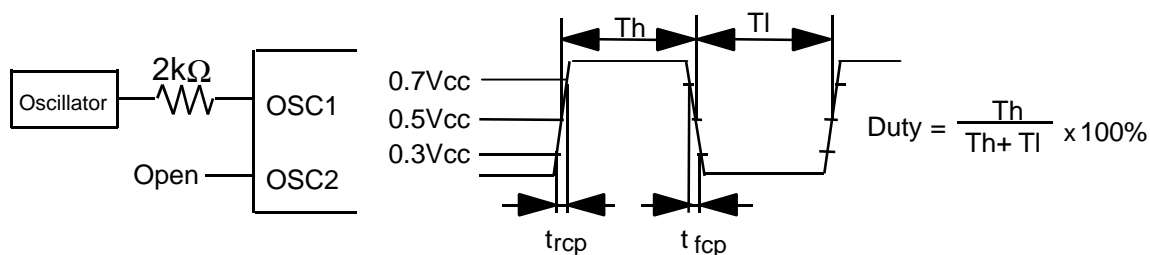


Figure 89 External Clock Supply

8. Applies to the internal oscillator operations using external oscillation resistor Rf (figure and table).

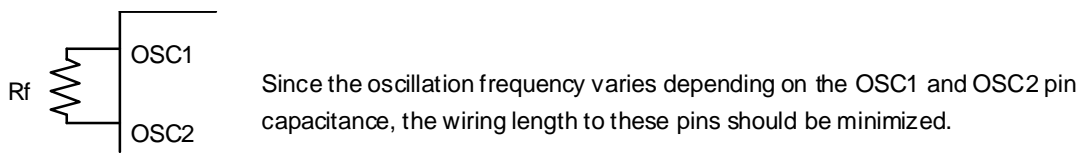
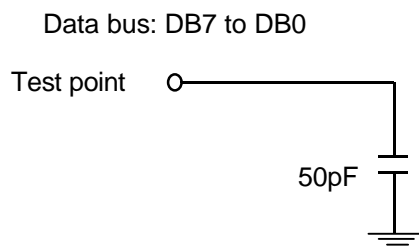


Figure 90 Internal Oscillation

Oscillation resistance (kΩ)	Vcc				
	1.7V	2.2V	2.4 V	3.0 V	3.6 V
75 kΩ	TBD	TBD	TBD	TBD	TBD
130 kΩ	TBD	TBD	TBD	TBD	TBD
180 kΩ	TBD	TBD	TBD	TBD	TBD
200 kΩ	TBD	TBD	TBD	TBD	TBD
240 kΩ	TBD	TBD	TBD	TBD	TBD
280 kΩ	TBD	TBD	TBD	TBD	TBD
360 kΩ	TBD	TBD	TBD	TBD	TBD
470 kΩ	TBD	TBD	TBD	TBD	TBD

Table 44 External Resistance Value and R-C Oscillation Frequency (Referential Data)

**AC Characteristics Test Load Circuits****Figure 91 Load Circuit**

AC Characteristics ( $V_{CC} = 1.7$  to  $3.6$  V,  $T_a = -40$  to  $+85^\circ\text{C}$  \*1)Clock Characteristics ( $V_{CC} = 1.7$  to  $3.6$  V)

Table 45

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
External clock frequency	f <sub>cp</sub>	kHz	$V_{CC} = 1.7$ to $3.6$ V	140	210	315	7
External clock duty ratio	Duty	%	$V_{CC} = 1.7$ to $3.6$ V	45	50	55	7
External clock rise time	tr <sub>cp</sub>	μs	$V_{CC} = 1.7$ to $3.6$ V	—	—	0.2	7
External clock fall time	tf <sub>cp</sub>	μs	$V_{CC} = 1.7$ to $3.6$ V	—	—	0.2	7
R-C oscillation clock	f <sub>osc</sub>	kHz	R <sub>f</sub> = 220kΩ, $V_{CC} = 3$ V	150	210	252	8

## 80-system Bus Interface Timing Characteristics

Normal Write Mode (HWM=0) ( $V_{CC} = 1.7$  to  $1.8$  V)

Table 46

Item	Symbol	Unit	Test Condition	Min	Typ	Max	
Bus cycle time	Write	t <sub>CYCW</sub>	ns	Figure 2	900	—	—
	Read	t <sub>CYCR</sub>	ns	Figure 2	1000	—	—
Write low-level pulse width		PW <sub>LW</sub>	ns	Figure 2	120	—	—
Read low-level pulse width		PW <sub>LR</sub>	ns	Figure 2	450	—	—
Write high-level pulse width		PW <sub>HW</sub>	ns	Figure 2	400	—	—
Read high-level pulse width		PW <sub>HR</sub>	ns	Figure 2	450	—	—
Write/Read rise/fall time		t <sub>WRf, WRF</sub>	ns	Figure 2	—	—	25
Setup time (RS to CS*, WR*, RD*)		t <sub>AS</sub>	ns	Figure 2	20	—	—
Address hold time		t <sub>AH</sub>	ns	Figure 2	10	—	—
Write data set up time		t <sub>DSW</sub>	ns	Figure 2	60	—	—
Write data hold time		t <sub>H</sub>	ns	Figure 2	30	—	—
Read data delay time		t <sub>DDR</sub>	ns	Figure 2	—	—	250
Read data hold time		t <sub>DHR</sub>	ns	Figure 2	10	—	—

High-Speed Write Mode (HWM=1) ( $V_{CC} = 1.7$  to  $1.8$  V)

Table 47

Item	Symbol	Unit	Test Condition	Min	Typ	Max	
Bus cycle time	Write	t <sub>CYCW</sub>	ns	Figure 2	900	—	—
	Read	t <sub>CYCR</sub>	ns	Figure 2	1000	—	—
Write low-level pulse width		PW <sub>LW</sub>	ns	Figure 2	120	—	—
Read low-level pulse width		PW <sub>LR</sub>	ns	Figure 2	450	—	—
Write high-level pulse width		PW <sub>HW</sub>	ns	Figure 2	400	—	—
Read high-level pulse width		PW <sub>HR</sub>	ns	Figure 2	450	—	—
Write/Read rise/fall time		t <sub>WRf, WRF</sub>	ns	Figure 2	—	—	25
Set up time (RS to CS*, WR*, RD*)		t <sub>AS</sub>	ns	Figure 2	20	—	—
Address hold time		t <sub>AH</sub>	ns	Figure 2	10	—	—
Write data set up time		t <sub>DSW</sub>	ns	Figure 2	60	—	—
Write data hold time		t <sub>H</sub>	ns	Figure 2	30	—	—
Read data delay time		t <sub>DDR</sub>	ns	Figure 2	—	—	250
Read data hold time		t <sub>DHR</sub>	ns	Figure 2	10	—	—

## 80-system Bus Interface Timing Characteristics

Normal Write Mode (HWM=0) (Vcc = 1.8 to 2.4 V)

Table 48

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	$t_{CYCW}$	ns	Figure 2	600	—	—
	Read	$t_{CYCR}$	ns	Figure 2	800	—	—
Write low-level pulse width		$PW_{LW}$	ns	Figure 2	90	—	—
Read low-level pulse width		$PW_{LR}$	ns	Figure 2	350	—	—
Write high-level pulse width		$PW_{HW}$	ns	Figure 2	300	—	—
Read high-level pulse width		$PW_{HR}$	ns	Figure 2	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25
Set up time (RS to CS*, WR*, RD*)		$t_{AS}$	ns	Figure 2	10	—	—
Address hold time		$t_{AH}$	ns	Figure 2	5	—	—
Write data setup time		$t_{DSW}$	ns	Figure 2	60	—	—
Write data hold time		$t_H$	ns	Figure 2	15	—	—
Read data delay time		$t_{DDR}$	ns	Figure 2	—	—	200
Read data hold time		$t_{DHR}$	ns	Figure 2	5	—	—

High-Speed Write Mode (HWM=1) (Vcc = 1.8 to 2.4V)

Table 49

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	$t_{CYCW}$	ns	Figure 2	200	—	—
	Read	$t_{CYCR}$	ns	Figure 2	800	—	—
Write low-level pulse width		$PW_{Lw}$	ns	Figure 2	90	—	—
Read low-level pulse width		$PW_{LR}$	ns	Figure 2	350	—	—
Write high -level pulse width		$PW_{HW}$	ns	Figure 2	90	—	—
Read high -level pulse width		$PW_{HR}$	ns	Figure 2	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	—
Set up time (RS to CS*, WR*, RD*)		$t_{AS}$	ns	Figure 2	10	—	—
Address hold time		$t_{AH}$	ns	Figure 2	5	—	—
Write data set up time		$t_{DSW}$	ns	Figure 2	60	—	—
Write data hold time		$t_H$	ns	Figure 2	15	—	—
Read data delay time		$t_{DDR}$	ns	Figure 2	—	—	—
Read data hold time		$t_{DHR}$	ns	Figure 2	5	—	—

Normal Write Mode (HWM=0) (V<sub>CC</sub> = 2.4 to 3.6 V)

Table 50

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t <sub>CYCW</sub>	ns	Figure 2	300	—	—
	Read	t <sub>CYCR</sub>	ns	Figure 2	500	—	—
Write low-level pulse width		PW <sub>LW</sub>	ns	Figure 2	40	—	—
Read low-level pulse width		PW <sub>LR</sub>	ns	Figure 2	250	—	—
Write high -level pulse width		PW <sub>HW</sub>	ns	Figure 2	100	—	—
Read high -level pulse width		PW <sub>HR</sub>	ns	Figure 2	200	—	—
Write/Read rise/fall time		t <sub>WR↑, WR↓</sub>	ns	Figure 2	—	—	25
Set up time (RS to CS*, WR*, RD*)		t <sub>AS</sub>	ns	Figure 2	10	—	—
Address hold time		t <sub>AH</sub>	ns	Figure 2	5	—	—
Write data set up time		t <sub>DSW</sub>	ns	Figure 2	60	—	—
Write data hold time		t <sub>H</sub>	ns	Figure 2	15	—	—
Read data delay time		t <sub>DDR</sub>	ns	Figure 2	—	—	200
Read data hold time		t <sub>DHR</sub>	ns	Figure 2	5	—	—

High-Speed Write Mode (HWM=1) (V<sub>CC</sub> = 2.4 to 3.6 V)

Table 51

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t <sub>CYCW</sub>	ns	Figure 2	100	—	—
	Read	t <sub>CYCR</sub>	ns	Figure 2	500	—	—
Write low-level pulse width		PW <sub>LW</sub>	ns	Figure 2	40	—	—
Read low-level pulse width		PW <sub>LR</sub>	ns	Figure 2	250	—	—
Write high -level pulse width		PW <sub>HW</sub>	ns	Figure 2	40	—	—
Read high -level pulse width		PW <sub>HR</sub>	ns	Figure 2	200	—	—
Write/Read rise/fall time		t <sub>WR↑, WR↓</sub>	ns	Figure 2	—	—	25
Set up time (RS to CS*, WR*, RD*)		t <sub>AS</sub>	ns	Figure 2	10	—	—
Address hold time		t <sub>AH</sub>	ns	Figure 2	5	—	—
Write data set up time		t <sub>DSW</sub>	ns	Figure 2	60	—	—
Write data hold time		t <sub>H</sub>	ns	Figure 2	15	—	—
Read data delay time		t <sub>DDR</sub>	ns	Figure 2	—	—	200
Read data hold time		t <sub>DHR</sub>	ns	Figure 2	5	—	—

## Clock Synchronized Serial Interface Timing Characteristics (Three lines system)

Table 52 (Vcc = 1.7 to 1.8 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Serial clock cycle time	t <sub>SCYC</sub>	μs	Figure 3	0.15	—	20
Serial clock high-level pulse width	t <sub>SCH</sub>	ns	Figure 3	70	—	—
Serial clock low-level pulse width	t <sub>SCL</sub>	ns	Figure 3	70	—	—
Serial clock rise/fall time	t <sub>scr, scf</sub>	ns	Figure 3	—	—	20
Chip select set up time	t <sub>CSU</sub>	ns	Figure 3	40	—	—
Chip select hold time	t <sub>CH</sub>	ns	Figure 3	320	—	—
Serial input data set up time	t <sub>SISU</sub>	ns	Figure 3	70	—	—
Serial input data hold time	t <sub>SIH</sub>	ns	Figure 3	70	—	—
Chip select high-level pulse	t <sub>CSH</sub>	ns	Figure 3	150	—	—

Table 53 (Vcc = 1.8 to 2.4 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Serial clock cycle time	t <sub>SCYC</sub>	μs	Figure 3	0.125	—	20
Serial clock high-level pulse width	t <sub>SCH</sub>	ns	Figure 3	50	—	—
Serial clock low-level pulse width	t <sub>SCL</sub>	ns	Figure 3	50	—	—
Serial clock rise/fall time	t <sub>scr, scf</sub>	ns	Figure 3	—	—	20
Chip select set up time	t <sub>CSU</sub>	ns	Figure 3	20	—	—
Chip select hold time	t <sub>CH</sub>	ns	Figure 3	280	—	—
Serial input data set up time	t <sub>SISU</sub>	ns	Figure 3	50	—	—
Serial input data hold time	t <sub>SIH</sub>	ns	Figure 3	50	—	—
Chip select high-level pulse	t <sub>CSH</sub>	ns	Figure 3	125	—	—

Table 54 (Vcc = 2.4 to 3.6 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Serial clock cycle time	t <sub>SCYC</sub>	μs	Figure 3	0.1	—	20
Serial clock high-level pulse width	t <sub>SCH</sub>	ns	Figure 3	40	—	—
Serial clock low-level pulse width	t <sub>SCL</sub>	ns	Figure 3	40	—	—
Serial clock rise/fall time	t <sub>scr, scf</sub>	ns	Figure 3	—	—	20
Chip select set up time	t <sub>CSU</sub>	ns	Figure 3	20	—	—
Chip select hold time	t <sub>CH</sub>	ns	Figure 3	200	—	—
Serial input data set up time	t <sub>SISU</sub>	ns	Figure 3	40	—	—
Serial input data hold time	t <sub>SIH</sub>	ns	Figure 3	40	—	—
Chip select high-level pulse	t <sub>CSH</sub>	ns	Figure 3	100	—	—

## Clock Synchronized Serial Interface Timing Characteristics (Four lines system)

Table 55 (V<sub>CC</sub> = 1.7 to 1.8 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Serial clock cycle time	t <sub>SCYC</sub>	μs	Figure 3	0.15	—	20
Serial clock high-level pulse width	t <sub>SCH</sub>	ns	Figure 3	70	—	—
Serial clock low-level pulse width	t <sub>SCL</sub>	ns	Figure 3	70	—	—
Serial clock rise/fall time	t <sub>scr, scf</sub>	ns	Figure 3	—	—	20
Chip select set up time	t <sub>CSU</sub>	ns	Figure 3	40	—	—
Chip select hold time	t <sub>CH</sub>	ns	Figure 3	320	—	—
Serial input data set up time	t <sub>SISU</sub>	ns	Figure 3	70	—	—
Serial input data hold time	t <sub>SIH</sub>	ns	Figure 3	70	—	—
Chip select high-level pulse	t <sub>CSH</sub>	ns	Figure 3	150	—	—

Table 56 (V<sub>CC</sub> = 1.8 to 2.4 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Serial clock cycle time	t <sub>SCYC</sub>	μs	Figure 3	0.125	—	20
Serial clock high-level pulse width	t <sub>SCH</sub>	ns	Figure 3	50	—	—
Serial clock low-level pulse width	t <sub>SCL</sub>	ns	Figure 3	50	—	—
Serial clock rise/fall time	t <sub>scr, scf</sub>	ns	Figure 3	—	—	20
Chip select set up time	t <sub>CSU</sub>	ns	Figure 3	20	—	—
Chip select hold time	t <sub>CH</sub>	ns	Figure 3	280	—	—
Serial input data set up time	t <sub>SISU</sub>	ns	Figure 3	50	—	—
Serial input data hold time	t <sub>SIH</sub>	ns	Figure 3	50	—	—
Chip select high-level pulse	t <sub>CSH</sub>	ns	Figure 3	125	—	—

Table 57 (V<sub>CC</sub> = 2.4 to 3.6 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Serial clock cycle time	t <sub>SCYC</sub>	μs	Figure 3	0.1	—	20
Serial clock high-level pulse width	t <sub>SCH</sub>	ns	Figure 3	40	—	—
Serial clock low-level pulse width	t <sub>SCL</sub>	ns	Figure 3	40	—	—
Serial clock rise/fall time	t <sub>scr, scf</sub>	ns	Figure 3	—	—	20
Chip select set up time	t <sub>CSU</sub>	ns	Figure 3	20	—	—
Chip select hold time	t <sub>CH</sub>	ns	Figure 3	200	—	—
Serial input data set up time	t <sub>SISU</sub>	ns	Figure 3	40	—	—
Serial input data hold time	t <sub>SIH</sub>	ns	Figure 3	40	—	—
Chip select high-level pulse	t <sub>CSH</sub>	ns	Figure 3	100	—	—

Reset Timing Characteristics ( $V_{CC} = 1.8$  to  $3.6$  V)

Table 58

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Reset low-level width	$t_{RES}$	ms	Figure 4	1	—	—
Reset rise time	$t_{tRES}$	$\mu$ s	Figure 4	—	—	10

80-system Bus Operation

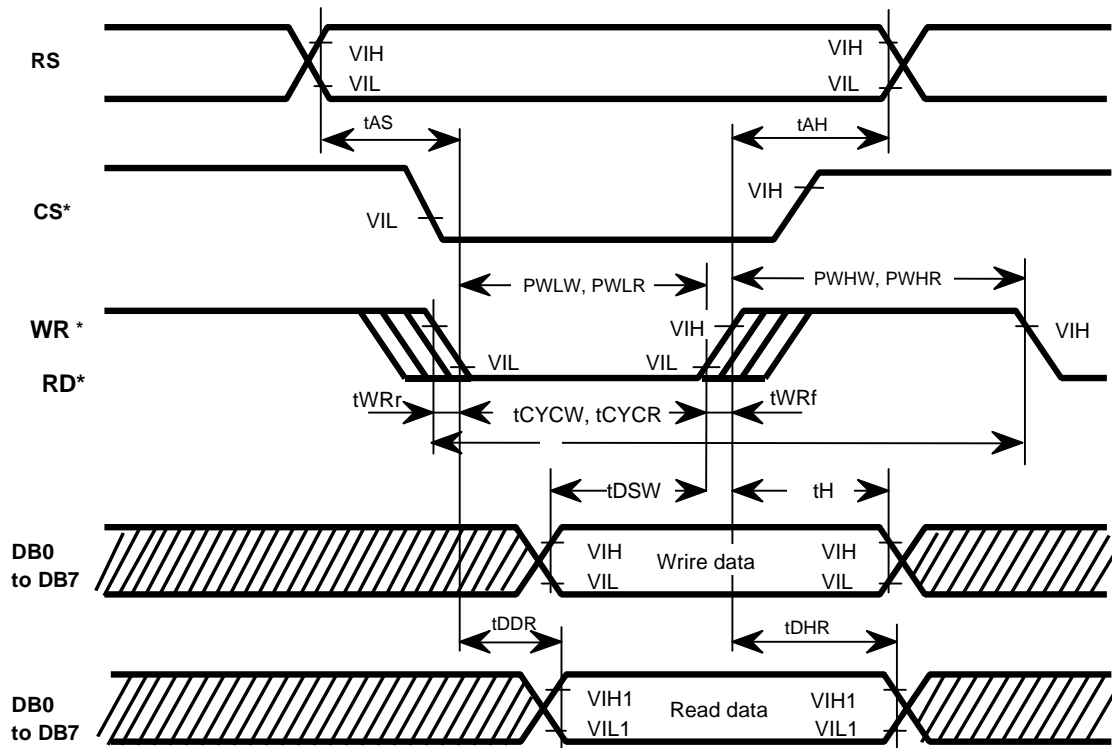


Figure 92 80-system Bus Timing

Note: PHLW and PHLR are specified in the overlapped period when CS\* is low and WR\* or RD\* is Low.

Clock Synchronized Serial Interface Operation (Three lines system)

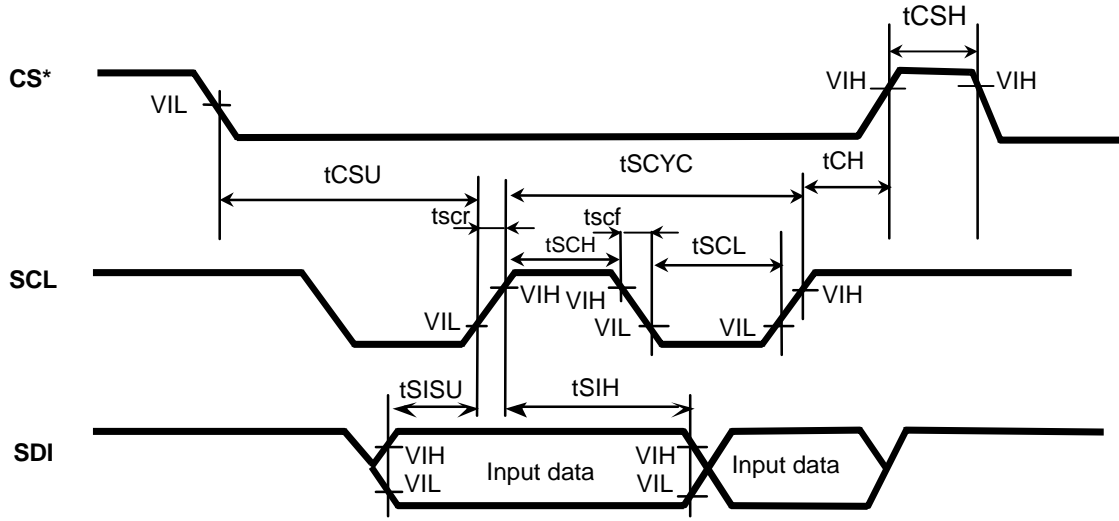


Figure 93

Clock Synchronized Serial Interface Operation (Four lines system)

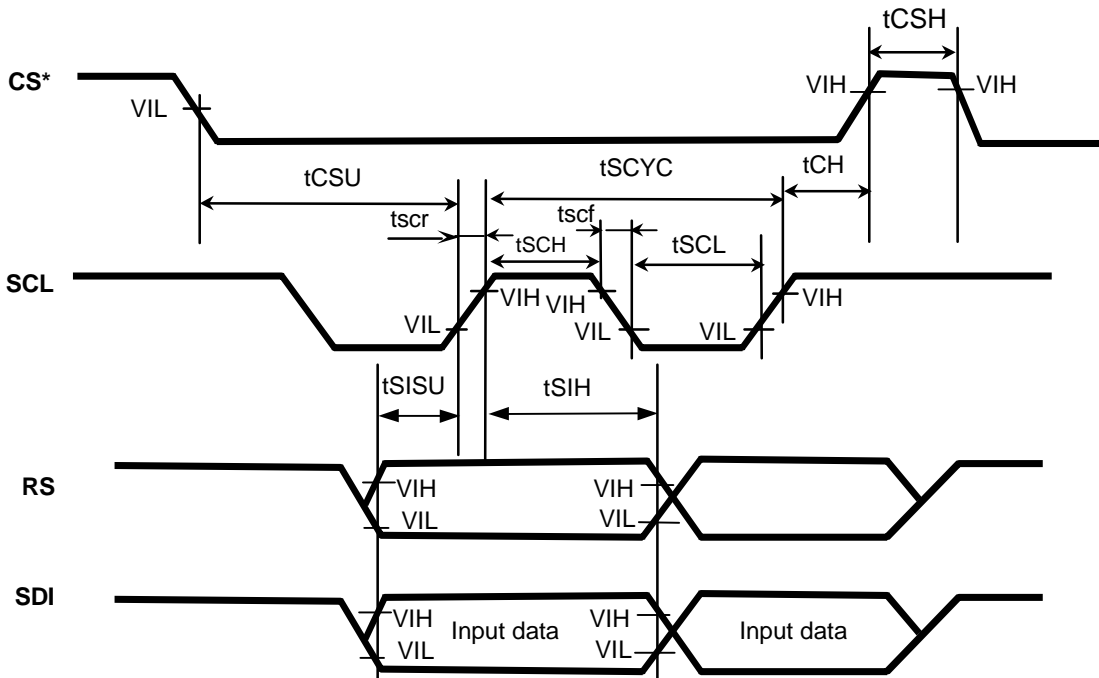


Figure 94

Reset Operation

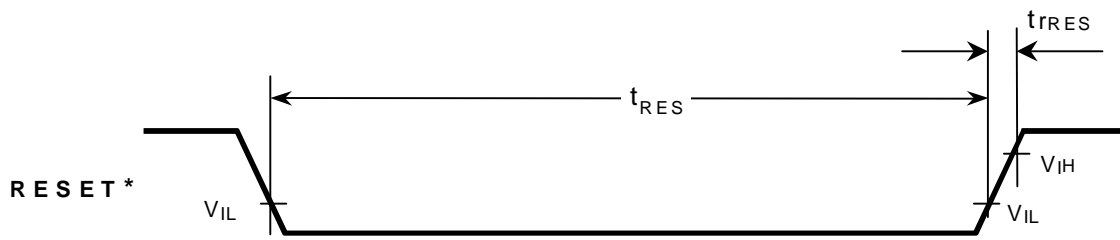


Figure 95 Reset Timing

## Revision History

Rev.	Date	Page	Contents
0.2	September 13, 2002		First Release
0.31	October 2, 2002	7	Change description in IM2-1, IM0/ID Functions from "GND/GND/Vcc" to "GND/Vcc/Vcc".
		8	Correct "HCD66768BP" to "HCD66768" in Functions of RESET1 to 3. Change "supply under 2.5 to 2.75V" to "supply 2.5 to 2.75V" in Functions of Vci1. Change "supply under 5.0 to 5.5V" to "supply 5.0 to 5.5V" in Functions of Vci2.
		10	Exchange the descriptions of Three line serial and Four lines serial (RS* and Start bytes RS Bits) in Table4.
		17	Correct digit from "000000" to "0000000" and from "111111" to "1111111" in 9-1. Index: IR. Add register W to Figure 11.
		18	Correct DB10 bit from "0" to "CSFT" in Figure 12. Correct "CSFT="1"" to "CSFT = "0"" in Note written under Figure 13.
		22	Correct "VciL" in Table 9 to "Vci1". Correct "Vci1" in Table 12 to "VciL".
		30	Correct "HSA5-0/HEA7-0" to "HSA7-0" to "HEA7-0".
		34	Correct R/W bit of Figure 29 from "W" to "R".
		36	Correct R/W bit of Figure 31 from "R" to "R/W".
		37	Correct R/W bit of Figure 32 from "R" to "W". Correct R/W bit of Figure 33 from "R" to "W". Correct "(768)" to "(HD66768)" in the description of IDX7-0. Add "Note 1" and "Note 2" to the upper right of Table 26. Correct R/W bit of R40h in Table 26 from "0" to "0/1".
		46	Correct bus width of register 1 to 4 from "48" to "64" in Figure 46.
		47	Correct the title of c) from "Example of the operation of high-speed consecutive writing to RAM" to "Example of normal writing to RAM".
		48	Exchange descriptions for RAM write and descriptions for Window address of Normal RAM Write and High-Speed RAM Write in Table 30.
		54	In Figure 53: Change the last three of Write data (2) in GRAM from "1 1 1" to "* * *".
		55	In Figure 54: Correct "AF00"H to "5300"H in Note2.
		57	In Figure 56: Correct "AF00"H to "5300"H in Note 2.
		61	Add "(Note2)" to Table 37.
		63	Change details of Figure 63 and 64.
		65	Delete "Master/slave signal" from Table 38. Delete "for the time-sharing drive" from the fourth line of Standby Mode description. Add "and stand-by cancellation instruction." to the seventh line of Standby Mode description.
		68	Delete the figure of Relationship with SEG/COM Output Level.
		69	Correct 198kHz in Example Calculation 1 to 126kHz.
		72	Add a new page "Quadruple display mode".
		75	Add a new page "Power supply level correlation".

Rev.	Date	Page	Contents
0.31	October 2, 2002	77	Change description of Caution 4 from "Generate an output voltage of V1 level within the range from VLPS to 0.5V." to "Be sure that V1 output level is set lower than (VLPS-0.5)V. (Caution 5 is changed in the same way.) Delete Caution 7.
		78	Correct "0.50" to "0.05" in the third line of the Contrast adjustment description.
		82	Add "Vcc = 1.7V" to Table 44.
		90	Correct "DB0 to DB15" to "DB0 to DB7" in Figure 92.
			Delete Note 2.