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# HD667P00

Power-Supply IC for Systems with Color-TFT Liquid Crystal Displays

HITACHI

Rev.1.0
March 2002

## Description

HD667P00 is a power-supply IC for systems with color-TFT-liquid-crystal dot-matrix graphic displays. It incorporates multiple step-up circuits, regulators, and operational amplifiers, and generates power-supply voltages of the source driver or gate driver from Vcc, Vci, or GND.

When used with the HD66770 396-channel source driver with on-chip RAM, and HD66771 228-channel gate driver this LSI is suitable for color TFT displays of cellular phones with 132-by-176 dots and it enables low-power consumption.

## Features

- Structure for TFT-display retention volume
  - — Cst/Cadd structure
- Alternating functions for TFT-display counter-electrode power supply
  - — N-line alternating drive of Vcom (Vgoff is also available for N-line alternating drive for Cadd)
  - — Adjustment of Vcom (Vgoff) amplitude: internal 22-level digital potentiometer
- Internal power-supply circuit
  - — Step-up circuit: five to nine times, positive-polarity inversion
- Mode setting
  - — Serial transfer from the HD66770 source driver
- Low-power consumption
  - — Equalizing function for the switching performance of step-up circuits and operational amplifiers
- Input power-supply voltage
  - — Vcc - GND = 1.8 to 3.3 V
  - — Vci - GND = 2.5 to 3.3 V (internal reference power-supply voltage)

- Output power-supply voltage
  - For the source driver: DDVDH - GND = 4.5 to 5.5 V (power supply for HD66770 liquid crystal output circuits),VDH - GND = 4.0 to 5.0 V (reference power supply for HD66770 grayscale voltages)
  - For the gate driver: VGH - GND = +9.0 to +16.5 V, VGL - GND = -16.5 to –9.0 V, Vgoff - GND = -16.0 to -5.0 V
  - For the TFT-display counter electrode: Vcom amplitude = 6 V (max), VcomH - GND = VDH (max), VcomL - GND = Vci + 0.5 to 1.0V (max)

## Type Number

| Type Number | External Appearance |
|---|---|
| HCD667P00BP | Die with Au bump |

## Pin Functions

**Table 1 Pin Functions**

| Signal Name | Quantity* | Input/ Output | Connected to | Function |
|---|---|---|---|---|
| Vcc | 2 | Input | Power supply | VCC-GND: a logic-circuit power supply. Supply the same voltage as that for HD66770 and HD66771. |
| GND | 2 | Input | Power supply | |
| VDH | 1 | Output | Capacitor for stabilization, HD66770 | A reference power supply for the HD66770 source-driver grayscale voltage. Outputs a regulated voltage input in VREG1. Adjust the VDH level with VREG1 because the VREG1 input voltage is output as the output level. Connect a capacitor for stabilization. |
| VGH | 1 | Input | VLOUT2 or power supply, and HD66771 | A positive side power supply for HD66771, gate driver. Connect VLOUT2. When VLOUT2 is not used, connect an external-voltage power supply lower than 16.5 V. |
| VGL | 1 | Input | VLOUT3 or power supply, and HD66771 | A negative side power supply for HD66771, gate driver. Connect VLOUT3. When VLOUT3 is not used, connect an external-voltage power supply higher than -16.5 V. |
| Vci | 1 | Input | Power supply | A power supply for an analogue circuit. Connect a 2.5- to 3.3-V external-voltage power supply. |
| Vciout | 1 | Output | Vci1 and capacitor for stabilization, or open | Outputs the internal reference voltage generated between Vci and GND. The internal reference voltage can be set by a register. |
| Vci1 | 1 | Input | VciOUT or power supply | A step-up voltage for step-up circuit 1. Connect VciOUT to lower than 2.75V or external power supply. |
| VLOUT1 | 1 | Output | DDVDH and capacitor for stabilization, or open | Outputs a voltage that doubles or triples the voltage from step-up voltage Vci1. The step-up factor can be set in an internal register. Connect a capacitor for stabilization. When this pin is not used, leave it open. |

**Table 1 Pin Functions (cont)**

| Signal Name | Quantity* | Input/ Output | Connected to | Function |
|---|---|---|---|---|
| DDVDH | 1 | Input | VLOUT1 or power supply, and HD66770 | A power supply for outputting the HD66770 source driver. Connect this pin to VLOUT1. When VLOUT1 is not used, connect an external power supply lower than 5.5 V. |
| Vci2 | 1 | Input | VLOUT1 or power supply | A reference voltage in step-up circuit 2. Connect this pin to VLOUT1. When VLOUT1 is not used, connect an external power supply lower than 5.5 V. |
| VLOUT2 | 1 | Output | VGH and capacitor for stabilization, or open | Output a voltage that doubles, triples, or quadruples, outputs a voltage between DDVDH and GND in step-up circuit 2. The step-up factor can be set in an internal register. Connect a capacitor for stabilization. When this pin is not used, leave it open. |
| Vci3 | 1 | Input | VLOUT2 or power supply | A reference voltage in step-up circuit 3. Connect this pin to VLOUT2. When VLOUT2 is not used, connect an external power supply lower than 16.5 V. |
| VLOUT3 | 1 | Output | VGL and capacitor for stabilization, or open | Outputs a voltage between VLOUT2 and GND as an equivalent negative voltage in step-up circuit 3. Connect a capacitor for stabilization. When this pin is not used, leave it open. |
| Vci4 | 1 | Input | Vci or power supply | A reference voltage in step-up circuit 4. Connect Vci, or an external power supply lower than 2.5 to 3.3 V. |
| VLOUT4 | 1 | Output | VCL and capacitor for stabilization, or open | Outputs a voltage between Vci4 and GND as an equivalent negative voltage in step-up circuit 4. Connect a capacitor for stabilization and the VCL pin. When this pin is not used, leave it open. |
| VCL | 1 | Input | VLOUT4 or power supply | A power supply for generating VcomL. When VcomL is a negative voltage, connect VLOUT4 or an external power supply higher than –3.3 V. When VcomL is higher than GND, connect GND. |

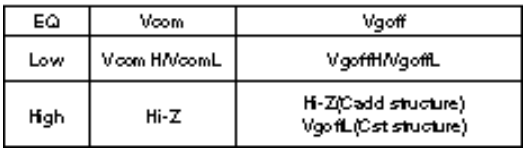
**Table 1 Pin Functions (cont)**

| Signal Name | Quantity* | Input/ Output | Connected to | Function |
|---|---|---|---|---|
| VREG1OUT | 1 | Output | Capacitor for stabilization and VREG1, or open | This pin generates and outputs a reference voltage for VREG1 between DDVDH and GND from the reference voltage between Vci and GND that is internally generated. The step-up factor can be set in an internal register. Connect this pin to VREG1 and a capacitor for stabilization. When this pin is not used, leave it open. |
| VREG1 | 1 | Input | VREG1OUT or power supply | A reference voltage for generating VDH or Vcom. Connect VREG1OUT. When VREG1OUT is not used, connect an external power supply lower than DDVDH. |
| VREG2OUT | 1 | Output | Capacitor for stabilization and VREG2, or open | This pin generates and outputs a reference voltage for VREG2 between GND and VGL from the reference voltage between Vci and GND that is internally generated. The step-up factor can be set in an internal register. Connect this pin to VREG2 and a capacitor for stabilization. When this pin is not used, leave it open. |
| VREG2 | 1 | Input | VREG2OUT or power supply | A reference voltage for generating Vgoff. Connect VREG2OUT. When VREG2OUT is not used, connect an external power supply lower than VGL. |
| C11+, C11- to C23+, C23- | 10 | - | Step-up capacitor | Connect the step-up capacitors according to the step-up factor. When the internal step-up circuit is not used, leave this pin open. |
| C31+, C31- | 2 | - | Step-up capacitor | Connect a step-up capacitor for generating the VGL level from the VGH and GND levels. When the internal step-up circuit is not used, leave these pins open. |
| C41+, C41- | 2 | - | Step-up capacitor | Connect a step-up capacitor for generating the –Vci4 level from the Vci4 and GND levels. When the internal step-up circuit is not used, leave these pins open. |
| Vcom | 1 | Output | TFT-display counter electrode | A power supply for the TFT-display counter electrode. When the reversing Vcom alternation is not driven, the amplitude between VcomH and VcomL is output. The alternating cycle can be set by the M pin. Connect this pin to the TFT-display counter electrode. |

**Table 1 Pin Functions (cont)**

| Signal Name | Quantity* | Input/ Output | Connected to | Function |
|---|---|---|---|---|
| VcomR | 1 | Input | Variable resistor or open | A reference voltage of VcomH. When VcomH is externally adjusted, halt the internal adjuster of VcomH by setting the register and insert a variable resistor between VDH and GND. When this pin is not externally adjusted, leave it open and adjust VcomH by setting the internal register. |
| VcomH | 1 | Output | Capacitor for stabilization | This pin indicates a high level of Vcom generated in driving the Vcom alternation. Connect this pin to the capacitor for stabilization. |
| VcomL | 1 | Output | Capacitor for stabilization or open | The Vcom voltage when the Vcom alternation is not driven. When the Vcom alternation is driven, this pin indicates a low level of Vcom. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VcomL output stops and a capacitor for stabilization is not needed. |
| Vgoff | 1 | Output | HD66771 | A power supply for driving the gate line of the HD66771 gate driver. This pin is a negative voltage at the TFT-gate off level. Alternation can be driven by synchronizing Vcom with the setting of the internal register. Set the internal register according to the structure of the TFT-display retention volume. For the amplitude at the alternation driving, this pin outputs a voltage between VcomH and VcomL with the VgoffL reference voltage. Connect this pin to HD66771. |
| VgoffH | 1 | Output | Capacitor for stabilization or open | When the Vgoff alternation is driven, this pin indicates a high level of Vgoff. Connect this pin to a capacitor for stabilization. When the CAD bit is low, the VgoffH output stops and a capacitor for stabilization is not needed. |
| VgoffL | 1 | Output | Capacitor for stabilization | The Vgoff voltage when the Vgoff alternation is not driven. When the Vgoff alternation is driven, this pin indicates a low level of Vgoff. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization. |
| REGN, REGP | 2 | Input/ output | Open or Capacitor for stabilization | TEST pins for VREG1OUT, Vciout, and VREG2OUT. Leave these pins open or connect a capacitor for stabilization according to the display quality. |

**Table 1 Pin Functions (cont)**

| Signal Name | Quantity* | Input/ Output | Connected to | Function |
|---|---|---|---|---|
| M | 1 | Input | M of HD66770 | Inputs current-alternating signals of Vcom and Vgoff. The following levels are output according to the status of M:<br>Low: VcomL or VgoffL, high: VcomH or VgoffH<br>When the VCOMG bit is low, the VcomL output stops and the low level of Vcom is output as GND. When the CAD bit is low, the VgoffH output stops. |
| EQ | 1 | Input | EQ of HD66770 or GND | When the Vcom alternation is driven, the output of Vcom and Vgoff are Hi-Z at the transition timing of Vcom and Vgoff. The following levels are output according to the status of EQ:<br>  <br>Note: When EQ = high, the output status of Vgoff depends on the mode setting of the structure of the TFT-display retention volume. For the mode setting, refer to the Instructions section. When EQ is not used, connect this pin to GND. |
| DCCLK | 1 | Input | DCCLK of HD66770 | A clock for the step-up circuits supplied from HD66770. |
| GCL | 1 | Input | GCL of HD66770 | Operates as a clock for the transfer of register settings. Latches data on the rising edge of the clock. |
| GDA | 1 | Input | GDA of HD66770 | Operates as the data for the transfer of register settings. |
| GCS* | 1 | Input | GCS* of HD66770 | A chip-select signal.<br>Low: selected (data-transfer enabled), high: not selected (data-transfer disabled) |
| RESET* | 1 | Input | External reset circuit | The reset pin. When a low level is input here, the LSI is initialized. Be sure to apply a signal to this pin after the system's power-on reset. |
| TESTA1 | 1 | Input/ output | Test pin | A test pin for the VcomH output. Leave it open or connect a capacitor for stabilization according to the display quality. |
| TESTA2 | 1 | Input/ output | Test pin | A test pin for the VcomL output. Leave it open or connect a capacitor for stabilization according to the display quality. |
| TESTA3 | 1 | Input/ output | Test pin | A test pin for the VgoffH output. Leave it open or connect a capacitor for stabilization according to the display quality. |



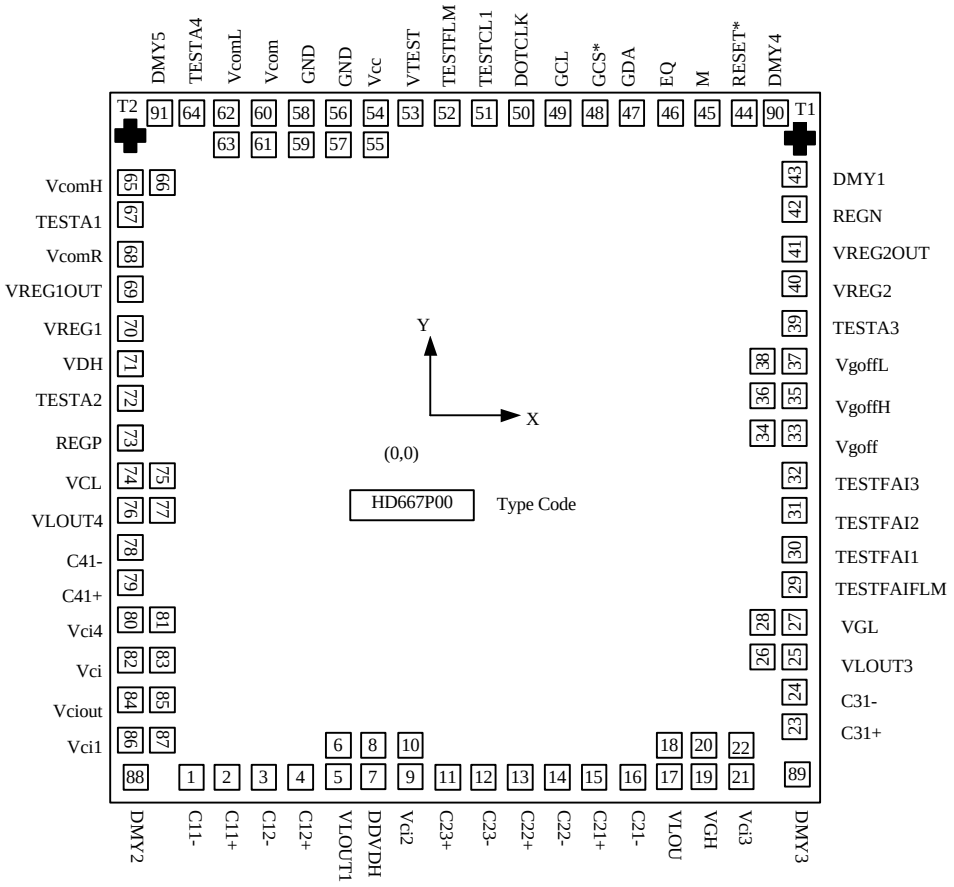
| EQ | Vcom | Vgoff |
|---|---|---|
| Low | Vcom H/VcomL | VgoffH/VgoffL |
| High | Hi-Z | Hi-Z(Cadd structure)<br>VgoffL(Cst structure) |

**Table 1 Pin Functions (cont)**

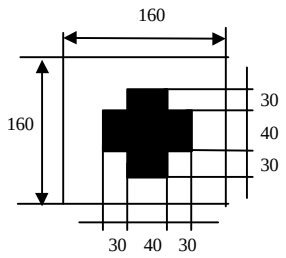
| Signal Name | Quantity* | Input/ Output | Connected to | Function |
|---|---|---|---|---|
| TESTA4 | 1 | Input/ output | Test pin | A test pin for the VcomL output. Leave it open or connect a capacitor for stabilization according to the display quality. |
| VTEST | 1 | Input | Test pin | A test pin. Must be left open. |
| TESTFLM | 1 | Input | Test pin | A test pin. Must be shorted to GND. |
| TESTCL1 | 1 | Input | Test pin | A test pin. Must be shorted to GND. |
| TESFAIFLM | 1 | Output | Test pin | A test pin. Must be left open. |
| TESTFAI1 | 1 | Output | Test pin | A test pin. Must be left open. |
| TESTFAI2 | 1 | Output | Test pin | A test pin. Must be left open. |
| TESTFAI3 | 1 | Output | Test pin | A test pin. Must be left open. |

Note: The quantity does not match the number of pads.

## HCD667P00BP Pad Arrangement




-Chip size: 3.8mm x 3.8mm
-Chip thickness: 550µm (typ.)
-Pad coordinates, Coordinate origin: Chip center
-Au bump size: See the following
(1) 80µmx80µm: pads No.1 to No.87
(2) 40µmx40µm: pads No.88 (DMY2) to No.91 (DMY5)
-Au bump pitch: See the pad coordinates
-Hight of the Au bump: 15µm (typ)
The target (T1 or T2) pattern for the chip alignment AL without the Au bump.
-The sizes are shown below.




Note: Although the DMY pad is designed as an open pad, the open check for manufacturing has not been performed. Therefore, when the chip is assembled, do not connect the dummy pads to the power supply, signal lines, or other dummy pads.

## HCD667P00BP Pad Coordinates

The pad coordinates are shown below. The pad numbers in the pad arrangement correspond to the numbers in the following table that lists the pad center coordinates with the chip-centered origin.

[µm]

| No. | Pin Name | X | Y | Bump Size |
|---|---|---|---|---|
| 1 | C11- | -1500 | -1737 | 80 x 80 µm |
| 2 | C11+ | -1300 | -1737 | 80 x 80 µm |
| 3 | C12- | -1100 | -1737 | 80 x 80 µm |
| 4 | C12+ | -900 | -1737 | 80 x 80 µm |
| 5 | VLOUT1 | -700 | -1737 | 80 x 80 µm |
| 6 | VLOUT1 | -700 | -1627 | 80 x 80 µm |
| 7 | DDVDH | -500 | -1737 | 80 x 80 µm |
| 8 | DDVDH | -500 | -1627 | 80 x 80 µm |
| 9 | Vci2 | -300 | -1737 | 80 x 80 µm |
| 10 | Vci2 | -300 | -1627 | 80 x 80 µm |
| 11 | C23+ | -100 | -1737 | 80 x 80 µm |
| 12 | C23- | 100 | -1737 | 80 x 80 µm |
| 13 | C22+ | 300 | -1737 | 80 x 80 µm |
| 14 | C22- | 500 | -1737 | 80 x 80 µm |
| 15 | C21+ | 700 | -1737 | 80 x 80 µm |
| 16 | C21- | 900 | -1737 | 80 x 80 µm |
| 17 | VLOUT2 | 1100 | -1737 | 80 x 80 µm |
| 18 | VLOUT2 | 1100 | -1627 | 80 x 80 µm |
| 19 | VGH | 1300 | -1737 | 80 x 80 µm |
| 20 | VGH | 1300 | -1627 | 80 x 80 µm |
| 21 | Vci3 | 1500 | -1737 | 80 x 80 µm |
| 22 | Vci3 | 1500 | -1627 | 80 x 80 µm |
| 23 | C31+ | 1737 | -1500 | 80 x 80 µm |
| 24 | C31- | 1737 | -1300 | 80 x 80 µm |
| 25 | VLOUT3 | 1737 | -1100 | 80 x 80 µm |
| 26 | VLOUT3 | 1627 | -1100 | 80 x 80 µm |
| 27 | VGL | 1737 | -900 | 80 x 80 µm |
| 28 | VGL | 1627 | -900 | 80 x 80 µm |
| 29 | TESTFAIFLM | 1737 | -700 | 80 x 80 µm |
| 30 | TESTFAI1 | 1737 | -500 | 80 x 80 µm |
| 31 | TESTFAI2 | 1737 | -300 | 80 x 80 µm |
| 32 | TESTFAI3 | 1737 | -100 | 80 x 80 µm |
| 33 | Vgoff | 1737 | 100 | 80 x 80 µm |
| 34 | Vgoff | 1627 | 100 | 80 x 80 µm |
| 35 | VgoffH | 1737 | 300 | 80 x 80 µm |
| 36 | VgoffH | 1627 | 300 | 80 x 80 µm |
| 37 | VgoffL | 1737 | 500 | 80 x 80 µm |
| 38 | VgoffL | 1627 | 500 | 80 x 80 µm |
| 39 | TESTA3 | 1737 | 700 | 80 x 80 µm |
| 40 | VREG2 | 1737 | 900 | 80 x 80 µm |
| 41 | VREG2OUT | 1737 | 1100 | 80 x 80 µm |
| 42 | REGN | 1737 | 1300 | 80 x 80 µm |
| 43 | DMY1 | 1737 | 1500 | 80 x 80 µm |

| No. | Alignment Target | X | Y | Notes |
|---|---|---|---|---|
| T1 | Right | 1694 | 1641 | |
| T2 | Left | -1694 | 1641 | |

| No. | Pin Name | X | Y | Bump Size |
|---|---|---|---|---|
| 44 | RESET* | 1500 | 1737 | 80 x 80 µm |
| 45 | M | 1300 | 1737 | 80 x 80 µm |
| 46 | EQ | 1100 | 1737 | 80 x 80 µm |
| 47 | GDA | 900 | 1737 | 80 x 80 µm |
| 48 | GCS* | 700 | 1737 | 80 x 80 µm |
| 49 | GCL | 500 | 1737 | 80 x 80 µm |
| 50 | DOCLK | 300 | 1737 | 80 x 80 µm |
| 51 | TESTCL1 | 100 | 1737 | 80 x 80 µm |
| 52 | TESTFLM | -100 | 1737 | 80 x 80 µm |
| 53 | VTEST | -300 | 1737 | 80 x 80 µm |
| 54 | Vcc | -500 | 1737 | 80 x 80 µm |
| 55 | Vcc | -500 | 1627 | 80 x 80 µm |
| 56 | GND | -700 | 1737 | 80 x 80 µm |
| 57 | GND | -700 | 1627 | 80 x 80 µm |
| 58 | GND | -900 | 1737 | 80 x 80 µm |
| 59 | GND | -900 | 1627 | 80 x 80 µm |
| 60 | Vcom | -1100 | 1737 | 80 x 80 µm |
| 61 | Vcom | -1100 | 1627 | 80 x 80 µm |
| 62 | VcomL | -1300 | 1737 | 80 x 80 µm |
| 63 | VcomL | -1300 | 1627 | 80 x 80 µm |
| 64 | TESTA4 | -1500 | 1737 | 80 x 80 µm |
| 65 | VcomH | -1737 | 1500 | 80 x 80 µm |
| 66 | VcomH | -1627 | 1500 | 80 x 80 µm |
| 67 | TESTA1 | -1737 | 1300 | 80 x 80 µm |
| 68 | VcomR | -1737 | 1100 | 80 x 80 µm |
| 69 | VREG1OUT | -1737 | 900 | 80 x 80 µm |
| 70 | VREG1 | -1737 | 700 | 80 x 80 µm |
| 71 | VDH | -1737 | 500 | 80 x 80 µm |
| 72 | TESTA2 | -1737 | 300 | 80 x 80 µm |
| 73 | REGP | -1737 | 100 | 80 x 80 µm |
| 74 | VCL | -1737 | -100 | 80 x 80 µm |
| 75 | VCL | -1627 | -100 | 80 x 80 µm |
| 76 | VLOUT4 | -1737 | -300 | 80 x 80 µm |
| 77 | VLOUT4 | -1627 | -300 | 80 x 80 µm |
| 78 | C41- | -1737 | -500 | 80 x 80 µm |
| 79 | C41+ | -1737 | -700 | 80 x 80 µm |
| 80 | Vci4 | -1737 | -900 | 80 x 80 µm |
| 81 | Vci4 | -1627 | -900 | 80 x 80 µm |
| 82 | Vci | -1737 | -1100 | 80 x 80 µm |
| 83 | Vci | -1627 | -1100 | 80 x 80 µm |
| 84 | Vciout | -1737 | -1300 | 80 x 80 µm |
| 85 | Vciout | -1627 | -1300 | 80 x 80 µm |
| 86 | Vci1 | -1737 | -1500 | 80 x 80 µm |
| 87 | Vci1 | -1627 | -1500 | 80 x 80 µm |

| No. | Pin Name | X | Y | Bump Size |
|---|---|---|---|---|
| 88 | DMY2 | -1757 | -1757 | 40 x 40 µm |
| 89 | DMY3 | 1757 | -1757 | 40 x 40 µm |
| 90 | DMY4 | 1757 | 1757 | 40 x 40 µm |
| 91 | DMY5 | -1757 | 1757 | 40 x 40 µm |

## Internal Block Diagram

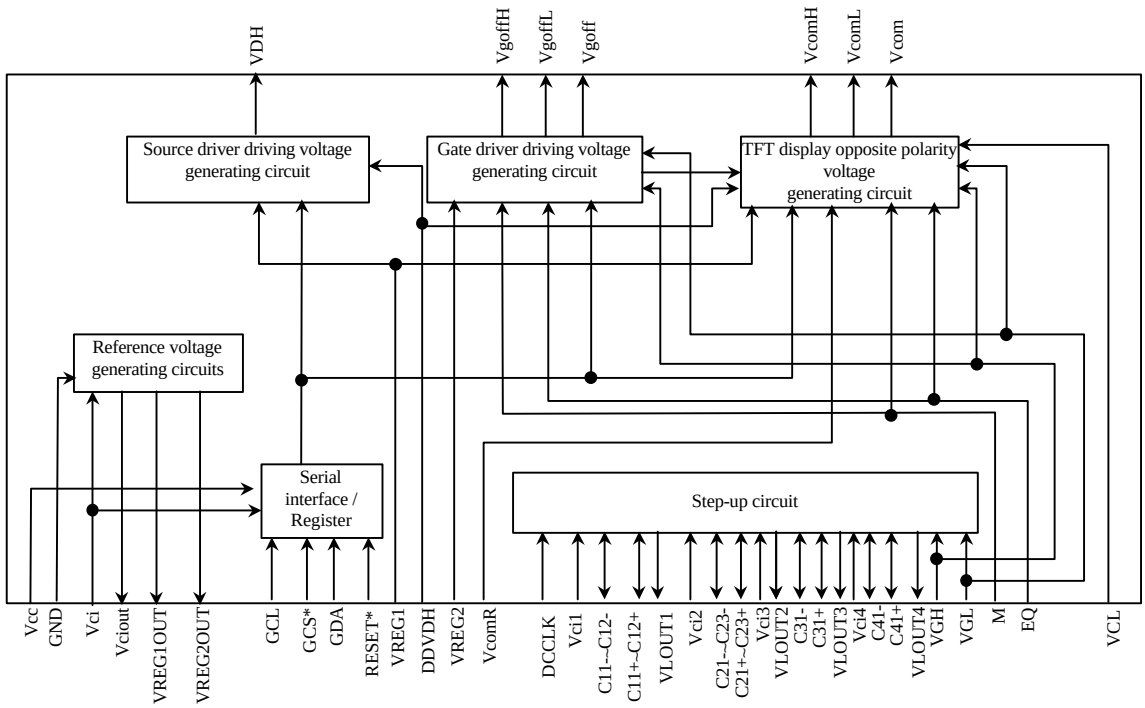



**Figure 1 Block Diagram**

## Block Functions

1. Step-up circuit

Boosts the Vci1 voltage five to nine times. The required voltage is generated by combining double or triple step-up circuit 1 and double, triple, or quadruple step-up circuit 2. The factor is controlled by the register settings. A negative-polarity voltage is also generated according to the boosted voltage. For details on the register settings for the factor, refer to the Instructions section.

2. Reference-voltage generation circuit

Generates internal reference voltages for the source-driver driving voltage generation circuit, gate-driver driving voltage generation circuit, and TFT-display counter-electrode voltage generation circuit, from the Vci voltage. The internal reference voltage is controlled by the register settings. For details on the register settings for the internal reference voltage, refer to the Instructions section.

3. Serial interface/register circuit

Transfers data to the internal control registers.

4. Source-driver driving voltage generation circuit

Generates VDH to be supplied to the source driver from VREG1. A voltage set for VREG1 is output as an output voltage for VDH.

5. TFT-display counter-electrode voltage generation circuit

Generates Vcom to be supplied to the TFT-display counter electrode from VREG1, and alternates Vcom between the VcomH and VcomL levels in any amplitude by an alternating signal. The amplitude can be adjusted by using the register settings. For details on the register settings, refer to the Instructions section.

6. Gate-driver driving voltage generation circuit

Generates Vgoff to be supplied to the gate driver from VREG2, and alternates Vgoff between the VgoffH and VgoffL levels in the same amplitude as that of Vcom by an alternating signal. The amplitude can be controlled in the Vgoff level by the register settings. For details on the register settings of Vgoff, refer to the Instructions section.

## Instructions

### Outline

HD667P00 has three internal registers. The data is written on to these registers by using a gate serial data interface. This interface can be directly connected to the HD66770 source driver for an automatic transfer of instructions. When an instruction is written on to HD66770 via the bus from the CPU, it is output from the serial interface of HD66770, and HD667P00 receives the instruction to adjust the settings of one of its internal registers.

In the bit configuration for the transfer of instructions, the upper three bits are index numbers that indicate the target register of the transfer, and the lower 13 bits are the data. This interface is common for HD66771 and HD667P00. Index numbers R00h to R02h are instructions for HD667P00, and numbers R06h to R07h are instructions for HD66771.

### Detailed Description

**Power Control 1 (R00h)**

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Index code | 0 | 0 | 0 | 0 | GON | VCOMG | BT2 | BT1 | BT0 | DC2 | DC1 | DC0 | AP2 | AP1 | AP0 | SLP |

**Figure 2 Power Control 1 Instructions**

**BT2-0:** Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power-supply voltage to be used. Set the output of VLOUT1 to 5.5 V or lower.

**DC2-0:** Set the step-up cycle of the step-up circuit. When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

**AP2-0:** Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuit increases. Adjust the current taking into account the power-supply ability for each driver and the power consumption. During times when there is no display, such as when the system is in a sleep mode, AP2-0 can be set to (0, 0, 0) and the power consumption can be reduced by shutting down the operational amplifier.

**SLP:** Sets the sleep mode. When SLP = 1, bits AP2-0 are all fixed to 0. This stops the operation of the power-supply circuit. The state of the SLP bit does not change the values of these bits.

**GON:** Sets the Vcom and Vgoff outputs. When GON = 0, the Vcom and Vgoff outputs are fixed to GND.

**VCOMG:** When VCOMG = 0, the low-level voltage of Vcom becomes GND, and the amplifier for the negative voltage and a step-up circuit 4 stop. This enables low-power consumption. When VCOMG = 1, a positive or a negative voltage (–Vci + 0.5 V to 1.0V) of VcomL can be output. When VCOMG = 1, follow the Flow of Power Supply Setting. When VCOMG = 0, if the Vcom alternation is driven, the settings of VDV4-0 become invalid. Adjust the alternating amplitudes of Vcom and Vgoff with VCM4-0 in the VcomH settings.

**Table 2 BT Bits and VLOUT1 and VLOUT2 Outputs**

| BT2 | BT1 | BT0 | VLOUT1 Output | VLOUT2 Output | Notes* |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 2 x Vci1 | 3 x Vci2 | VLOUT2 = Vci1 x six times |
| 0 | 0 | 1 | 2 x Vci1 | 4 x Vci2 | VLOUT2 = Vci1 x eight times |
| 0 | 1 | 0 | 3 x Vci1 | 3 x Vci2 | VLOUT2 = Vci1 x nine times |
| 0 | 1 | 1 | 3 x Vci1 | 2 x Vci2 | VLOUT2 = Vci1 x six times |
| 1 | 0 | 0 | 2 x Vci1 | Vci1 + 2 x Vci2 | VLOUT2 = Vci1 x five times |
| 1 | 0 | 1 | 2 x Vci1 | Vci1 + 3 x Vci2 | VLOUT2 = Vci1 x seven times |
| 1 | 1 | 0 | Step-up stopped | 3 x Vci2 | VLOUT2 = Vci2 x three times |
| 1 | 1 | 1 | Step-up stopped | 4 x Vci2 | VLOUT2 = Vci2 x four times |

Note: The step-up factors of VLOUT2 are derived from Vci1 when VLOUT1 and Vci2 are shorted. The conditions of VLOUT1 ≤ 5.5 V and VLOUT2 ≤ 16.5 V must be satisfied.

**Table 3 DC Bits and Step-up Cycle**

| DC2 | DC1 | DC0 | Step-up Cycle in Step-up Circuit 1 | Step-up Cycle in Step-up Circuits 2/3/4 |
|---|---|---|---|---|
| 0 | 0 | 0 | DCCLK | DCCLK divided by four |
| 0 | 0 | 1 | DCCLK divided by two | DCCLK divided by four |
| 0 | 1 | 0 | DCCLK divided by four | DCCLK divided by four |
| 0 | 1 | 1 | DCCLK divided by two | DCCLK divided by 16 |
| 1 | 0 | 0 | DCCLK | DCCLK divided by eight |
| 1 | 0 | 1 | DCCLK divided by two | DCCLK divided by eight |
| 1 | 1 | 0 | DCCLK divided by four | DCCLK divided by eight |
| 1 | 1 | 1 | DCCLK divided by four | DCCLK divided by 16 |

**Table 4 AP Bits and Amount of Current in Operational Amplifier**

| AP2 | AP1 | AP0 | Amount of Current in Operational Amplifier |
|---|---|---|---|
| 0 | 0 | 0 | Operation of the operational amplifier and step-up circuit stops. |
| 0 | 0 | 1 | Small |
| 0 | 1 | 0 | Small or medium |
| 0 | 1 | 1 | Medium |
| 1 | 0 | 0 | Medium or large |
| 1 | 0 | 1 | Large |
| 1 | 1 | 0 | Setting inhibited |
| 1 | 1 | 1 | Setting inhibited |

**Voltage Setting 1 (R01h)**

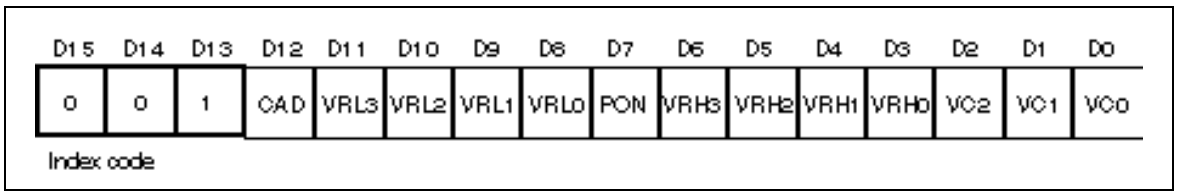



**Figure 3 Voltage Setting 1 Instructions**

**VC2-0:** Adjust each reference voltage for the VREG1OUT, VREG2OUT, and Vciout voltages to a fraction of Vci.

**PON:** Starts operation of step-up circuit 3. The operation stops when PON = 0 and starts when PON = 1. For the timing when PON = 1, refer to the Flow of Power-Supply Setting section.

**VRH3-0:** Set the amplified factor of the VREG1OUT voltage (the voltage for the VREG1 reference voltage when the VDH and Vcom amplification is generated). These bits amplify the VREG1OUT voltage 1.45 to 2.85 times the voltage set by VC2-0.

**VRL3-0:** Set the amplified factor of the VREG2OUT voltage (the voltage for the VREG2 reference voltage when Vgoff is generated). These bits amplify the VREG2OUT voltage -3 to -9.5 times the voltage set by VC2-0. Note that the reference voltage of VREG2OUT is Vci.

**CAD:** Set this bit according to the structure for the TFT-display retention volume.
CAD = 0: Set this bit when the Cst retention volume is structured. Vgoff outputs the VgoffL level regardless of the Vcom alternating drive.
**CAD = 1**: Set this bit when the Cadd retention volume is structured. At the Vcom alternating drive, the Vgoff voltage is output in the VgoffL voltage reference by the amount of Vcom alternating amplitude.

**Table 5 VC Settings and Internal Reference Voltage**

| VC2 | VC1 | VC0 | VREG1OUT (Reference Voltage) VciOUT (Reference Volatage) (Output Voltage of REGP) | VREG2OUT (Reference Voltage) (Output Voltage of REGN) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0.92 x Vci | 0.08 x Vci |
| 0 | 0 | 1 | 0.83 x Vci | 0.17 x Vci |
| 0 | 1 | 0 | 0.73 x Vci | 0.27 x Vci |
| 0 | 1 | 1 | 0.68 x Vci | 0.32 x Vci |
| 1 | * | * | Setting inhibited | Setting inhibited |

Note: Leave REGP pin and REGN pin open because the setting voltage above is output for these pins.

**Table 6 VRH Bits and VREG1OUT Voltage**

| VRH3 | VRH2 | VRH1 | VRH0 | VREG1OUT Voltage |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | REGP x 1.45 times |
| 0 | 0 | 0 | 1 | REGP x 1.55 times |
| 0 | 0 | 1 | 0 | REGP x 1.65 times |
| 0 | 0 | 1 | 1 | REGP x 1.75 times |
| 0 | 1 | 0 | 0 | REGP x 1.80 times |
| 0 | 1 | 0 | 1 | REGP x 1.85 times |
| 0 | 1 | 1 | 0 | REGP x 1.90 times |
| 0 | 1 | 1 | 1 | Stopped |
| 1 | 0 | 0 | 0 | REGP x 2.175 times |
| 1 | 0 | 0 | 1 | REGP x 2.325 times |
| 1 | 0 | 1 | 0 | REGP x 2.475 times |
| 1 | 0 | 1 | 1 | REGP x 2.625 times |
| 1 | 1 | 0 | 0 | REGP x 2.700 times |
| 1 | 1 | 0 | 1 | REGP x 2.775 times |
| 1 | 1 | 1 | 0 | REGP x 2.850 times |
| 1 | 1 | 1 | 1 | Stopped |

Notes: 1. Adjust VC2-0 and VRH3-0 so that the VREG1OUT voltage is lower than 5.0 V.

**Table 7 VRL Bits and VREG2OUT Voltage**

| VRL3 | VRL2 | VRL1 | VRL0 | VREG2OUT Voltage |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | -(Vci – REGN) x 3.0 times |
| 0 | 0 | 0 | 1 | -(Vci – REGN) x 3.5 times |
| 0 | 0 | 1 | 0 | -(Vci – REGN) x 4.0 times |
| 0 | 0 | 1 | 1 | -(Vci – REGN) x 4.5 times |
| 0 | 1 | 0 | 0 | -(Vci – REGN) x 5.0 times |
| 0 | 1 | 0 | 1 | -(Vci – REGN) x 5.5 times |
| 0 | 1 | 1 | 0 | -(Vci – REGN) x 6.0 times |
| 0 | 1 | 1 | 1 | Stopped |
| 1 | 0 | 0 | 0 | -(Vci – REGN) x 6.5 times |
| 1 | 0 | 0 | 1 | -(Vci – REGN) x 7.0 times |
| 1 | 0 | 1 | 0 | -(Vci – REGN) x 7.5 times |
| 1 | 0 | 1 | 1 | -(Vci – REGN) x 8.0 times |
| 1 | 1 | 0 | 0 | -(Vci – REGN) x 8.5 times |
| 1 | 1 | 0 | 1 | -(Vci – REGN) x 9.0 times |
| 1 | 1 | 1 | 0 | -(Vci – REGN) x 9.5 times |
| 1 | 1 | 1 | 1 | Stopped |

Notes: 1. Adjust VC2-0 and VRL3-0 so that the VREG2OUT voltage is higher than –16.0 V.
2. The VREG2OUT voltage is the factor when Vci is the reference voltage.

**Voltage Setting 2 (R02h)**

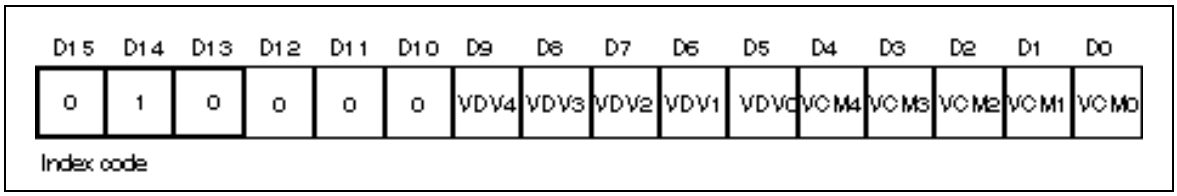



**Figure 4 Voltage Setting 2 Instructions**

**VCM4-0:** Set the VcomH voltage (a high-level voltage at the Vcom alternating drive).
These bits amplify the VcomH voltage 0.4 to 0.98 times the VREG1 voltage. When VCOM3-0 ALL= 1, the adjustment of the internal volume stops, and VcomH can be adjusted from VcomR by an external resistor.

**VDV4-0:** Set the alternating amplitudes of Vcom and Vgoff at the Vcom alternating drive.
These bits amplify Vcom and Vgoff 0.6 to 1.23 times the VREG1 voltage. When the Vcom alternation is not driven, the settings become invalid.

**Table 8 VCM4-0 Bits and VcomH Voltage**

| VCM4 | VCM3 | VCM2 | VCM1 | VCM0 | VcomH Voltage |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | VREG1 x 0.40 times |
| 0 | 0 | 0 | 0 | 1 | VREG1 x 0.42 times |
| 0 | 0 | 0 | 1 | 0 | VREG1 x 0.44 times |
| : | : | : | : | : | : |
| 0 | 1 | 1 | 0 | 0 | VREG1 x 0.64 times |
| 0 | 1 | 1 | 0 | 1 | VREG1 x 0.66 times |
| 0 | 1 | 1 | 1 | 0 | VREG1 x 0.68 times |
| 0 | 1 | 1 | 1 | 1 | The internal volume stops, and VcomH can be adjusted from VcomR by an external variable resistor. |
| 1 | 0 | 0 | 0 | 0 | VREG1 x 0.70 times |
| 1 | 0 | 0 | 0 | 1 | VREG1 x 0.72 times |
| 1 | 0 | 0 | 1 | 0 | VREG1 x 0.74 times |
| : | : | : | : | : | : |
| 1 | 1 | 1 | 0 | 0 | VREG1 x 0.94 times |
| 1 | 1 | 1 | 0 | 1 | VREG1 x 0.96 times |
| 1 | 1 | 1 | 1 | 0 | VREG1 x 0.98 times |
| 1 | 1 | 1 | 1 | 1 | The internal volume stops, and VcomH can be adjusted from VcomR by an external variable resistor. |

Note: Adjust VREG1 and VCM4-0 so that the VcomH voltage is lower than VDH.

**Table 9 VDV4-0 Bits and Vcom Amplitude**

| VDV4 | VDV3 | VDV2 | VDV1 | VDV0 | Vcom Amplitude |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | VREG1 x 0.60 times |
| 0 | 0 | 0 | 0 | 1 | VREG1 x 0.63 times |
| 0 | 0 | 0 | 1 | 0 | VREG1 x 0.66 times |
| : | : | : | : | : | : |
| 0 | 1 | 1 | 0 | 0 | VREG1 x 0.96 times |
| 0 | 1 | 1 | 0 | 1 | VREG1 x 0.99 times |
| 0 | 1 | 1 | 1 | 0 | VREG1 x 1.02 times |
| 0 | 1 | 1 | 1 | 1 | Setting inhibited |
| 1 | 0 | 0 | 0 | 0 | VREG1 x 1.05 times |
| 1 | 0 | 0 | 0 | 1 | VREG1 x 1.08 times |
| 1 | 0 | 0 | 1 | 0 | VREG1 x 1.11 times |
| 1 | 0 | 0 | 1 | 1 | VREG1 x 1.14 times |
| 1 | 0 | 1 | 0 | 0 | VREG1 x 1.17 times |
| 1 | 0 | 1 | 0 | 1 | VREG1 x 1.20 times |
| 1 | 0 | 1 | 1 | 0 | VREG1 x 1.23 times |
| 1 | 0 | 1 | 1 | 1 | Setting inhibited |
| 1 | 1 | * | * | * | |

Note: Adjust VREG1 and VDV4-0 so that the Vcom and Vgoff amplitudes are lower than 6.0 V.

## Gate Serial Transfer

The register settings are transferred from HD66770. The interface consists of a chip select (GCS*), a transfer clock (GCL), and data input (GDA) lines.

The data transfer starts when the falling edge of the GCS* line indicates that the data is to be transferred. The transfer ends when the rising edge of the GCS* line indicates that the transfer is over. The bits are transferred in 16-bit units, and the data is transferred in the order from MSB to LSB.

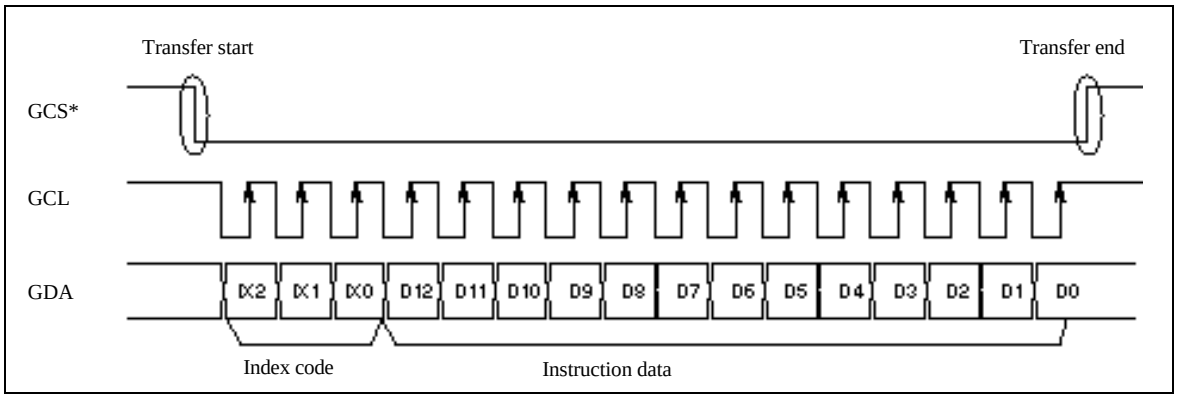



**Figure 5 Format for Data Transfer**

## Reset Functions

HD667P00 sets the internal initialization with the RESET pin. Input a power-on reset signal when the power is applied the same HD66770 and HD66771. Table 10 shows the initial setting values.

**Table 10 Initial Setting Values for Registers at Reset**

| Index Code | Control Bit | Initial Value | Status |
|---|---|---|---|
| R00h | SLP | 0 | Cancels sleep mode. |
| | AP2-0 | 000 | Stops operational amplifier and step-up circuit operations. |
| | DC2-0 | 000 | Step-up cycle: Equal to DCCLK |
| | GON | 0 | Vcom and Vgoff output control for display off: GND |
| | BT2-0 | 000 | Step-up factor VLOUT2 = Vci x five times |
| | VCOMG | 0 | Vcom output control for display on: GND |
| R01h | VC2-0 | 000 | Internal reference voltage of VREG1OUT/Vciout: 0.92 Vci<br>Internal reference voltage of VREG2OUT: 0.08 Vci |
| | PON | 0 | Stops the step-up circuits. |
| | VRH3-0 | 0000 | VREG1OUT output voltage: REGP x 1.45 times |
| | VRL3-0 | 0000 | VREG2OUT output voltage: -(Vci - REGN) x 3.0 times |
| | CAD | 0 | Structure for TFT-display retention volume: Cst |
| R02h | VCM4-0 | 00000 | VcomH output voltage: VREG1 x 0.4 times |
| | VDV4-0 | 00000 | Vcom amplitude: VREG1 x 0.6 times |

## Flow of Power-Supply Setting

Apply the power in a sequence as shown in figure 6.
The stable times of the oscillation circuit, step-up circuit, and operational amplifier depend on the external resistor or capacitance.
After the serial signal transfer has started by TE and IDX2-0 in HD66770, the mode settings of HD66771 and HD667P00 become valid with a delay of CL1 = 1 cyc. Take this fact into account when setting the modes.

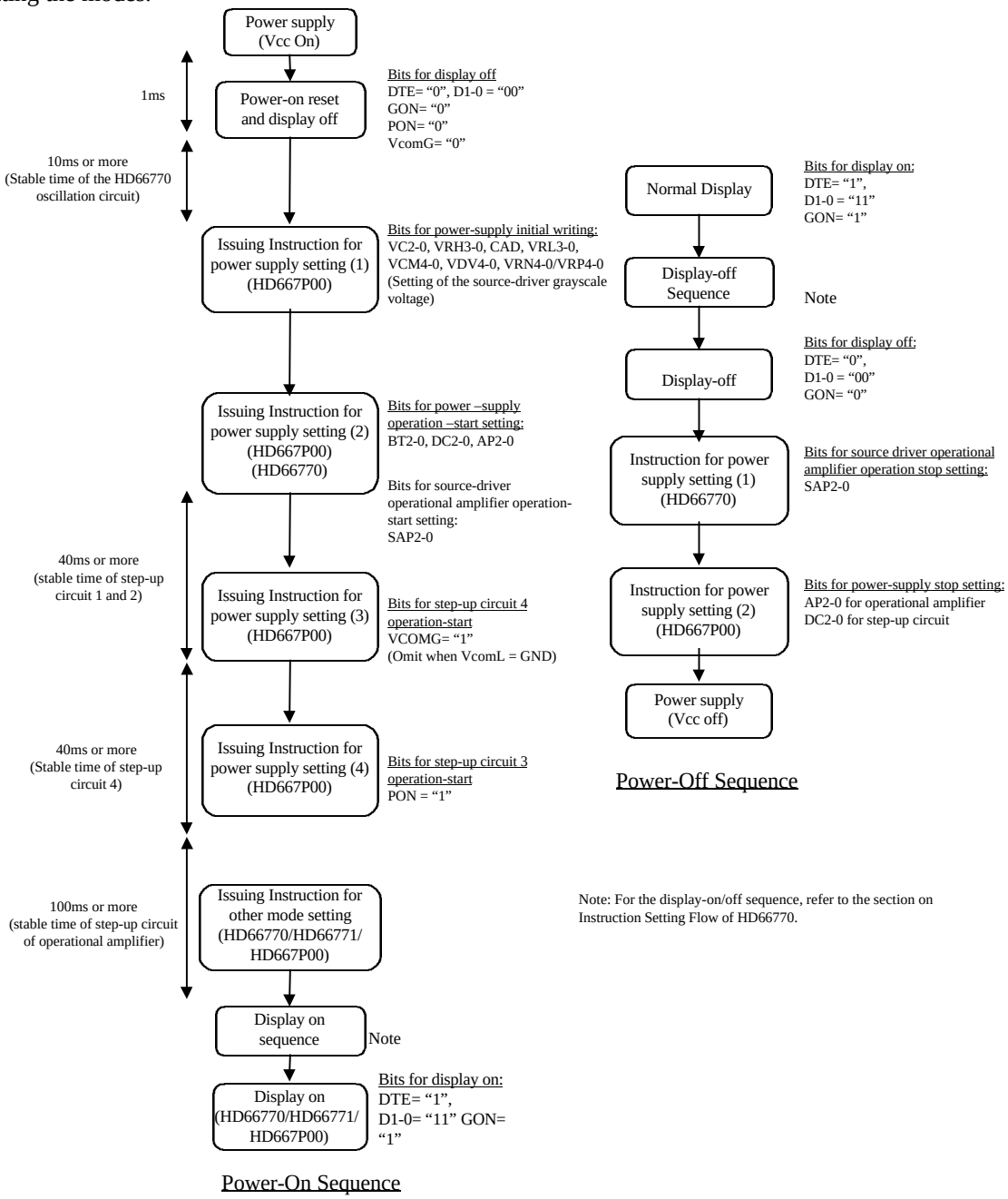
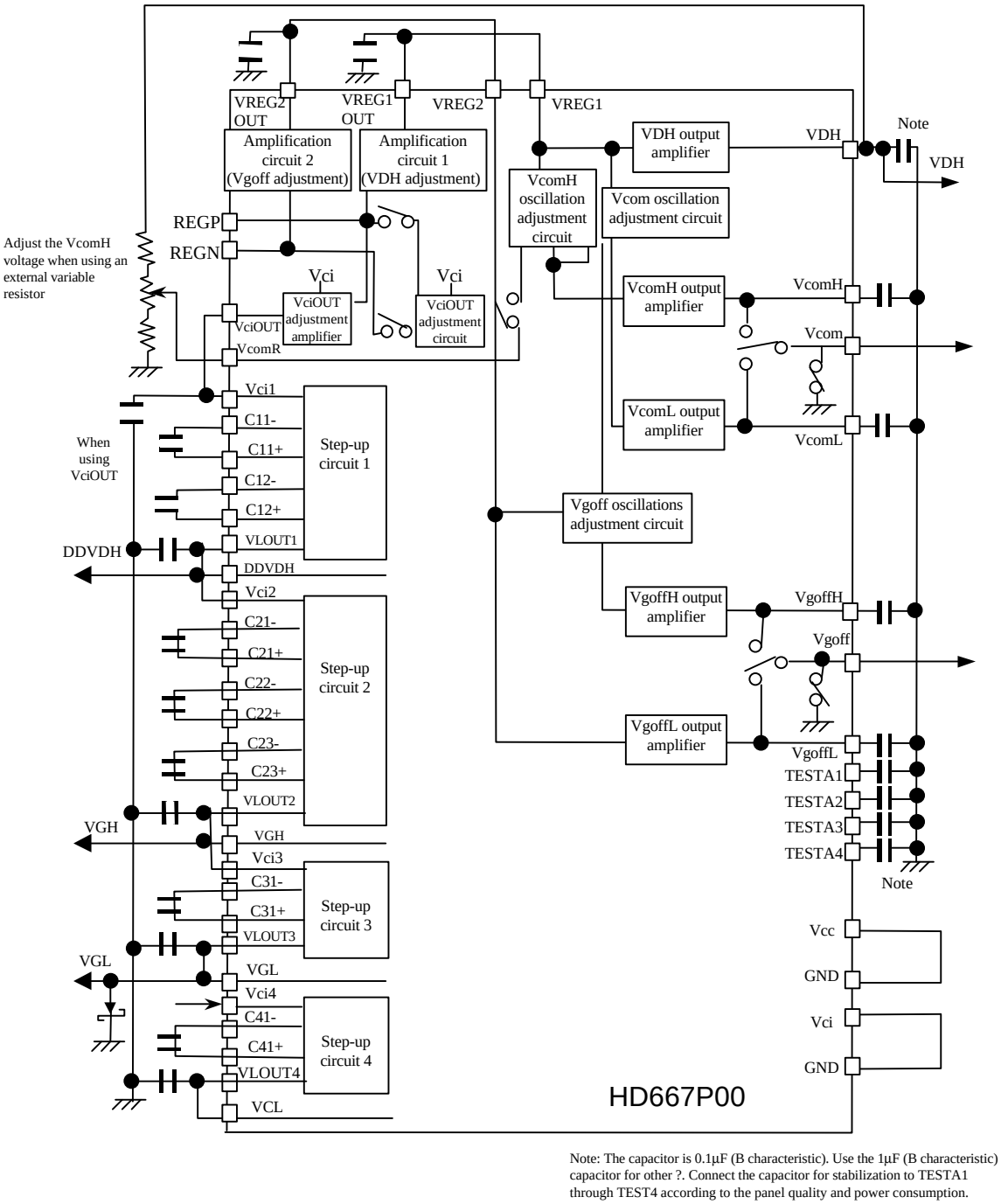



**Figure 6 Flow of Power-Supply Setting**

## Configuration of Internal Power-Supply Generation Circuit

Figure 7 shows a configuration of the voltage generation circuit for HD66770/771 of HD667P00. The step-up circuits consist of step-up circuits 1 to 4. Step-up circuit 1 doubles or triples the voltage supplied to Vci1, and that voltage is doubled, tripled, or quadrupled in step-up circuit 2. Step-up circuit 3 reverses the VGH level with reference to GND and generates the VGL level. Step-up circuit 4 reverses the Vci level with reference to GND and generates the VCL level. These step-up circuits generate power supplies DDVDH, VDH, VGH, VGL, Vgoff, and Vcom required for HD66770/771, or TFT display panel counter electrode. Reference voltages VDH, Vcom, and Vgoff for the HD66770 grayscale voltage are amplified in amplification circuits 1 and 2 from the internal-voltage adjustment circuit, and generate each level depending on that voltage. The Vcom and Vgoff voltages can be alternated with any voltages. Connect DDVDH and VDH to HD66770, VGH, VGL, and Vgoff to HD66771, and Vcom to the panel and HD66770.




Note: The capacitor is 0.1µF (B characteristic). Use the 1µF (B characteristic) capacitor for other ?. Connect the capacitor for stabilization to TESTA1 through TEST4 according to the panel quality and power consumption.

**Figure 7 Configuration of the Internal Power-Supply Circuit**

## Pattern Diagrams for Voltage Setting

Figure 8 shows a pattern diagram for the HD667P00 voltage setting and an example of waveforms when HD667P00 is combined with HD66770 and HD66771.

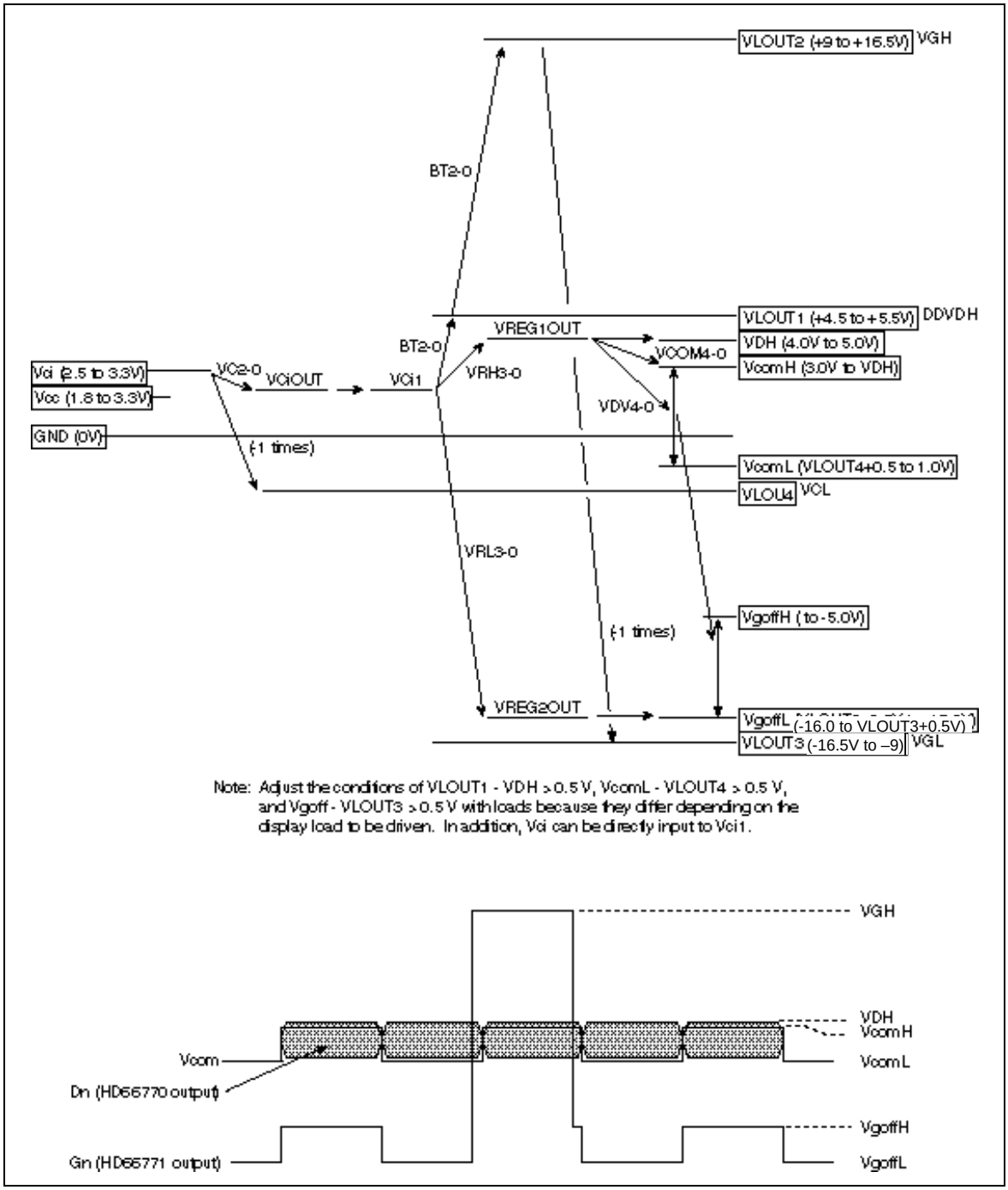



**Figure 8 Pattern Diagram and an Example of Waveforms**

## Example of System Configuration

Figure 9 shows a TFT-LCD panel with 132 (horizontal)-by-176 (vertical) dots, configured by using the HD66770 source driver and HD66771 gate driver.

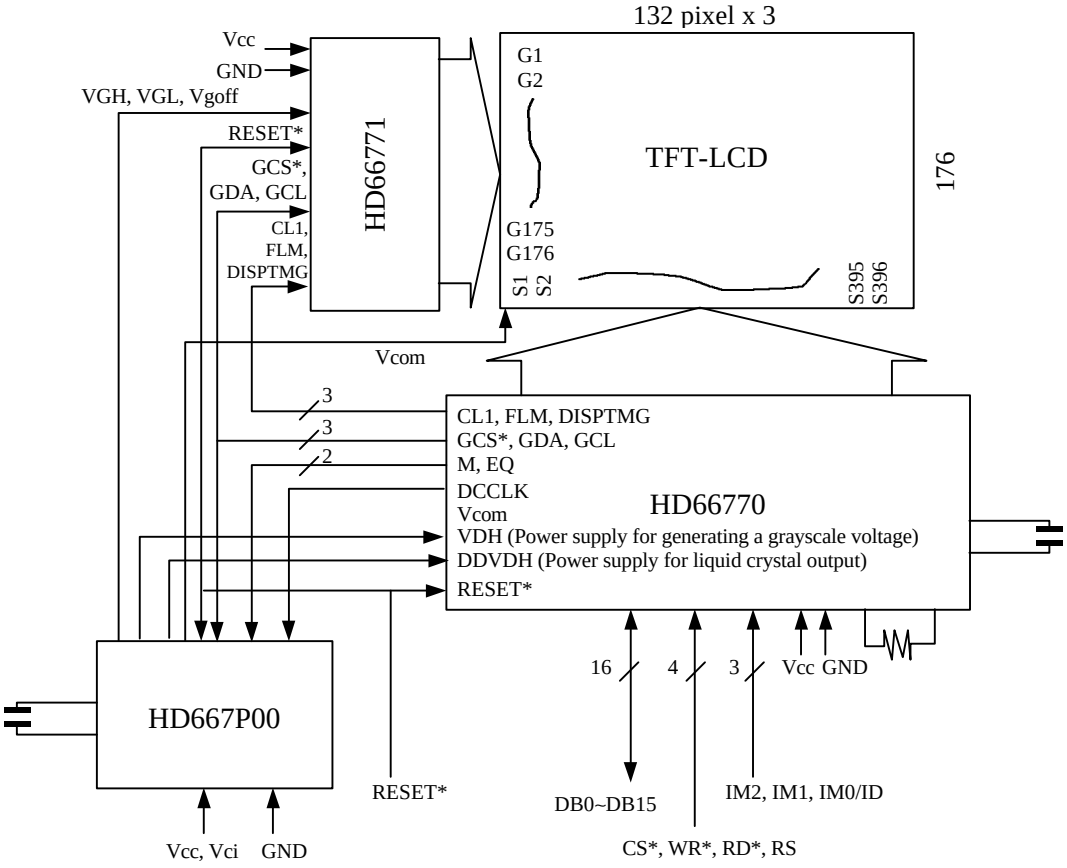
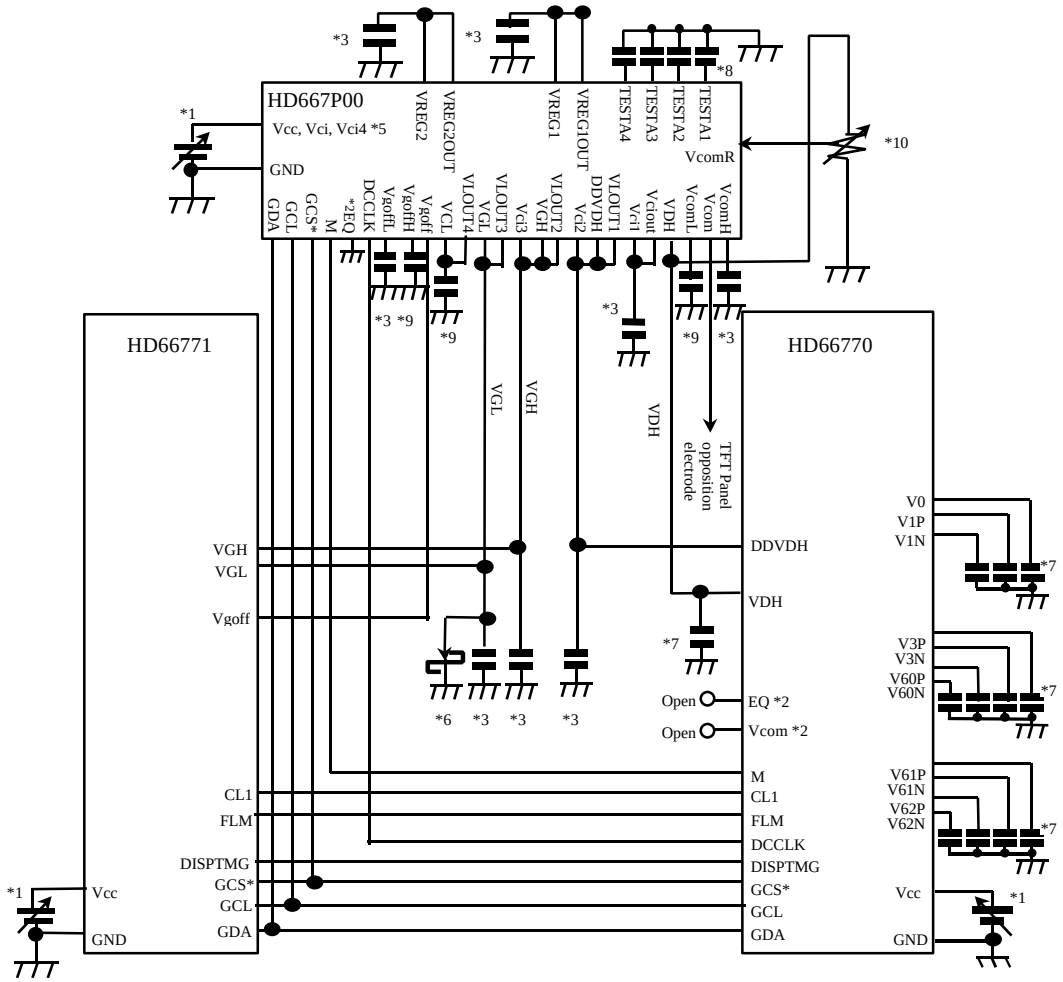



**Figure 9 System Configuration**

## Example of Connection to HD66770 and HD66771

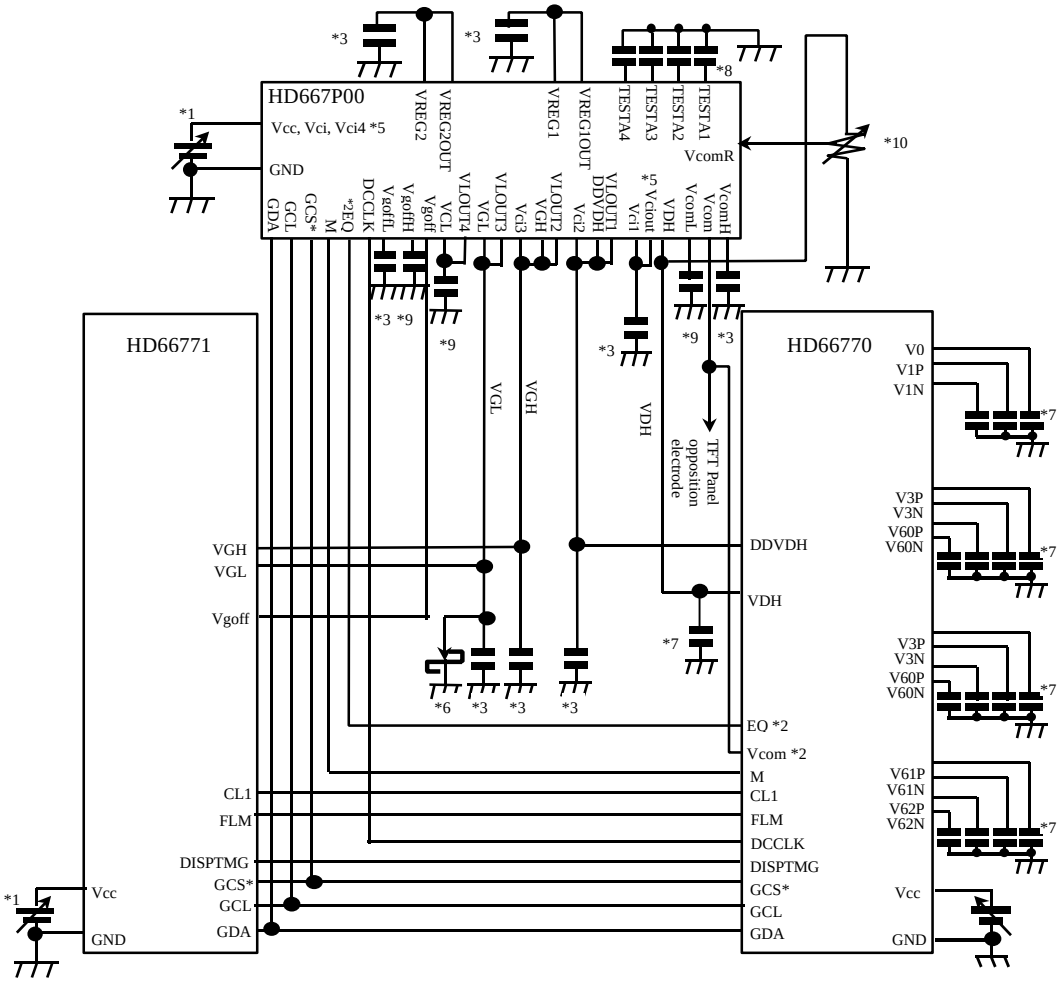
Connection differs according to the voltage setting of Vcom. Figure 10 shows an example of connection to HD66770 and HD66771 when VcomL < 0 V.




Notes:
1. All Vcc and GND input to HD66770, HD66771, and HD667P00 must be the same.
2. Leave the EQ and Vcom pins of HD66770 open. Set the EQ pin of HD667P00 to GND.
3. Use the 1-µF capacitor (B characteristics) as a capacitor for stabilization to be connected.
4. There is no description of how to connect the capacitors of C11- to C12-, C11+ to C12+, C21- to C23-, C21+ to C23+, C31-, C31+, C41-, and C41+ of HD667P00. Connect these capacitors according to the HD667P00 pin functions.
5. Apply 2.5V to 3.3V to Vci by using an external power supply. Apply toVci1,VCiOUT or less than 2.75V by using an external power supply. Apply 2.5V to 3.3V to Vci4 by using an external power supply.
6. Conncet the Shotkey barrier diode when VF = 0.4 V/20 mA and VR ≥ 30 V.
7. Use the 0.1-µF capacitor (B characteristics) as a capacitor for stabilization to be connected.
8. Connect the 0.1-µF capacitor (B characteristics) as a capacitor for stabilization according to the display quality and power consumption.
9. When step-up circuit 4, VcomL, and VgoffH are used, use the 1-µF capacitor (B characteristics) according to the setting mode. When they are not used, leave the pin open.
10. Use a variable resistor more than 200kΩ

**Figure 10 Example of Connection to HD66770 and HD66771 when VcomL < 0 V**

Figure 11 shows an example of connection to HD66770 source driver and HD66771 gate driver when 0 ≤ VcomL < 5.5 V.




Notes:
1. All Vcc and GND input to HD66770, HD66771, and HD667P00 must be the same.
2. Connect the EQ pins of HD66770 and HD667P00. The Vcom pin must be connected to the Vcom pin of HD667P00. Do not set the Vcom voltage higher than 5.5 V.
3. Use the 1-µF capacitor (B characteristics) as a capacitor for stabilization to be connected.
4. There is no description of how to connect the capacitors of C11- to C12-, C11+ to C12+, C21- to C23-, C21+ to C23+, C31-, C31+, C41-, and C41+ of HD667P00. Connect these capacitors according to the HD667P00 pin functions.
5. Apply 2.5V to 3.3V to Vci by using an external power supply. Apply less than 2.75V toVci1 by VCiOUT or by using an external power supply. Apply 2.5V to 3.3V to Vci4 by using an external power supply.
6. Conncet the Shotkey barrier diode when VF = 0.4 V/20 mA and VR ≥ 30 V.
7. Use the 0.1-µF capacitor (B characteristics) as a capacitor for stabilization to be connected.
8. Connect the 0.1-µF capacitor (B characteristics) as a capacitor for stabilization according to the display quality and power consumption.
9. When step-up circuit 4, VcomL, and VgoffH are used, use the 1-µF capacitor (B characteristics) according to the setting mode. When they are not used, leave the pin open.
10. Use a variable resistor more than 200kΩ

**Figure 11 Example of Connection to HD66770 and HD66771 when 0 V £ VcomL < 5.5 V**

## Specifications for the Capacitor Connected to HD667P00

Table 11 shows the specifications for the capacitor connected to HD667P00.

**Table 11 Specifications for the Capacitor Connected to HD667P00**

| Product | Capacitor | Recommended Breakdown Voltage | Connected Pin (19 in Total) |
|---|---|---|---|
| HD667P00 | 1 µF (B characteristics) | 6 V | VREG1OUT, Vciout, C41-/+[*1], VLOUT4[*1], VcomH, VcomL[*1] |
| | | 10 V | VLOUT1, C11-/+, C12-/+, C21-/+, C22-/+, C23-/+ |
| | | 25 V | VREG2OUT, VLOUT2, VLOUT3, C31-/+, VgoffH[*1], VgoffL |
| | 0.1 µF (B characteristics) | 6 V | VDH, (TESTA1)[*2], (TESTA2)[*2] |
| | | 25 V | (TESTA3)[*2], (TESTA4)[*2] |

Notes: 1. These pins may be unnecessary depending on the mode setting.
2. Connect the capacitor for stabilization according to the display quality and power consumption.

## Absolute Maximum Ratings

| Item | | Symbol | Ratings | Unit | Notes |
|---|---|---|---|---|---|
| Power supply voltage | Logic circuit | Vcc | -0.3 to +7.0 | V | 1 |
| | Analogue Circuit | Vci - GND | -0.3 to +10.0 | V | 1 |
| | LCD drive circuit | DDVDH - VLC | -0.3 to +10.0 | V | 1 |
| | | GND - VCL | -0.3 to +7.0 | V | 1 |
| | | VGH - GND | -0.3 to +18.5 | V | 1 |
| | | GND - VGL | -0.3 to +18.5 | V | 1 |
| Input voltage | | VT1 | -0.3 to Vcc + 0.3 | V | 1, 2 |
| Operating temperature | | topr | -40 to +85 | °C | |
| Storage temperature | | Tstg | -55 to +110 | °C | |

Notes: 1. Voltage from GND.
2. Applies to the EQ, DCCLK, GCS*, GDA, GCL, M, and RESET pins.

Note: If the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

## Electrical Characteristics

**DC Characteristics (VCC = 1.8 to 3.3 V, GND = 0 V, VGH - VGL = 18 to 33 V, Ta = -40 to +85ºC)[*1]**

| Item | Symbol | Test Condition | min. | typ. | max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Input high voltage | VIH | | 0.8 x Vcc | - | Vcc | V | 2 |
| Input low voltage | VIL | | 0 | - | 0.2 x Vcc | V | 2 |
| Input leakage current | IIL | Vin = 0 to VCC | -1.0 | - | +1.0 | µA | 2 |
| Current consumption 1 | IVci | Vcc - GND = 3 V, Vci - GND = 3 V, fM = 6.25 kHz, fDCCLK = 25kHz | - | 400 | 600 | µA | 3 |

Notes: 1. For electrical characteristics, guaranteed at 85°C.
2. Applies to the EQ, DCCLK, GCS*, GDA, GCL, and RESET pins.
3. Values when no load current flows on the VDH, VGH, VGL, Vgoff, and Vcom pins.

**AC Characteristics (VCC = 1.8 to 3.3 V, VGH - VGL = 18 to 33 V)**

| Item | Symbol | Pin | min. | typ. | max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| GCL rising time | tr | GCL | - | - | 100 | ns | |
| GCL falling time | tf | GCL | - | - | 100 | ns | |
| GCL cycle time | tcycG | GCL | 2.5 | - | 10 | µs | |
| CCL high-level width | tCWHG | GCL | 1.0 | - | - | µs | |
| CCL low-level width | tCWLG | GCL | 1.0 | - | - | µs | |
| GDA setup time | tGDS | GCL, GDA | 1.0 | - | - | µs | |
| GDA hold time | tGDH | GCL, GDA | 1.0 | - | - | µs | |
| GCS low setup time | tGSL | GCL, GCS* | 1.0 | - | - | µs | |
| GCS high hold time | tGHH | GCL, GCS* | 1.0 | - | - | µs | |
| RESET low-level width | tRES | RESET* | 1 | - | - | ms | |
| RESET rising time | trRES | RESET* | - | - | 10 | µs | |

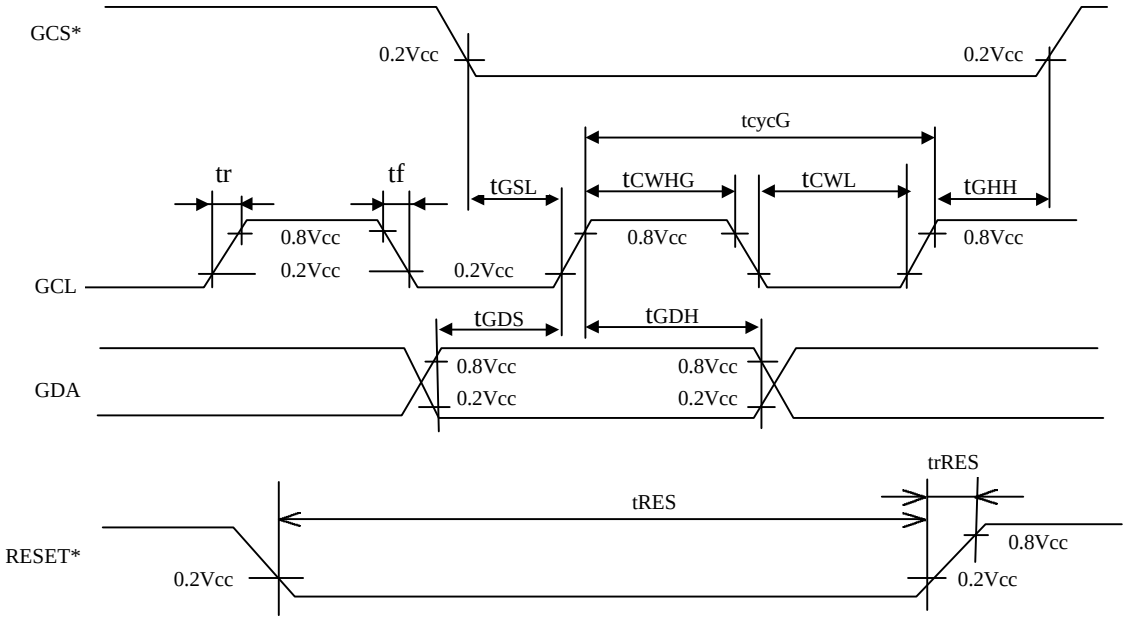



**Figure 12 AC Timing**

**Revision History**

| Rev. | Date | Page | Content |
|---|---|---|---|
| 0.6 | April, 2001 | | |
| 1.0 | February, 2002 | 1 | Delete a sentence in the Item “Input power-supply voltage”. (Vci1-GND = 2.5 to 3.3V (power supply for step-up circuits) |
| | | 3 | Add “HD66771” in the cell “Connected to” for VGH and VGL |
| | | | Correct a Function explanation sentence for VGH , VGL, and Vci. |
| | | 4 | Delete “HD66771” from the cell “Connected to” for VLOUT2 and VLOUT3. |
| | | | Correct a Function explanation sentence for VLOUT2 and VLOUT3. |
| | | | Correct “Connected to” for Vci4 (from “Vcc or Vci1” to “Vci”) Correct “Function” for Vci4. (from “lower than 3.3V” to “lower than 2.5 to 3.3V”) |
| | | 5 | Delete a Function explanation sentence for VREG1OUT. (When the internal reference voltage is not used, the reference voltage can be generated from the voltage of REGP.) |
| | | | Correct Function explanation sentence for VREG1. |
| | | | Delete a Function explanation sentence for VREG2OUT. (When the internal reference voltage is not used, the reference voltage can be generated from the voltage of REGP.) |
| | | | Correct Function explanation sentence for VREG2.(from “lower than 16.5V” to “lower than VGL”) |
| | | 6 | Correct “Connected to” (from “Open or power supply” to “Open or capacitor for stabilization”) |
| | | 14 | Correct explanation sentence for VCOMG. (Line2 “negative voltage stops.” to “negative voltage and a step-up circuit 4 stop.” / Line 3 “VcomL can be output.” to “VcomL can be output. When using VCOMG=1, follow the Flow of Power Supply Setting.(p22)) |
| | | 16 | Change title of rows. |
| | | | Delete Note1 for Table 6. |
| | | 17 | Change Notes for Table 7. |
| | | 22 | Change Figure 6 |
| | | 24 | Change Figure 7 |
| | | 27 | Correct Note5 and 6 for Figure 10 |
| | | 28 | Correct Note5 and 6 for Figure 11 |
| | | 31 | Add “VREG1OUT” to “Connected Pin” for 1uF-6V. Add “VREG2OUT” to “Connected Pin” for 1uF-25V. Delete “VREG1OUT” from “Connected Pin” for 0.1uF-6V. Delete “VREG2OUT” from “Connected Pin” for 0.1uF-25V. |
| | | 32 | Delete “Step-up circuit” and “LCD drive circuit”, and add “Analogue circuit” for instead. |

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|---|---|---|---|
| | | 33 | Delete “Output voltage”, “Current consumption 1”, “Current consumption 2”, “Current consumption 3”, and “Current consumption 4”. |
| | | 34 | Delete “Output delay time”, and add “RESET low-level width” and “RESET rising time” |
| | | 35 | Delete waveform of “M”, “Vcom output”, “Vgoff output”, and note. Add waveform of “RESET*”. |