# 20 characters × 2 lines transmissive character module (with LED backlight)

## RCM7011T

The RCM7011T is a transmissive, yellow mode STN type liquid crystal module with a built-in controller/driver LSI, and a display capacity of 20 characters × 2 lines.

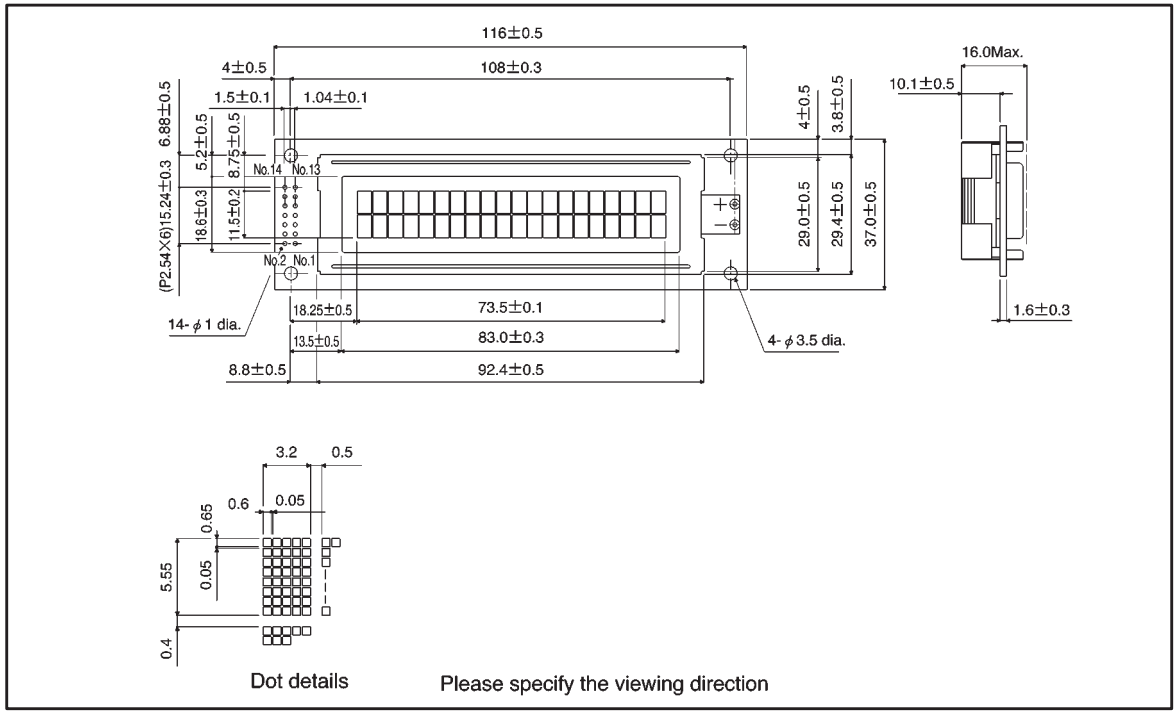
●Applications

Personal computers, word processors, facsimiles, telephones, etc.

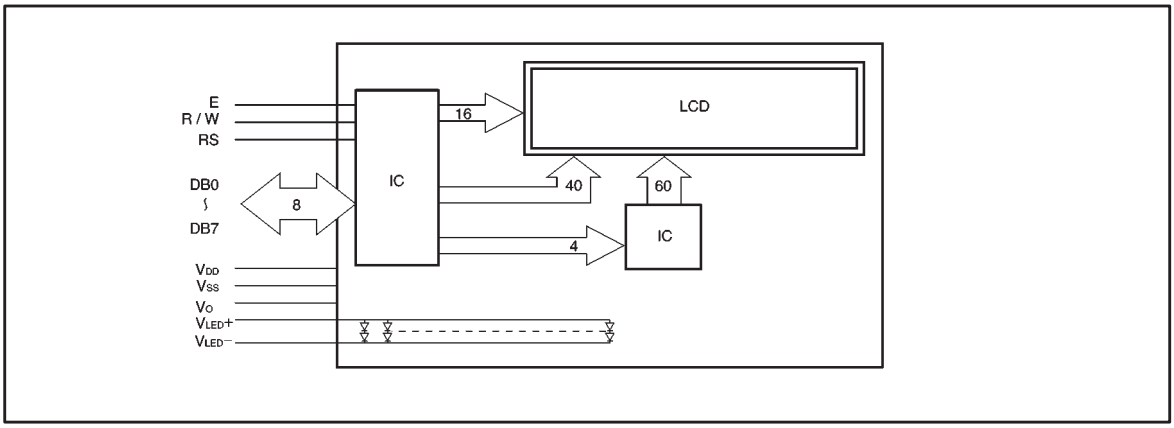
●Features

1) Wide viewing angle and high contrast.
2) 5 × 7 dot character matrix with cursor.
3) Interfaces with 4-bit or 8-bit MPUs.
4) Displays up to 226 characters and special symbols.
5) Custom character patterns are displayed with the character RAM.
6) Abundant instruction set including clear display, cursor on/off, and character blinking.
7) Compact and light weight for easy assembly to the host instrument.
8) Operable on single 5 V power supply.
9) Low power consumption.

●External dimensions (Units: mm)



●Block diagram




●Pin assignments

| Pin no. | Signal | Pin no. | Signal |
|---|---|---|---|
| 1 | $V_{SS}$ | 8 | DB1 |
| 2 | $V_{DD}$ | 9 | DB2 |
| 3 | $V_O$ | 10 | DB3 |
| 4 | RS | 11 | DB4 |
| 5 | R / W | 12 | DB5 |
| 6 | E | 13 | DB6 |
| 7 | DB0 | 14 | DB7 |

●Power supply example

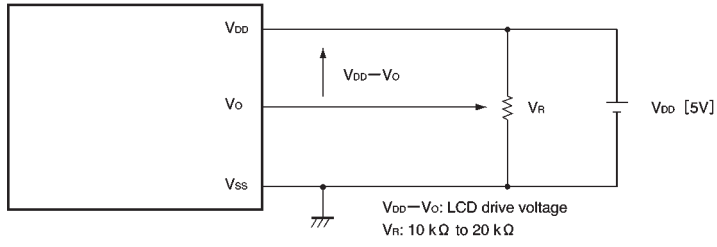



Fig.1

●Absolute maximum ratings (Ta = 25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Logic power supply voltage | $V_{DD}$-$V_{SS}$ | 0 | — | 6.5 | V |
| LCD drive voltage | $V_{DD}$-$V_O$ | 0 | — | 6.5 | V |
| Input voltage | $V_{IN}$ | $V_{SS}$ | — | $V_{DD}$ | V |
| Operating temperature | Topr | 0 | — | 50 | ℃ |
| Storage temperature | Tstg | −20 | — | 70 | ℃ |

●Electrical characteristics ($V_{DD}$ = 5.0 V ± 0.25 V, Ta = 25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Input high level voltage | $V_{IH}$ | 2.0 | — | $V_{DD}$ | V | |
| Input low level voltage | $V_{IL}$ | — | — | 0.8 | V | |
| Output high level voltage | $V_{OH}$ | 2.4 | — | — | V | $-I_{OH}$=1.2mA |
| Output low level voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$=2mA |
| Power supply current | $I_{DD}$ | — | 1.5 | 3 | mA | $V_{DD}$=5V |
| LED reverse current | $I_R$ | — | — | 1.2 | mA | $V_R$=8V |
| LED forward voltage | $V_F$ | 3.8 | 4.1 | 4.2 | V | $V_F$=120mA |

●Optical characteristics (Ta = 25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Rise time | $t_r$ | — | 100 | 250 | ms | $\theta$=10°, $\phi$=0° |
| Fall time | $t_d$ | — | 150 | 250 | ms | $\theta$=10°, $\phi$=0° |
| Contrast ratio | K | — | 3 | — | — | $\theta$=10°, $\phi$=0° |
| Viewing angle | $\theta_1$ | — | — | 10 | deg | $\phi$=0°, K≧1.4 |
| | $\theta_2$ | 40 | — | — | deg | $\phi$=0°, K≧1.4 |
| | $\phi$ | ±30 | — | — | deg | $\theta_1$=20°, K≧1.4 |

(1) Definition of $\theta$ and $\phi$

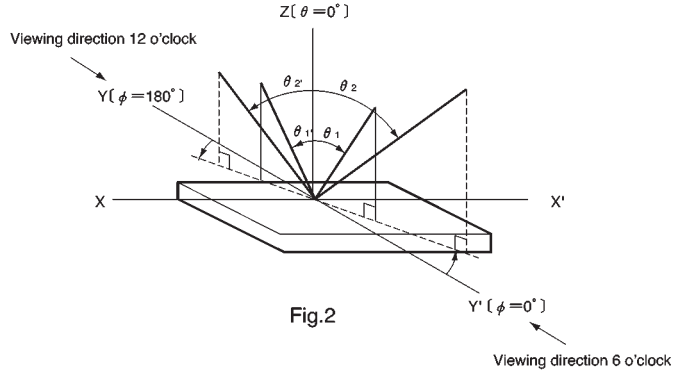



Fig.2

(2) Definition of viewing angles $\theta_1$ and $\theta_2$

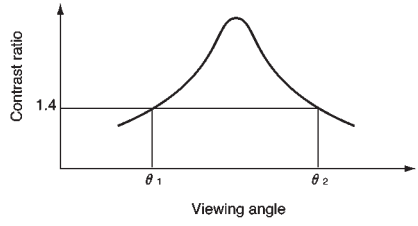



Fig.3

(3) Definition of contrast ratio"K"

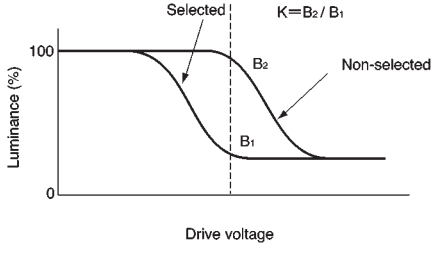



Fig.4

(4) Definition of optical response

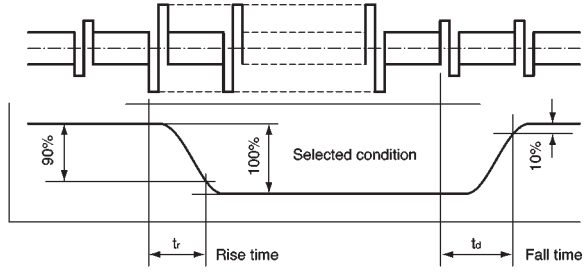



Fig.5

●Timing chart

(1) Writing

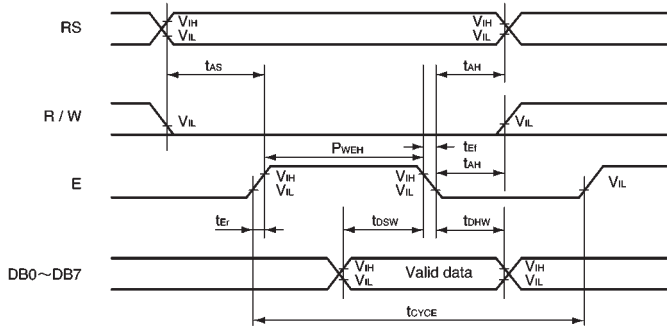



Fig. 6

| Parameter | Symbol | Min. | Typ. | Max. | Unit | |
|---|---|---|---|---|---|---|
| Enable cycle time | $t_{CYCE}$ | 500 | — | — | ns | Fig.6 |
| Enable pulse time | $P_{WEH}$ | 220 | — | — | ns | Fig.6 |
| Enable rise and fall time | $t_{Er}$, $t_{Ef}$ | — | — | 20 | ns | Fig.6 |
| Address setup time | $t_{AS}$ | 40 | — | — | ns | Fig.6 |
| Address hold time | $t_{AH}$ | 10 | — | — | ns | Fig.6 |
| Data setup time | $t_{DSW}$ | 60 | — | — | ns | Fig.6 |
| Data hold time | $t_{DHW}$ | 10 | — | — | ns | Fig.6 |

(2) Reading

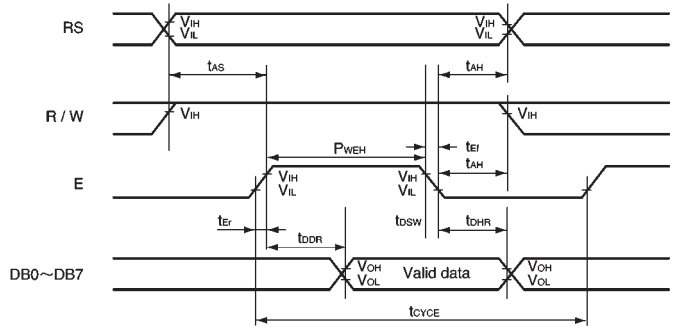



Fig. 7

| Parameter | Symbol | Min. | Typ. | Max. | Unit | |
|---|---|---|---|---|---|---|
| Enable cycle time | $t_{CYCE}$ | 500 | — | — | ns | Fig.7 |
| Enable pulse time | $P_{WEH}$ | 220 | — | — | ns | Fig.7 |
| Enable rise and fall time | $t_{Er}$, $t_{Ef}$ | — | — | 20 | ns | Fig.7 |
| Address setup time | $t_{AS}$ | 40 | — | — | ns | Fig.7 |
| Address hold time | $t_{AH}$ | 10 | — | — | ns | Fig.7 |
| Data delay time | $t_{DDR}$ | — | — | 120 | ns | Fig.7 |
| Data hold time | $t_{DHR}$ | 20 | — | — | ns | Fig.7 |

●Pin functions

| Symbol | Level | Input / output | Function | |
|---|---|---|---|---|
| $V_{SS}$ | — | — | GND : 0V | Power supply voltage |
| $V_{DD}$ | — | — | 5V | |
| $V_O$ | — | — | | |
| RS | H / L | Input | Register selection signal.<br>0: Instruction register (writing)<br>Busy flag, address counter (reading)<br>1: Data register (reading / writing) | |
| R / W | H / L | Input | Reading (R) and writing (W) selection signal.<br>"0": Writing MPU → LCD module<br>"1": Reading MPU ← LCD module | |
| E | H,H→L | Input | Data reading and writing start signal. | |
| DB0 ≀ DB3 | H / L | Input / output | The lower 4 line data buses are bi-directional and used for data transfer between the MPU and the module. They are not used during 4-bit operation. | |
| DB4 ≀ DB7 | H / L | Input / output | The upper 4 line data buses are bi-directional and used for data transfer between the MPU and the module. DB7 can also be used as a busy flag. | |

Note: In order to be able to interface with 4-bit or 8-bit MPUs, the module supports data transfer with two transmissions of 4 bits at a time or one transmission of 8 bits at once.

(1) When the interface data length is 4 bits, data is transferred along DB4 through DB7 buses and DB0 through DB3 buses are not used. Data transferal is completed after two transfers of 4 bit data. First the upper nibble (contents of DB4 through DB7 during 8-bit interfacing) is transferred and then the lower nibble (contents of DB0 through DB3 during 8-bit interfacing) is transferred.

(2) When the interface data length is 8 bits, the data DB0 through DB7 is transferred along the eight data buses.

●Instructions

| Instruction | Code | | | | | | | | | | Description | Execution time |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | fCP=250kHz |
| Clear display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Clears display and sets address 0 of DD RAM to address counter. | 1.64ms |
| Home cursor | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | Sets address 0 of DD RAM to address counter and returns a shifted display to original position. The contents of DD RAM are unchanged. | 1.64ms |
| Entry mode set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets the cursor move direction and specifies whether or not to shift display. This operation occurs when reading or writing data. | 40 μs |
| Display on / off control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Turns display on or off [D], turns cursor on or off [C], or blinks the character at the cursor position [B]. | 40 μs |
| Cursor / display shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | * | * | Moves cursor or shifts display without changing the DD RAM. | 40 μs |
| Function set | 0 | 0 | 0 | 0 | 1 | DL | N | F | * | * | Sets the interface data length [DL], number of lines displayed [N], and character font [F]. | 40 μs |
| CG RAM address set | 0 | 0 | 0 | 1 | ACG | | | | | | Sets the CG RAM address. Data received after this is CG RAM data. | 40 μs |
| DD RAM address set | 0 | 0 | 1 | ADD | | | | | | | Sets the DD RAM address. Data received after this is DD RAM data. | 40 μs |
| Read busy flag address | 0 | 1 | BF | AC | | | | | | | Reads the busy flag signifying internal operations in progress and reads the contents of the address counter. | 0 μs |
| Write data to CG or DD RAM | 1 | 0 | Write Data | | | | | | | | Data is written from the DD RAM or CG RAM. | 46 μs |
| Read data from CG or DD RAM | 1 | 1 | Read Data | | | | | | | | Data is read to DD RAM or CG RAM. | 46 μs |
| | I / D = 1: Increment<br>I / D = 0: Decrement<br>S = 1: Accompanies display shift<br>S / C = 1: Display shift<br>S / C = 0: Cursor movement<br>R / L = 1: Right shift<br>R / L = 0: Left shift<br>DL = 1: 8 bit<br>DL = 0: 4 bit<br>N = 1: 2 lines<br>N = 0: 1 line<br>F = 1: 5 × 10 dots<br>F = 0: 5 × 7 dots<br>BF = 1: Internal operation in progress<br>BF = 0: Instructions can be received | | | | | | | | | | DD RAM: Display data RAM<br>CG RAM: Character generator RAM<br>ACG: CG RAM address<br>ADD: DD RAM address (corresponds to cursor address)<br>AC: Address counter used for both DD and CG RAM. | Execution times will vary with frequency. |

(Note) * = Invalid

●Character code and corresponding character pattern

| Higher 4 bit / Lower 4 bit | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| XXXX0000 | CGRAM (0) | | | | | | | | | | |  | | | | | |
| XXXX0001 | (1) | | | | | | | | | | | | | | | |
| XXXX0010 | (2) | | | | | | | | | | | |  |  |  |  |
| XXXX0011 | (3) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| XXXX0100 | (4) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| XXXX0101 | (5) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| XXXX0110 | (6) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| XXXX0111 | (7) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| XXXX1000 | (0) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| XXXX1001 | (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| XXXX1010 | (2) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| XXXX1011 | (3) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| XXXX1100 | (4) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| XXXX1101 | (5) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| XXXX1110 | (6) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |
| XXXX1111 | (7) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

●Reset function

When you turn the power supply on using the internal reset circuit, the module automatically returns to its initial (reset) settings. At the initial settings, the following instructions are carried out.

(1) Clear display

The busy flag remains in the busy condition (BF = 1) until initialization is completed. This takes 15 ms.

(2) Function set

DL = 1: 8-bit interface data length

N = 1

F = 0: 5 × 7 dot matrix

(3) Display on/off control

D = 0: Display off

C = 0: Cursor off

B = 0: Blinking off

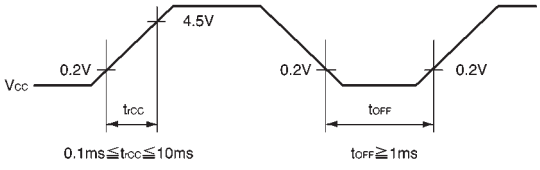
(4) Entry mode set

1/D = 1: +1 (increment)

S = 0: No shift

(5) Select DD RAM

Depending on the power supply's rise and fall times when it is turned on, there may be times when the initialization cannot be completed. Therefore, be aware of the following timing relationship.




$t_{OFF}$ regulates the power supply breaks, or on and off times.

Note) When the above power supply conditions are not met, the internal reset circuit will not operate properly.